PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

MITSUBISHI MICROCOMPUTERS

M37710EFBXXXFP
M37710EFBFS

PROM VERSION of M37710MFBXXXFP

DESCRIPTION

The M37710EFBXXXFP is a built-in PROM single-chip microcomputer designed with high-performance CMOS silicon gate technology. This is housed in a 80-pin plastic molded QFP. The features of this chip are similar to those of the M37710MFBXXXFP except that this chip has a 120K-byte PROM built in.

This single-chip microcomputer has a large 16M bytes address space, three instruction queue buffers, and two data buffers for high-speed instruction execution. The CPU is a 16-bit parallel processor that can also be switched to perform 8-bit parallel processing. This microcomputer is suitable for office, business, and industrial equipment controller that require high-speed processing of large data.

Since general purpose PROM writer can be used for the built-in PROM, this chip is suitable for small quantity production runs. For program development, the M37710EFBFS with erasable ROM that is housed in a windowed ceramic LCC is also provided.

FEATURES

- Number of basic instructions 103
- Memory size PROM ..... 120K bytes
  RAM ..... 2048 bytes
- Instruction execution time
  The fastest instruction at 25MHz frequency 160ns
- Single power supply ..... 5V±10%
- Low power dissipation (at 25MHz frequency) ..... 95mW (Typ.)
- Interrupts ..... 19 types 7 levels
- Multiple function 16-bit timer ..... 5+3
  (Pulse motor drive waveform can be output.)
- UART (may also be synchronous) 2
- 10-bit A-D converter ..... 8-channel inputs
- 8-bit D-A converter ..... 2-channel outputs
- 12-bit watchdog timer
- Programmable input/output
  (ports P0, P1, P2, P3, P4, P5, P6, P7, P8) 68

APPLICATION

Control devices for office equipment such as copiers, printers, typewriters, facsimiles, word processors, and personal computers

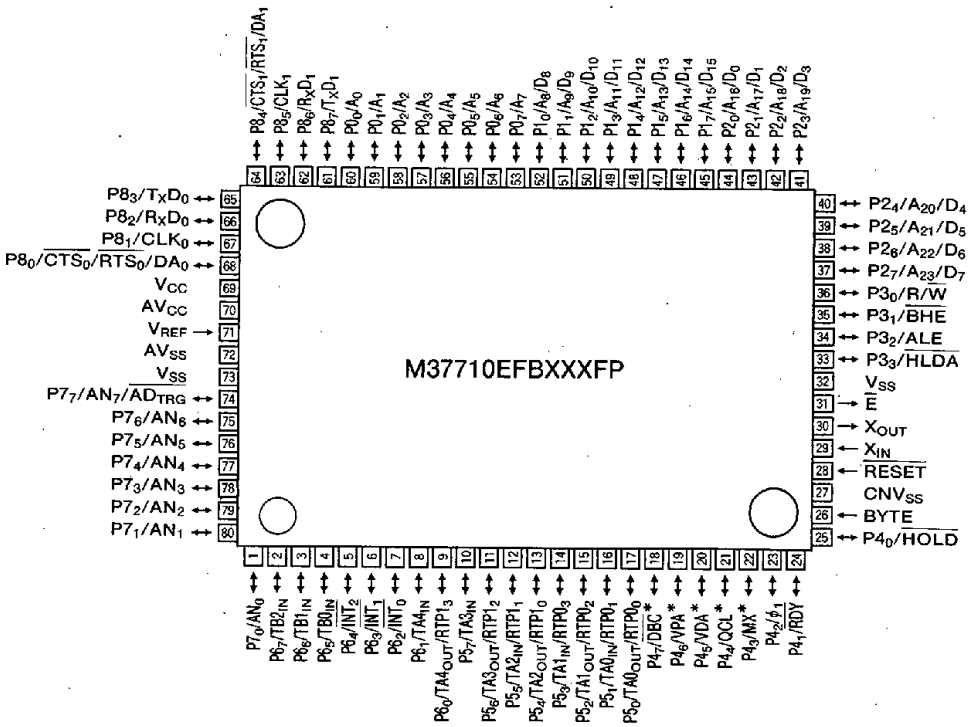
Control devices for industrial equipment such as NC, communication and measuring instruments

NOTE

(1) Do not use the M37710EFBFS for mass production because it is a tool for program development (for evaluation).

(2) Refer to "Chapter 5 PRECAUTIONS" when using this microcomputer.

PIN CONFIGURATION (TOP VIEW)



Outline 80P6N-A

*: Used in the evaluation chip mode only

PRELIMINARY
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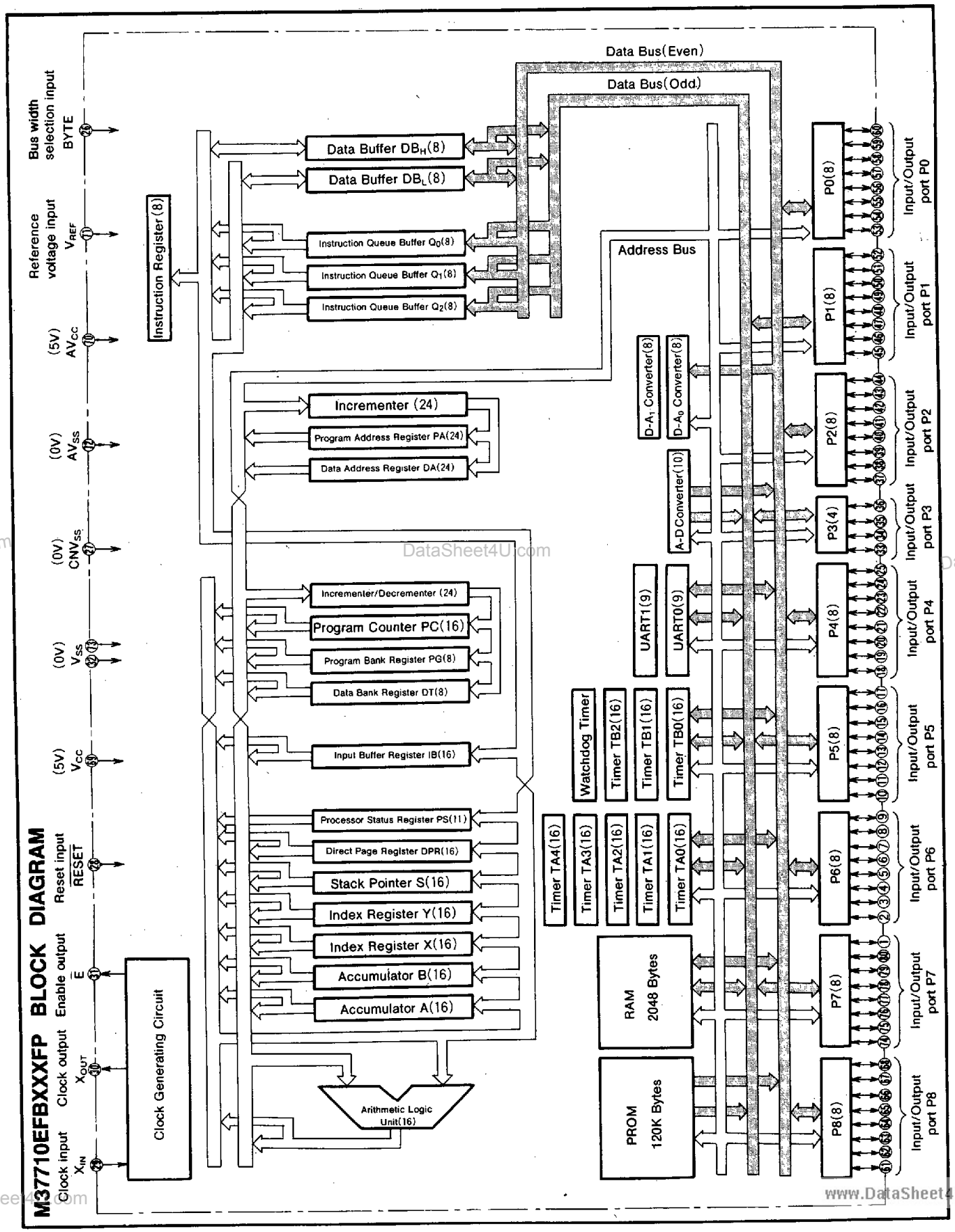
M37710EFBXXXFP BLOCK DIAGRAM



M37710EFBXXXFP
M37710EFBFS

PRELIMINARY
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PROM VERSION of M37710MFBXXXFP

FUNCTIONS OF M37710EFBXXXFP

Parameter		Functions
Number of basic instructions		103
Instruction execution time		160ns (the fastest instruction at external clock 25MHz frequency)
Memory size	PROM	120K bytes
	RAM	2048 bytes
Input/Output ports	P0～P2, P4～P8	8 -bit× 8
	P3	4 -bit× 1
Multi-function timers	TA0, TA1, TA2, TA3, TA4	16-bit× 5
	TB0, TB1, TB2	16-bit× 3
Serial I/O		(UART or clock synchronous serial I/O)×2
A-D converter		10-bit× 1 (8 channels)
D-A converter		8 -bit× 2
Watchdog timer		12-bit× 1
Interrupts		3 external types, 16 internal types (Each interrupt can be set the priority levels to 0～7.)
Clock generating circuit		Built-in(externally connected to a ceramic resonator or quartz crystal resonator)
Supply voltage		5 V±10%
Power dissipation		95mW(at external clock 25MHz frequency)
Input/Output characteristic	Input/Output voltage	5 V
	Output current	5 mA
Memory expansion		Maximum 16M bytes
Operating temperature range		−20～85℃
Device structure		CMOS high-performance silicon gate process
Package	M37710EFBXXXFP	80-pin plastic molded QFP
	M37710EFBFS	80-pin ceramic LCC (with a window)

PRELIMINARY
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PIN DESCRIPTION

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5 V±10% to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	CNV_{SS} input	Input	This pin controls the processor mode. Connect to V_{SS} for single-chip mode, and to V_{CC} for external ROM types.
$\overline{RESET}$	Reset input	Input	To enter the reset state, this pin must be kept at a "L" condition which should be maintained for the required time.
X_{IN}	Clock input	Input	These are I/O pins of internal clock generating circuit. Connect a ceramic or quartz crystal resonator between X_{IN} and X_{OUT}. When an external clock is used, the clock source should be connected to the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Data or instruction read and data write are performed when output from this pin is "L".
BYTE	Bus width selection input	Input	In memory expansion mode or microprocessor mode, this pin determines whether the external data bus is 8-bit width or 16-bit width. The width is 16 bits when "L" signal inputs and 8 bits when "H" signal inputs.
AV_{CC} AV_{SS}	Analog supply input		Power supply for the A-D converter. AV_{SS} is also used for D-A converter. Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS} externally.
V_{REF}	Reference voltage input	Input	This is reference voltage input pin for the A-D converter and the D-A converter.
$P0_0$~$P0_7$	I/O port P0	I/O	In single-chip mode, port P0 becomes an 8-bit I/O port. An I/O direction register is available so that each pin can be programmed for input or output. These ports are in input mode when reset . Address(A_7~A_0)is output in memory expansion mode or microprocessor mode.
$P1_0$~$P1_7$	I/O port P1	I/O	In single-chip mode, these pins have the same functions as port P0. When the BYTE pin is set to "L" in memory expansion mode or microprocessor mode and external data bus is 16-bit width, high-order data (D_{15}~D_8)is input or output when $\overline{E}$ output is "L" and an address (A_{15}~A_8) is output when $\overline{E}$ output is "H". If the BYTE pin is "H" that is an external data bus is 8-bit width, only address(A_{15}~A_8)is output.
$P2_0$~$P2_7$	I/O port P2	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode low-order data(D_7~D_0) is input or output when $\overline{E}$ output is "L" and an address(A_{23}~A_{16})is output when $\overline{E}$ output is "H".
$P3_0$~$P3_3$	I/O port P3	I/O	In single-chip mode , these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, R/$\overline{W}$, $\overline{BHE}$, ALE, and $\overline{HLDA}$ signals are output.
$P4_0$~$P4_7$	I/O port P4	I/O	In single-chip mode, these pins have the same functions as port P0. In memory expansion mode or microprocessor mode, $P4_0$ and $P4_1$ become $\overline{HOLD}$ and $\overline{RDY}$ input pin respectively. Functions of other pins are the same as in single-chip mode. In single-chip mode or memory expansion mode, port $P4_2$ can be programmed for ϕ_1 output pin divided the clock to X_{IN} pin by 2. In microprocessor mode, $P4_2$ always has the function as ϕ_1 output pin.
$P5_0$~$P5_7$	I/O port P5	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A0, timer A1, timer A2 and timer A3. $P5_0$~$P5_6$ also function as output pins for pulse motor drive waveform.
$P6_0$~$P6_7$	I/O port P6	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as I/O pins for timer A4, external interrupt input $\overline{INT_0}$, $\overline{INT_1}$ and $\overline{INT_2}$ pins, and input pins for timer B0, timer B1 and timer B2. $P6_0$ also functions as an output pin for pulse motor drive waveform.
$P7_0$~$P7_7$	I/O port P7	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as analog input AN_0~AN_7 input pins. $P7_7$ also has an A-D conversion trigger input function.
$P8_0$~$P8_7$	I/O port P8	I/O	In addition to having the same functions as port P0 in single-chip mode, these pins also function as R_XD, T_XD, CLK, $\overline{CTS}$/$\overline{RTS}$ pins for UART 0 and UART 1, and output pins for D-A converter.

PRELIMINARY
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PIN DESCRIPTION (EPROM MODE)

Pin	Name	Input/Output	Functions
V_{CC}, V_{SS}	Power supply		Supply 5 V±10% to V_{CC} and 0 V to V_{SS}.
CNV_{SS}	V_{PP} input	Input	Connect to V_{PP} when programming or verifing.
BYTE	V_{PP} Input	Input	Connect to V_{PP} when programming or verifing.
$\overline{RESET}$	Reset input	Input	Connect to V_{SS}.
X_{IN}	Clock input	Input	Connect a ceramic resonator between X_{IN} and X_{OUT}.
X_{OUT}	Clock output	Output	
$\overline{E}$	Enable output	Output	Keep open.
AV_{CC}, AV_{SS}	Analog supply input		Connect AV_{CC} to V_{CC} and AV_{SS} to V_{SS}.
V_{REF}	Reference voltage input	Input	Connect to V_{SS}.
$P0_0$~$P0_7$	Address input (A_0~A_7)	Input	Port P0 functions as the low-order 8 bits address input (A_0~A_7).
$P1_0$~$P1_7$	Address input (A_8~A_{15})	Input	Port P1 functions as the middle-order 8 bits address input (A_8~A_{15}).
$P2_0$~$P2_7$	Data I/O (D_0~D_7)	I/O	Port P2 functions as the 8 bits data bus (D_0~D_7).
$P3_0$	Address input (A_{16})	Input	$P3_0$ functions as the most significant bit of address input (A_{16}).
$P3_1$~$P3_3$	Input port P3	Input	Connect to V_{SS}.
$P4_0$~$P4_7$	Input port P4	Input	Connect to V_{SS}.
$P5_0$~$P5_7$	Control signal input	Input	$P5_0$, $P5_1$ and $P5_2$ function as $\overline{PGM}$, $\overline{OE}$ and $\overline{CE}$ input pins respectively. Connect $P5_3$, $P5_4$, $P5_5$ and $P5_6$ to V_{CC}. Connect $P5_7$ to V_{SS}.
$P6_0$~$P6_7$	Input port P6	Input	Connect to V_{SS}.
$P7_0$~$P7_7$	Input port P7	Input	Connect to V_{SS}.
$P8_0$~$P8_7$	Input port P8	Input	Connect to V_{SS}.

M37710EFBXXXFP
M37710EFBFS

PRELIMINARY
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PROM VERSION of M37710MFBXXXFP

BASIC FUNCTION BLOCKS

The M37710EFBXXXFP has the same functions as the M37710M4BXXXFP except for the following:

(1) The built-in ROM is PROM.
(2) The ROM size is 120K bytes
(3) The RAM size is 2048 bytes
(4) The processor mode is different.
(5) The reset circuit is different.

Therefore, refer to the section on the M37710M4BXXXFP.

MEMORY

The memory map is shown in Figure 1.

PROCESSOR MODE

Bit 4 of processor mode register 1 (address $5F_{16}$) must be "0". Except for this bit, the processor mode has the same functions as those of the M37710M4BXXXFP's processor mode.

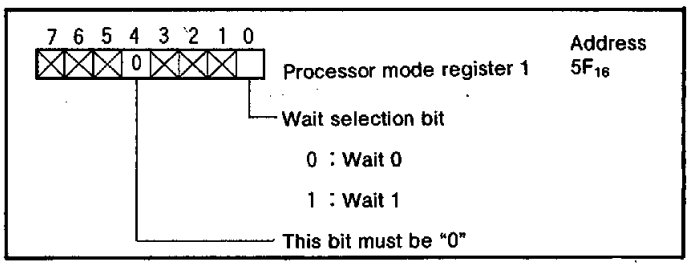

Fig. 2 Processor mode register 1 bit configulation

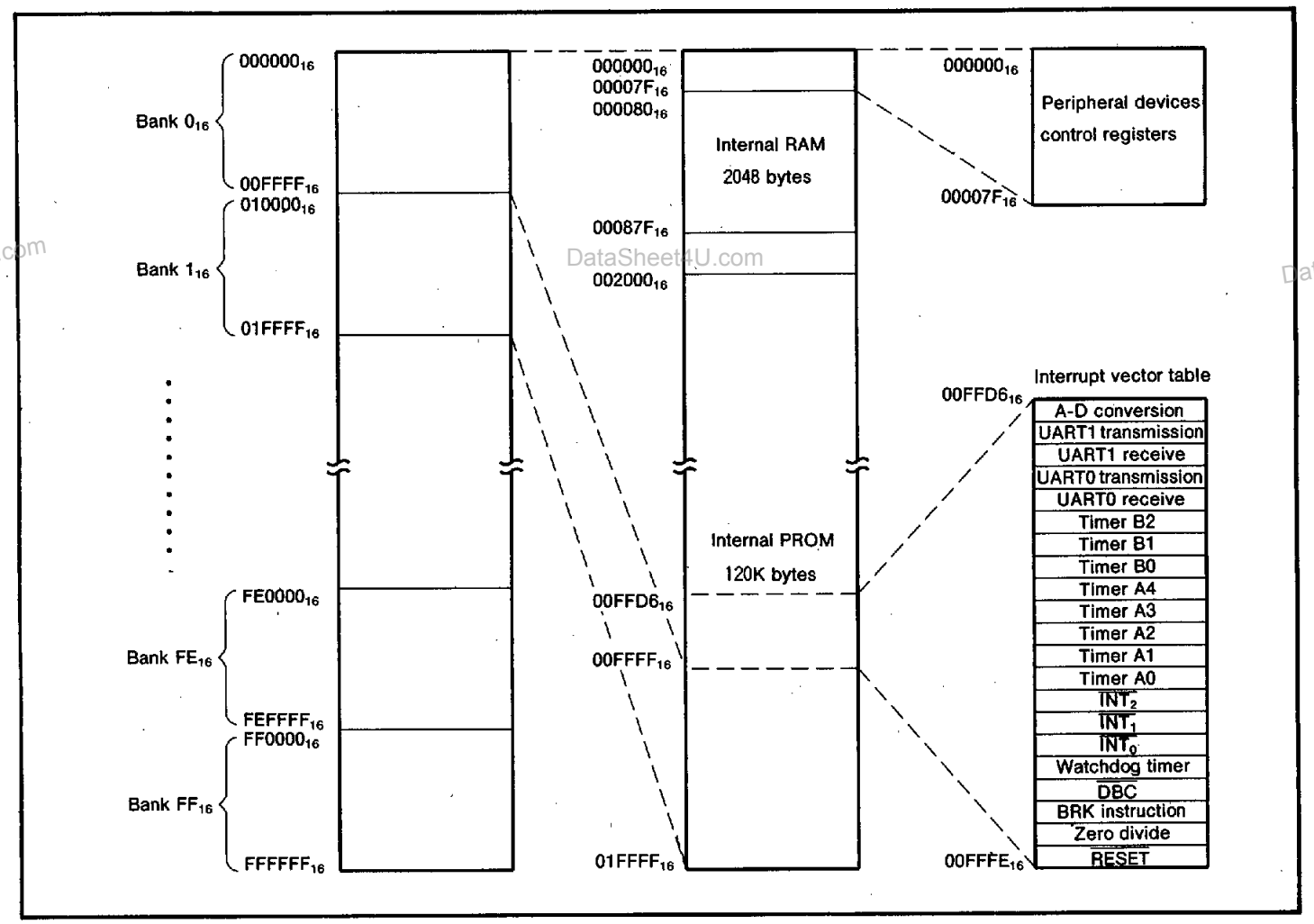

Fig. 1 Memory map

PRELIMINARY
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RESET CIRCUIT

Figure 3 shows the status of the internal registers when a reset occurs. Except for the status of processor mode register 1 when a reset occurs, the reset circuit has the same functions as those of the M37710M4BXXXFP's reset circuit.

		Address	
(1)	Port P0 data direction register	(04_{16})···	00_{16}
(2)	Port P1 data direction register	(05_{16})···	00_{16}
(3)	Port P2 data direction register	(08_{16})···	00_{16}
(4)	Port P3 data direction register	(09_{16})···	X X X X 0 0 0 0
(5)	Port P4 data direction register	($0C_{16}$)···	00_{16}
(6)	Port P5 data direction register	($0D_{16}$)···	00_{16}
(7)	Port P6 data direction register	(10_{16})···	00_{16}
(8)	Port P7 data direction register	(11_{16})···	00_{16}
(9)	Port P8 data direction register	(14_{16})···	00_{16}
(10)	A-D control register 0	($1E_{16}$)···	0 0 0 0 0 ? ? ?
(11)	A-D control register 1	($1F_{16}$)···	0 0 X 0 0 0 1 1
(12)	UART 0 Transmit/Receive mode register	(30_{16})···	00_{16}
(13)	UART 1 Transmit/Receive mode register	(38_{16})···	00_{16}
(14)	UART 0 Transmit/Receive control register 0	(34_{16})···	X X X 0 1 0 0 0
(15)	UART 1 Transmit/Receive control register 0	($3C_{16}$)···	X X X 0 1 0 0 0
(16)	UART 0 Transmit/Receive control register 1	(35_{16})···	0 0 0 0 0 0 1 0
(17)	UART 1 Transmit/Receive control register 1	($3D_{16}$)···	0 0 0 0 0 0 1 0
(18)	Count start flag	(40_{16})···	00_{16}
(19)	One-shot start flag	(42_{16})···	X X X 0 0 0 0 0
(20)	Up-down flag	(44_{16})···	00_{16}
(21)	Timer A0 mode register	(56_{16})···	00_{16}
(22)	Timer A1 mode register	(57_{16})···	00_{16}
(23)	Timer A2 mode register	(58_{16})···	00_{16}
(24)	Timer A3 mode register	(59_{16})···	00_{16}
(25)	Timer A4 mode register	($5A_{16}$)···	00_{16}
(26)	Timer B0 mode register	($5B_{16}$)···	0 0 1 0 0 0 0 0
(27)	Timer B1 mode register	($5C_{16}$)···	0 0 1 X 0 0 0 0
(28)	Timer B2 mode register	($5D_{16}$)···	0 0 1 X 0 0 0 0

		Address	
(29)	Processor mode register 0	($5E_{16}$)···	00_{16}
(30)	Processor mode register 1	($5F_{16}$)···	X X X 0 X X X 0
(31)	Watchdog timer	(60_{16})···	FFF_{16}
(32)	Watchdog timer frequency selection flag	(61_{16})···	X X X X X X X 0
(33)	Waveform output mode register	(62_{16})···	00_{16}
(34)	Reserved area (Do not write to this address)	(66_{16})···	00_{16}
(35)	A-D conversion interrupt control register	(70_{16})···	X X X X 0 0 0 0
(36)	UART 0 transmission interrupt control register	(71_{16})···	X X X X 0 0 0 0
(37)	UART 0 receive interrupt control register	(72_{16})···	X X X X 0 0 0 0
(38)	UART 1 transmission interrupt control register	(73_{16})···	X X X X 0 0 0 0
(39)	UART 1 receive interrupt control register	(74_{16})···	X X X X 0 0 0 0
(40)	Timer A0 interrupt control register	(75_{16})···	X X X X 0 0 0 0
(41)	Timer A1 interrupt control register	(76_{16})···	X X X X 0 0 0 0
(42)	Timer A2 interrupt control register	(77_{16})···	X X X X 0 0 0 0
(43)	Timer A3 interrupt control register	(78_{16})···	X X X X 0 0 0 0
(44)	Timer A4 interrupt control register	(79_{16})···	X X X X 0 0 0 0
(45)	Timer B0 interrupt control register	($7A_{16}$)···	X X X X 0 0 0 0
(46)	Timer B1 interrupt control register	($7B_{16}$)···	X X X X 0 0 0 0
(47)	Timer B2 interrupt control register	($7C_{16}$)···	X X X X 0 0 0 0
(48)	$\overline{INT}_0$ interrupt control register	($7D_{16}$)···	X X 0 0 0 0 0 0
(49)	$\overline{INT}_1$ interrupt control register	($7E_{16}$)···	X X 0 0 0 0 0 0
(50)	$\overline{INT}_2$ interrupt control register	($7F_{16}$)···	X X 0 0 0 0 0 0
(51)	Processor status register PS		0 0 0 ? ? 0 0 0 1 ? ?
(52)	Program bank register PG		00_{16}
(53)	Program counter PC_H		Content of $FFFF_{16}$
(54)	Program counter PC_L		Content of $FFFE_{16}$
(55)	Direct page register DPR		0000_{16}
(56)	Data bank register DT		00_{16}

Contents of other registers and RAM are not initialized and should be initialized by software.

Fig. 3 Microcomputer internal status during reset

PRELIMINARY
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EPROM MODE

The M37710EFBXXXFP features an EPROM mode in addition to its normal modes. When the RESET signal level is "L", the chip automatically enters the EPROM mode. Table 1 list the correspondence between pins and Figure 4 shows the pin connections in the EPROM mode.

The EPROM mode is the 1M mode for the EPROM that is equivalent to the M5M27C101K.

When in the EPROM mode, ports P0, P1, P2, $P3_0$, $P5_0$, $P5_1$, $P5_2$, CNV_{SS} and BYTE are used for the EPROM (equivalent to the M5M27C101K). When in this mode, the built-in PROM can be written to or read from using these pins in the same way as with the M5M27C101K.

This chip does not have Device Identifier Mode, so that set the corresponding program algorithm. The program area should specify address 02000_{16}~$1FFFF_{16}$.

Connect the clock which is either ceramic resonator or external clock to X_{IN} pin and X_{OUT} pin.

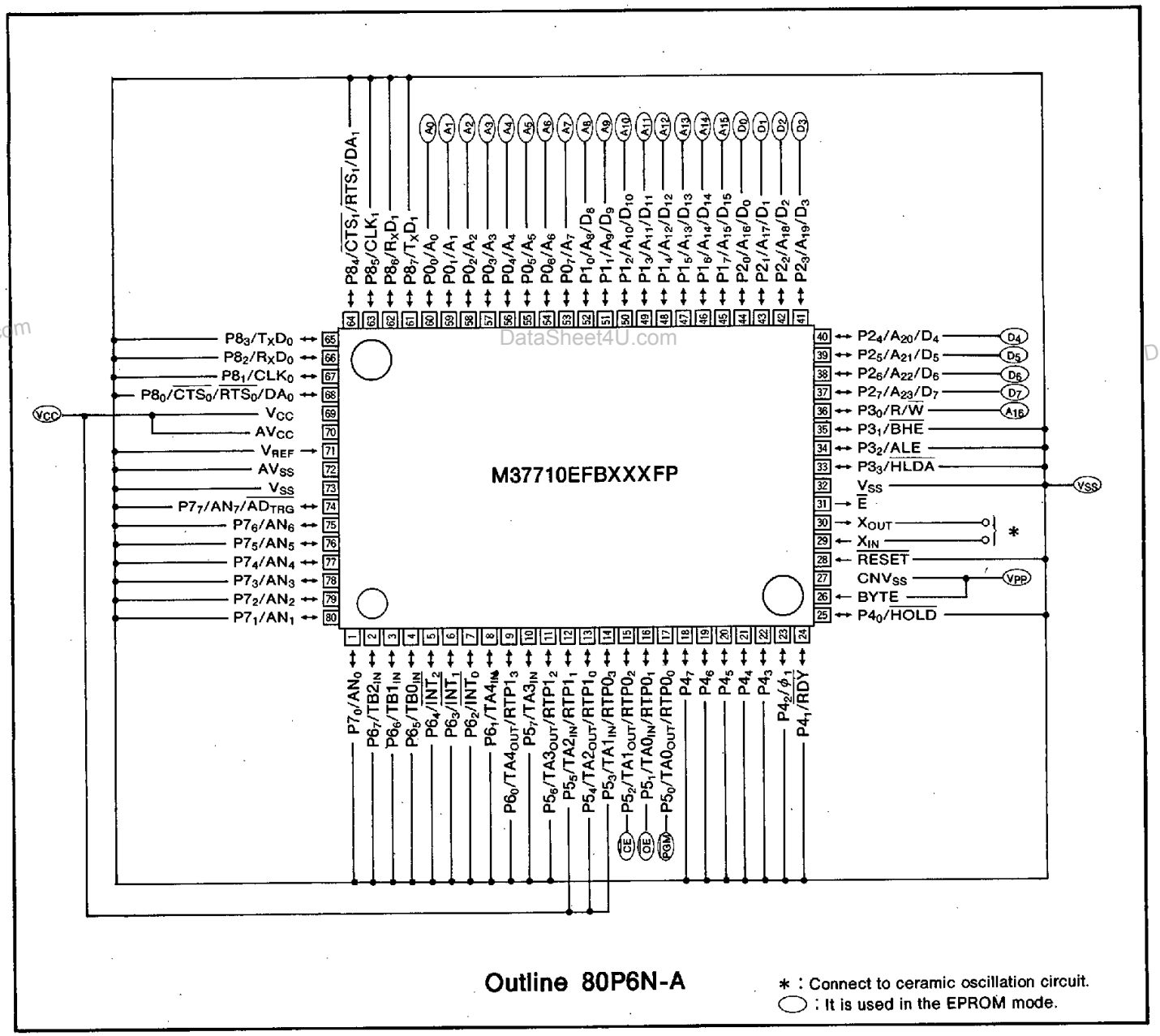

Fig. 4 Pin connection in EPROM mode

PRELIMINARY
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Table 1 Pin function in EPROM mode

	M37710EFBXXXFP	M5M27C101K
V_{CC}	V_{CC}	V_{CC}
V_{PP}	CNV_{SS}, BYTE	V_{PP}
V_{SS}	V_{SS}	V_{SS}
Address input	Ports P0, P1, $P3_0$	A_0~A_{16}
Data I/O	Port P2	D_0~D_7
$\overline{CE}$	$P5_2$	$\overline{CE}$
$\overline{OE}$	$P5_1$	$\overline{OE}$
$\overline{PGM}$	$P5_0$	$\overline{PGM}$

PRELIMINARY
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FUNCTION IN EPROM MODE 1M mode (equivalent to the M5M27C101K)

Reading

To read the EPROM, set the $\overline{CE}$ and $\overline{OE}$ pins to a "L" level. Input the address of the data (A_0~A_{16}) to be read, and the data will be output to the I/O pins D_0~D_7. The data I/O pins will be floating when either the $\overline{CE}$ or $\overline{OE}$ pins are in the "H" state.

Writing

Writing must be performed in 8 bits by a byte program. To write to the EPROM, set the $\overline{CE}$ pin to a "L" level and the $\overline{OE}$ pin to a "H" level. The CPU will enter the program mode when 12.5V is applied to the V_{PP} pin. The address to be written to is selected with pins A_0~A_{16}, and the data to be written is input to pins D_0~D_7. Set the $\overline{PGM}$ pin to a "L" level to being writing.

Erasing

To erase data on this chip, use an ultraviolet light source with a 2537 Angstrom wave length. The minimum radiation power necessary for erasing is 15 W·s/cm^2.

Writing operation

To program the M37710EFBXXXFP, first set V_{CC}=6V, V_{PP}=12.5V, and set the address to 02000_{16}. Apply a 0.2ms write pulse, check that the data can be read, and if it cannot be read OK, repeat the procedure, applying a 0.2ms write pulse and checking that the data can be read until it can be read OK. Record the accumulated number of pulse applied (X) before the data can be read OK, and then write the data again, applying a further once this number of pulses (0.2× X ms).

When this series of write operations is complete, increment the address, and continue to repeat the procedure above until the last address has been reached.

Finally, when all addresses have been written, read with V_{CC}=V_{PP}=5V(or V_{CC}=V_{PP}=5.5V).

Table 2. I/O signal in each mode

Mode \ Pin	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	V_{PP}	V_{CC}	Data I/O
Read-out	V_{IL}	V_{IL}	X	5 V	5 V	Output
Output Disable	V_{IL}	V_{IH}	X	5 V	5 V	Floating
	V_{IH}	X	X	5 V	5 V	Floating
Programming	V_{IL}	V_{IH}	V_{IL}	12.5V	6 V	Input
Programming Verify	V_{IL}	V_{IL}	V_{IH}	12.5V	6 V	Output
Program Disable	V_{IH}	V_{IH}	V_{IH}	12.5V	6 V	Floating

Note. An X indicates either V_{IL} or V_{IH}.

Program operation (equivalent to the M5M27C101K)

AC ELECTRICAL CHARACTERISTICS (T_a=25±5℃, V_{CC}=6V±0.25V, V_{PP}=12.5±0.3V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{AS}	Address setup time		2			μs
t_{OES}	$\overline{OE}$ setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{DFP}	Output enable to output float delay		0		130	ns
t_{VCS}	V_{CC} setup time		2			μs
t_{VPS}	V_{PP} setup time		2			μs
t_{PW}	$\overline{PGM}$ pulse width		0.19	0.2	0.21	ms
t_{OPW}	$\overline{PGM}$ over program pulse width		0.19		5.25	ms
t_{CES}	$\overline{CE}$ setup time		2			μs
t_{OE}	Data valid from $\overline{OE}$				150	ns

PRELIMINARY
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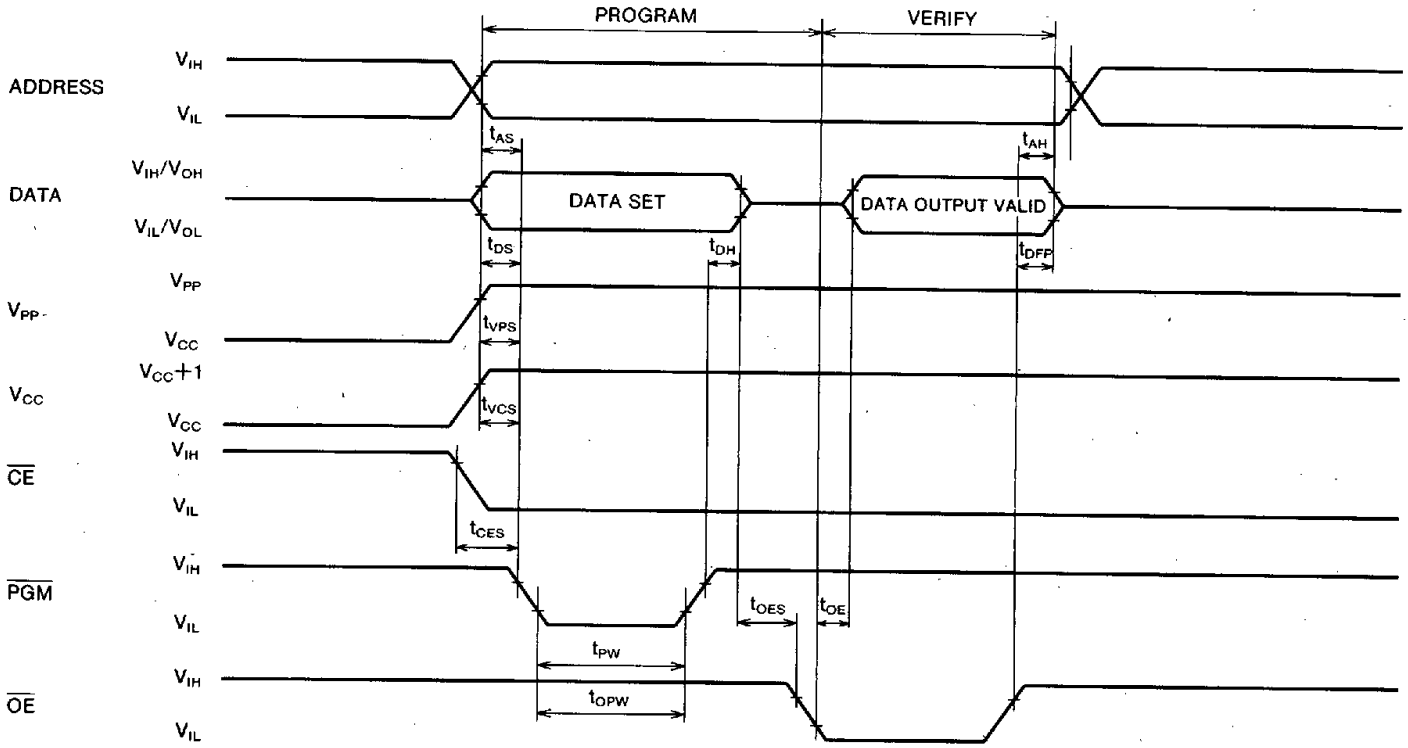
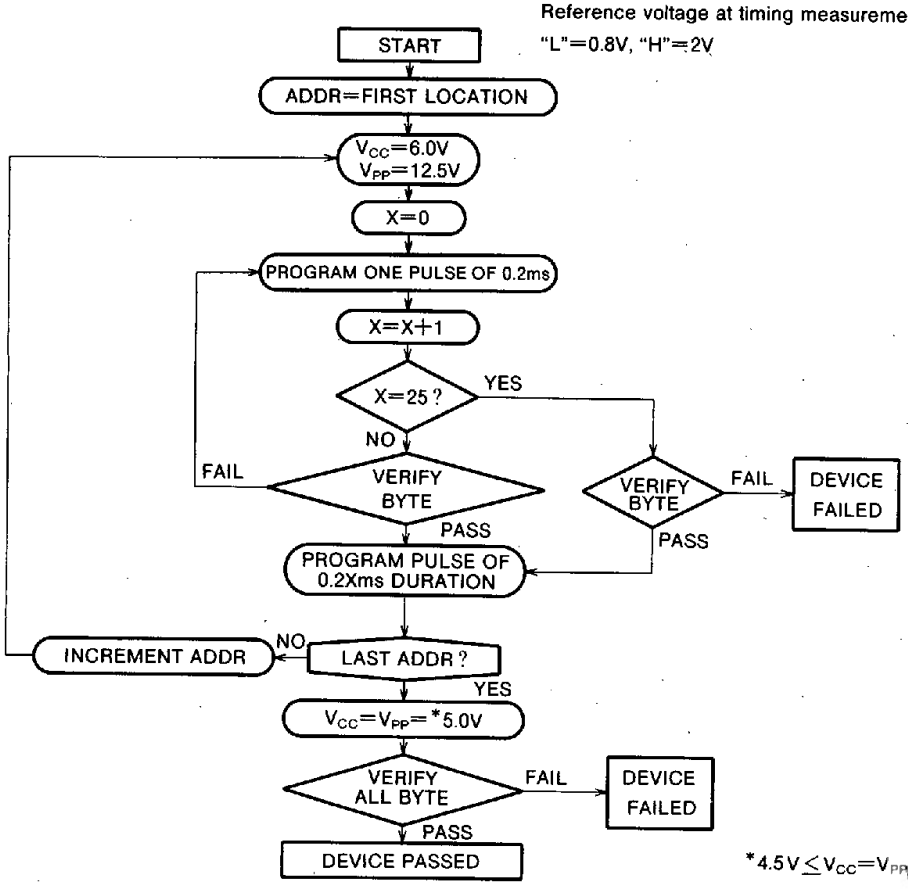
AC waveforms



Test conditions for A.C. characteristics
Input voltage : V_{IL}=0.45V, V_{IH}=2.4V
Input rise and fall times (10%~90%) : ≤20ns
Reference voltage at timing measurement : Input, Output "L"=0.8V, "H"=2V

Programming algorithm flow chart



*4.5V≤V_{CC}=V_{PP}≤5.5V

M37710EFBXXXFP
M37710EFBFS

PRELIMINARY
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PROM VERSION of M37710MFBXXXFP

SAFETY INSTRUCTIONS

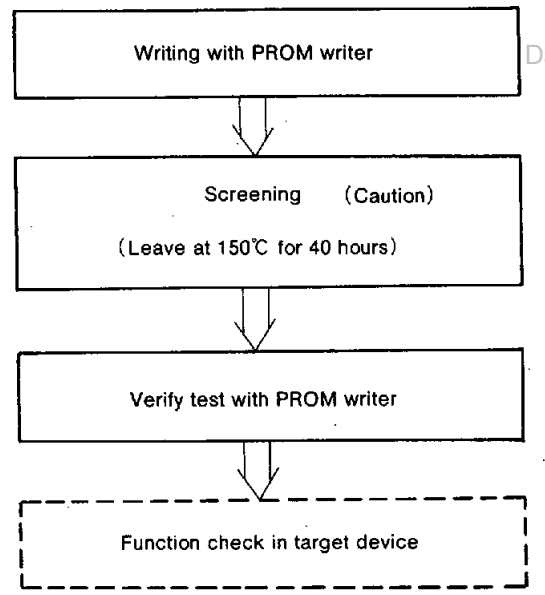
(1) Sunlight and fluorescent lamp contain light that can erase written information. When using in read mode, be sure to cover the transparent glass portion with a seal or other materials (ceramic package product).

(2) Mitsubishi Electric corp. provides the seal for covering the transparent glass. Take care that the seal does not touch the read pins (ceramic package product).

(3) Clean the transparent glass before erasing. Fingers' fat and paste disturb the passage of ultraviolet rays and may affect badly the erasure capability (ceramic package product).

(4) A high voltage is used for writing. Take care that over-voltage is not applied. Take care especially at power on.

(5) The programmable M37710EFBFP that is shipped in blank is also provided. For the M37710EFBFP, Mitsubishi Electric corp. does not perform PROM write test and screening following the assembly processes. To improve reliability after write, performing write and test according to the flow below before use is recommended.



Caution : Never expose to 150 ℃ exceeding 100 hours.

ADDRESSING MODES

The M37710EFBXXXFP has 28 powerful addressing modes. Refer to the 7700 Family addressing mode description for the details of each addressing mode.

MACHINE INSTRUCTION LIST

The M37710EFBXXXFP has 103 machine instructions. Refer to the 7700 Family machine instruction list for details.

DATA REQUIRED FOR PROM ORDERING

Please send the following data for writing to PROM.

(1) M37710EFBXXXFP writing to PROM order confirmation form

(2) 80P6N mark specification form

(3) ROM data (EPROM 3 sets)

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.3∼7	V
AV_{CC}	Analog supply voltage		−0.3∼7	V
V_I	Input voltage $\overline{RESET}$, CNV_{SS}, BYTE		−0.3∼12(Note 1)	V
V_I	Input voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$, V_{REF}, X_{IN}		−0.3∼V_{CC}+0.3	V
V_O	Output voltage $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$, X_{OUT}, $\overline{E}$		−0.3∼V_{CC}+0.3	V
P_d	Power dissipation	T_a=25℃	300	mW
T_{opr}	Operating temperature		−20∼85	℃
T_{stg}	Storage temperature		−40∼150	℃

Note 1. Input voltage for CNV_{SS} and BYTE pins is 13V in writing to PROM.

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=−20∼85℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
AV_{CC}	Analog supply voltage		V_{CC}		V
V_{SS}	Supply voltage		0		V
AV_{SS}	Analog supply voltage		0		V
V_{IH}	High-level input voltage $P0_0$∼$P0_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in single-chip mode)	0.8V_{CC}		V_{CC}	V
V_{IH}	High-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in memory expansion mode and microprocessor mode)	0.5V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage $P0_0$∼$P0_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in single-chip mode)	0		0.2V_{CC}	V
V_{IL}	Low-level input voltage $P1_0$∼$P1_7$, $P2_0$∼$P2_7$ (in memory expansion mode and microprocessor mode)	0		0.16V_{CC}	V
$I_{OH(peak)}$	High-level peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$			−10	mA
$I_{OH(avg)}$	High-level average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$			−5	mA
$I_{OL(peak)}$	Low-level peak output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$			10	mA
$I_{OL(avg)}$	Low-level average output current $P0_0$∼$P0_7$, $P1_0$∼$P1_7$, $P2_0$∼$P2_7$, $P3_0$∼$P3_3$, $P4_0$∼$P4_7$, $P5_0$∼$P5_7$, $P6_0$∼$P6_7$, $P7_0$∼$P7_7$, $P8_0$∼$P8_7$			5	mA
$f(X_{IN})$	External clock frequency input			25	MHz

Note 2. Average output current is the average value of a 100ms interval.
3. The sum of $I_{OL(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of $I_{OH(peak)}$ for ports P0, P1, P2, P3, and P8 must be 80mA or less, the sum of $I_{OL(peak)}$ for ports P4, P5, P6, and P7 must be 80mA or less, and the sum of $I_{OH(peak)}$ for ports P4, P5, P6, and P7 must be 80mA or less.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

ELECTRICAL CHARACTERISTICS (V_{CC}=5V, V_{SS}=0V, T_a=25℃, f(X_{IN})=25MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
V_{OH}	High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$	I_{OH}=−10mA	3			V
V_{OH}	High-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OH}=−400μA	4.7			V
V_{OH}	High-level output voltage $P3_2$	I_{OH}=−10mA	3.1			V
		I_{OH}=−400μA	4.8			
V_{OH}	High-level output voltage $\overline{E}$	I_{OH}=−10mA	3.4			V
		I_{OH}=−400μA	4.8			
V_{OL}	Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P3_3$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$	I_{OL}=10mA			2	V
V_{OL}	Low-level output voltage $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$, $P3_1$, $P3_3$	I_{OL}=2mA			0.45	V
V_{OL}	Low-level output voltage $P3_2$	I_{OL}=10mA			1.9	V
		I_{OL}=2mA			0.43	
V_{OL}	Low-level output voltage $\overline{E}$	I_{OL}=10mA			1.6	V
		I_{OL}=2mA			0.4	
V_{T+}−V_{T-}	Hysteresis $\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$~$TA4_{IN}$, $TB0_{IN}$~$TB2_{IN}$, $\overline{INT_0}$~$\overline{INT_2}$, $\overline{AD_{TRG}}$, $\overline{CTS_0}$, $\overline{CTS_1}$, CLK_0, CLK_1		0.4		1	V
V_{T+}−V_{T-}	Hysteresis $\overline{RESET}$		0.2		0.5	V
V_{T+}−V_{T-}	Hysteresis X_{IN}		0.1		0.3	V
I_{IH}	High-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_3$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5	μA
I_{IL}	Low-level input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_3$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $P7_0$~$P7_7$, $P8_0$~$P8_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			−5	μA
V_{RAM}	RAM hold voltage	When clock is stopped.	2			V
I_{CC}	Power supply current	In single-chip mode output only pin is open and other pins are V_{SS} during reset. f(X_{IN})=25MHz, square waveform		19	38	mA
		T_a=25℃ when clock is stopped.			1	μA
		T_a=85℃ when clock is stopped.			20	

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

A-D CONVERTER CHARACTERISTICS (V_{CC}=AV_{CC}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=25MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution	V_{REF}=V_{CC}			10	Bits
—	Absolute accuracy	V_{REF}=V_{CC}			±3	LSB
R_{LADDER}	Ladder resistance	V_{REF}=V_{CC}	5		20	kΩ
t_{CONV}	Conversion time		4.72			μs
V_{REF}	Reference voltage		2		V_{CC}	V
V_{IA}	Analog input voltage		0		V_{REF}	V

D-A CONVERTER CHARACTERISTICS (V_{CC}=V_{REF}=5V, V_{SS}=AV_{SS}=0V, T_a=25℃, f(X_{IN})=25MHz, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
—	Resolution				8	Bits
—	Absolute accuracy				±1.0	%
t_{SU}	Set time				3	μs
R_O	Output resistance		1	2.5	4	kΩ
I_{VREF}	Reference power input current	(Note)			3.2	mA

Note. One D-A converter is used, and the value of D-A register for unused D-A converter is "00_{16}".
Current that flows to the ladder resistance of A-D converter is excluded.

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

TIMING REQUIREMENTS (V_{CC}=5V±10%, V_{SS}=0V, T_a=25°C, f(X_{IN})=25MHz, unless otherwise noted)

External clock input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
t_C	External clock input cycle time	40		ns
$t_{W(H)}$	External clock input high-level pulse width	15		ns
$t_{W(L)}$	External clock input low-level pulse width	15		ns
t_r	External clock rise time		8	ns
t_f	External clock fall time		8	ns

Single-chip mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{SU(P0D-E)}$	Port P0 input setup time	60		ns
$t_{SU(P1D-E)}$	Port P1 input setup time	60		ns
$t_{SU(P2D-E)}$	Port P2 input setup time	60		ns
$t_{SU(P3D-E)}$	Port P3 input setup time	60		ns
$t_{SU(P4D-E)}$	Port P4 input setup time	60		ns
$t_{SU(P5D-E)}$	Port P5 input setup time	60		ns
$t_{SU(P6D-E)}$	Port P6 input setup time	60		ns
$t_{SU(P7D-E)}$	Port P7 input setup time	60		ns
$t_{SU(P8D-E)}$	Port P8 input setup time	60		ns
$t_{h(E-P0D)}$	Port P0 input hold time	0		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(E-P3D)}$	Port P3 input hold time	0		ns
$t_{h(E-P4D)}$	Port P4 input hold time	0		ns
$t_{h(E-P5D)}$	Port P5 input hold time	0		ns
$t_{h(E-P6D)}$	Port P6 input hold time	0		ns
$t_{h(E-P7D)}$	Port P7 input hold time	0		ns
$t_{h(E-P8D)}$	Port P8 input hold time	0		ns

Memory expansion mode and microprocessor mode

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{SU(P1D-E)}$	Port P1 input setup time	30		ns
$t_{SU(P2D-E)}$	Port P2 input setup time	30		ns
$t_{SU(RDY-\phi_1)}$	$\overline{RDY}$ input setup time	55		ns
$t_{SU(HOLD-\phi_1)}$	$\overline{HOLD}$ input setup time	55		ns
$t_{h(E-P1D)}$	Port P1 input hold time	0		ns
$t_{h(E-P2D)}$	Port P2 input hold time	0		ns
$t_{h(\phi_1-RDY)}$	$\overline{RDY}$ input hold time	0		ns
$t_{h(\phi_1-HOLD)}$	$\overline{HOLD}$ input hold time	0		ns

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Timer A input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time	80		ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width	40		ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width	40		ns

Timer A input (Gating input in timer mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time	320		ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width	160		ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width	160		ns

Timer A input (External trigger input in one-shot pulse mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TA)}$	TAi_{IN} input cycle time	160		ns
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width	80		ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width	80		ns

Timer A input (External trigger input in pulse width modulation mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAi_{IN} input high-level pulse width	80		ns
$t_{W(TAL)}$	TAi_{IN} input low-level pulse width	80		ns

Timer A input (Up-down input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(UP)}$	TAi_{OUT} input cycle time	2000		ns
$t_{W(UPH)}$	TAi_{OUT} input high-level pulse width	1000		ns
$t_{W(UPL)}$	TAi_{OUT} input low-level pulse width	1000		ns
$t_{SU(UP-T_{IN})}$	TAi_{OUT} input setup time	400		ns
$t_{h(T_{IN}-UP)}$	TAi_{OUT} input hold time	400		ns

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Timer B input (Count input in event counter mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time (one edge count)	80		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width (one edge count)	40		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width (one edge count)	40		ns
$t_{C(TB)}$	TBi_{IN} input cycle time (both edges count)	160		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width (both edges count)	80		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width (both edges count)	80		ns

Timer B input (Pulse period measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time	320		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width	160		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width	160		ns

Timer B input (Pulse width measurement mode)

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(TB)}$	TBi_{IN} input cycle time	320		ns
$t_{W(TBH)}$	TBi_{IN} input high-level pulse width	160		ns
$t_{W(TBL)}$	TBi_{IN} input low-level pulse width	160		ns

A-D trigger input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{AD_{TRG}}$ input cycle time (minimum allowable trigger)	1000		ns
$t_{W(ADL)}$	$\overline{AD_{TRG}}$ input low-level pulse width	125		ns

Serial I/O

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{C(CK)}$	CLK_i input cycle time	200		ns
$t_{W(CKH)}$	CLK_i input high-level pulse width	100		ns
$t_{W(CKL)}$	CLK_i input low-level pulse width	100		ns
$t_{d(C-Q)}$	TxD_i output delay time		80	ns
$t_{h(C-Q)}$	TxD_i hold time	0		ns
$t_{su(D-C)}$	RxD_i input setup time	30		ns
$t_{h(C-D)}$	RxD_i input hold time	90		ns

External interrupt $\overline{INT_i}$ input

Symbol	Parameter	Limits		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT_i}$ input high-level pulse width	250		ns
$t_{W(INL)}$	$\overline{INT_i}$ input low-level pulse width	250		ns

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, V_{SS}=0V, T_a=25℃, f(X_{IN})=25MHz, unless otherwise noted)

Single-chip mode

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(E-P0Q)}$	Port P0 data output delay time	Fig. 5		80	ns
$t_{d(E-P1Q)}$	Port P1 data output delay time			80	ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			80	ns
$t_{d(E-P3Q)}$	Port P3 data output delay time			80	ns
$t_{d(E-P4Q)}$	Port P4 data output delay time			80	ns
$t_{d(E-P5Q)}$	Port P5 data output delay time			80	ns
$t_{d(E-P6Q)}$	Port P6 data output delay time			80	ns
$t_{d(E-P7Q)}$	Port P7 data output delay time			80	ns
$t_{d(E-P8Q)}$	Port P8 data output delay time			80	ns

Memory expansion mode and microprocessor mode (when wait bit = "1")

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 5	12		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			45	ns
$t_{pXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		12		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		5		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			45	ns
$t_{pXZ(E-P2Z)}$	Port P2 floating start delay time			5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		12		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		5		ns
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time			50	ns
$t_{d(ALE-E)}$	ALE output delay time		4		ns
$t_{W(ALE)}$	ALE pulse width		22		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		20		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		20		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	18	ns
$t_{h(E-P0A)}$	Port P0 address hold time		25		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25		ns
$t_{pZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		25		ns
$t_{pZX(E-P2Z)}$	Port P2 floating release delay time		25		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		18		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		18		ns
$t_{W(EL)}$	$\overline{E}$ pulse width		50		ns

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

(when wait bit = "0", wait selection bit = "1", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 5	12		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			45	ns
$t_{pXZ(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		12		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		5		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			45	ns
$t_{pXZ(E-P2Z)}$	Port P2 floating start delay time			5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		12		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		5		ns
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time			50	ns
$t_{d(ALE-E)}$	ALE output delay time		4		ns
$t_{W(ALE)}$	ALE pulse width		22		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		20		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		20		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	18	ns
$t_{h(E-P0A)}$	Port P0 address hold time		25		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		9		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25		ns
$t_{pZX(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		9		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		25		ns
$t_{pZX(E-P2Z)}$	Port P2 floating release delay time		25		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		18		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		18		ns
$t_{W(EL)}$	$\overline{E}$ pulse width		130		ns

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

(when wait bit = "0", wait selection bit = "0", and external memory area is accessed)

Symbol	Parameter	Test conditions	Limits		Unit
			Min.	Max.	
$t_{d(P0A-E)}$	Port P0 address output delay time	Fig. 5	92		ns
$t_{d(E-P1Q)}$	Port P1 data output delay time (BYTE="L")			45	ns
$t_{pxz(E-P1Z)}$	Port P1 floating start delay time (BYTE="L")			5	ns
$t_{d(P1A-E)}$	Port P1 address output delay time		92		ns
$t_{d(P1A-ALE)}$	Port P1 address output delay time		70		ns
$t_{d(E-P2Q)}$	Port P2 data output delay time			45	ns
$t_{pxz(E-P2Z)}$	Port P2 floating start delay time			5	ns
$t_{d(P2A-E)}$	Port P2 address output delay time		92		ns
$t_{d(P2A-ALE)}$	Port P2 address output delay time		70		ns
$t_{d(\phi_1-HLDA)}$	$\overline{HLDA}$ output delay time			50	ns
$t_{d(ALE-E)}$	ALE output delay time		15		ns
$t_{w(ALE)}$	ALE pulse width		62		ns
$t_{d(BHE-E)}$	$\overline{BHE}$ output delay time		100		ns
$t_{d(R/W-E)}$	R/$\overline{W}$ output delay time		100		ns
$t_{d(E-\phi_1)}$	ϕ_1 output delay time		0	18	ns
$t_{h(E-P0A)}$	Port P0 address hold time		25		ns
$t_{h(ALE-P1A)}$	Port P1 address hold time (BYTE="L")		20		ns
$t_{h(E-P1Q)}$	Port P1 data hold time (BYTE="L")		25		ns
$t_{pzx(E-P1Z)}$	Port P1 floating release delay time (BYTE="L")		25		ns
$t_{h(E-P1A)}$	Port P1 address hold time (BYTE="H")		25		ns
$t_{h(ALE-P2A)}$	Port P2 address hold time		20		ns
$t_{h(E-P2Q)}$	Port P2 data hold time		25		ns
$t_{pzx(E-P2Z)}$	Port P2 floating release delay time		25		ns
$t_{h(E-BHE)}$	$\overline{BHE}$ hold time		18		ns
$t_{h(E-R/W)}$	R/$\overline{W}$ hold time		18		ns
$t_{w(EL)}$	$\overline{E}$ pulse width		130		ns

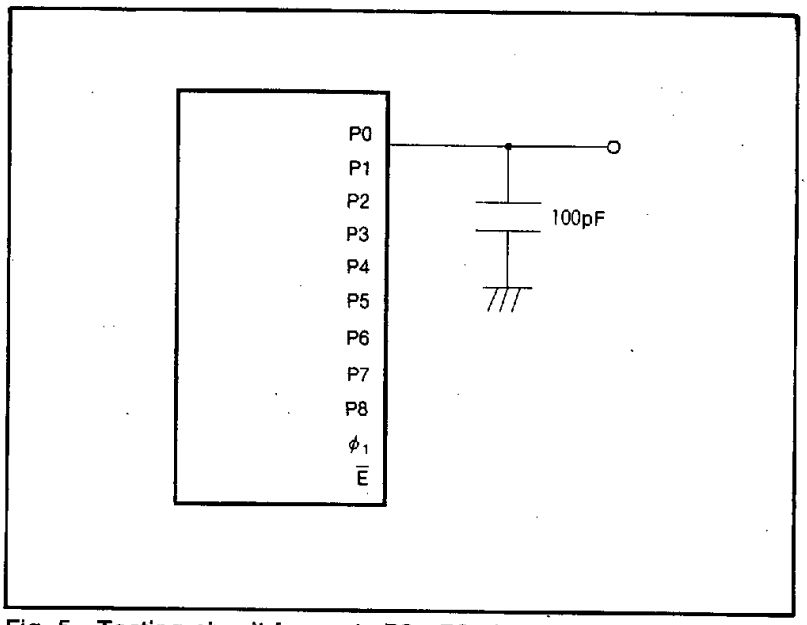
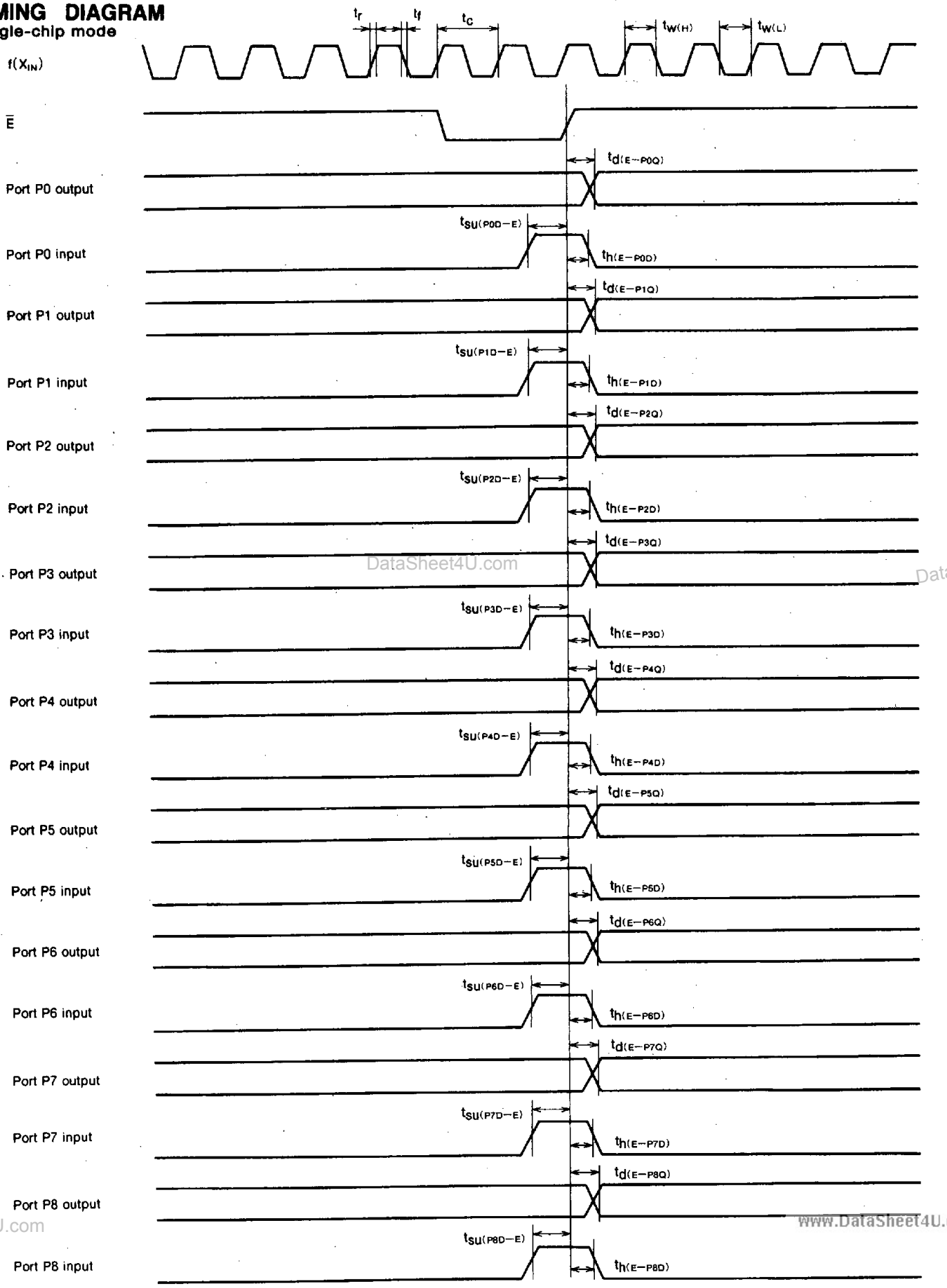


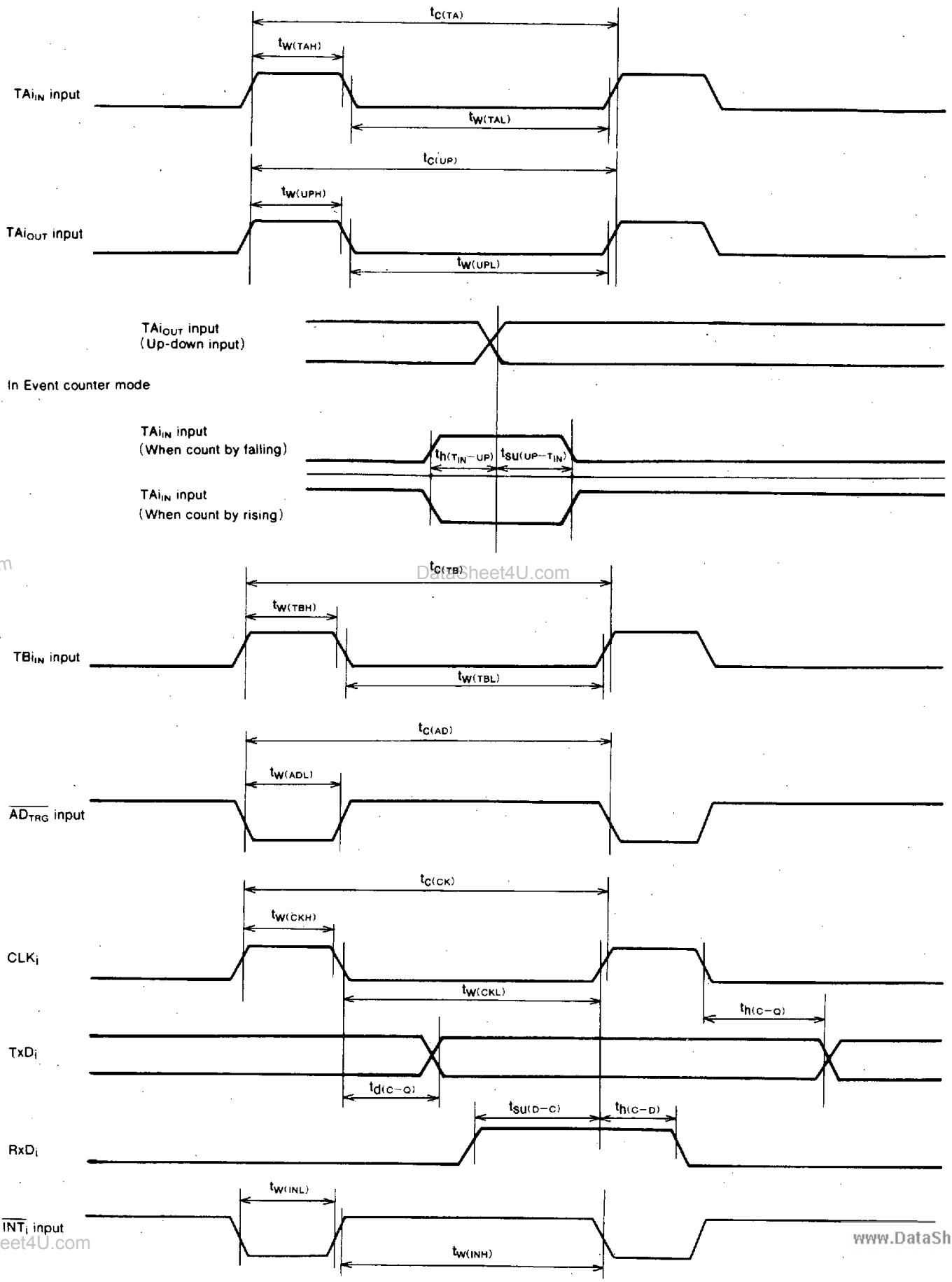
Fig. 5 Testing circuit for ports P0~P8, ϕ_1

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

TIMING DIAGRAM
Single-chip mode



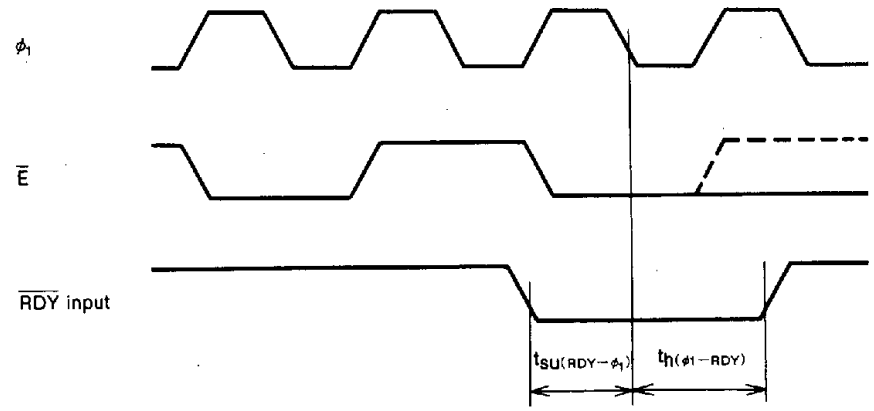
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.



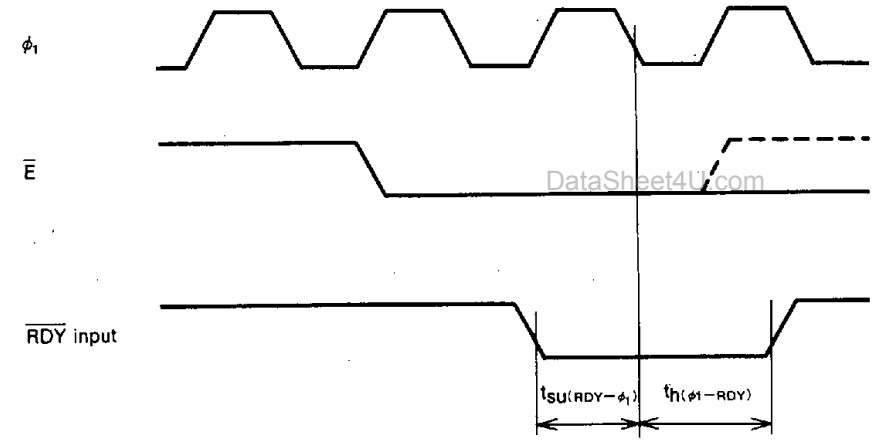
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

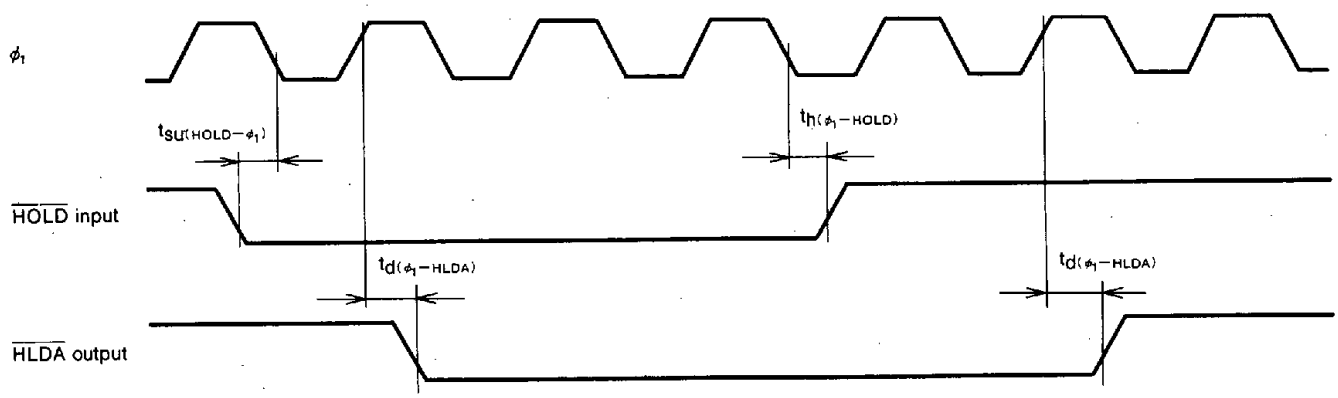
(When wait bit = "1")



(When wait bit = "0")



(When wait bit = "1" or "0" in common)

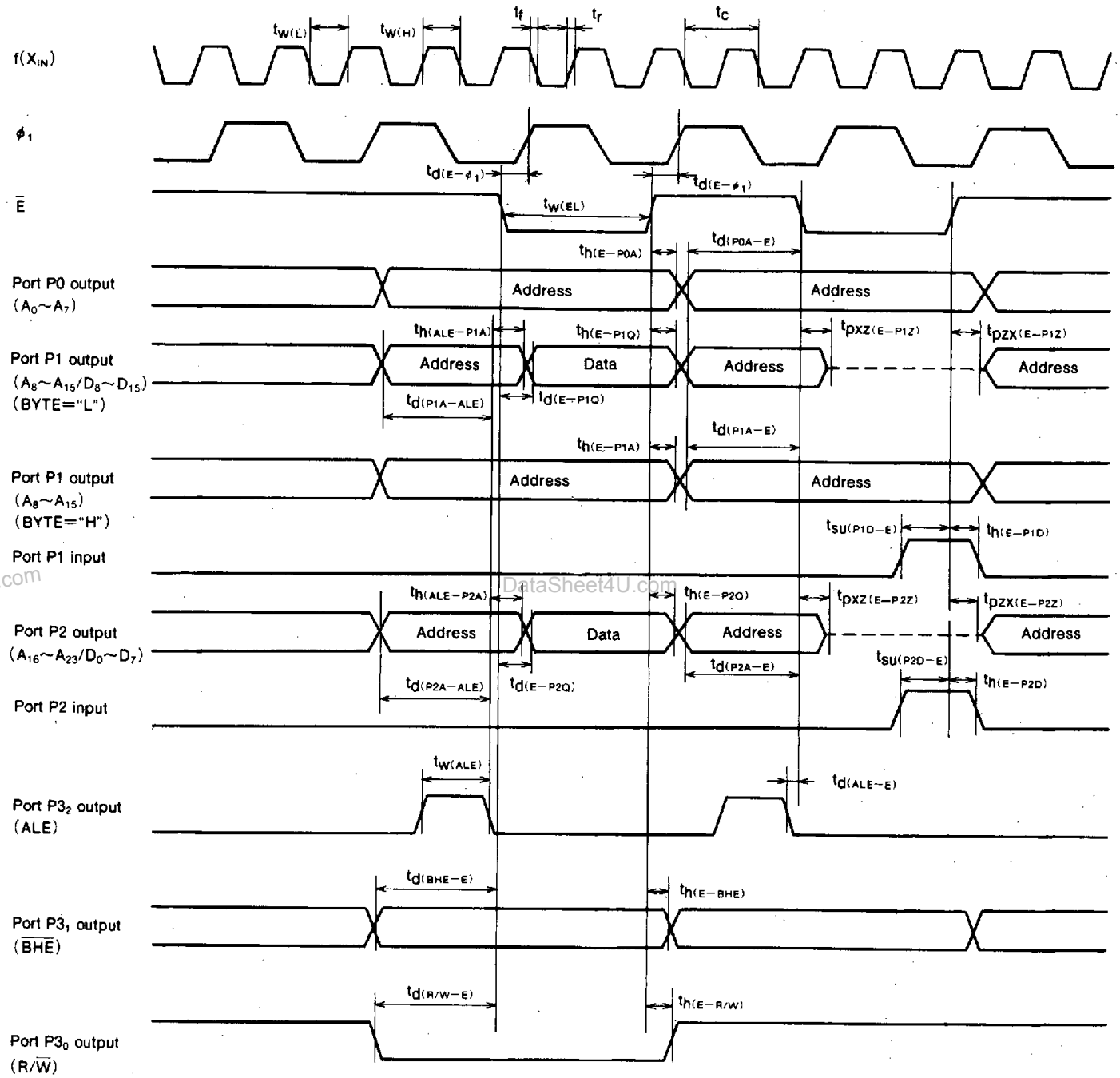


Test conditions

- V_{CC} = 5V±10%
- Input timing voltage : V_{IL} = 1.0V, V_{IH} = 4.0V
- Output timing voltage : V_{OL} = 0.8V, V_{OH} = 2.0V

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode (When wait bit="1")



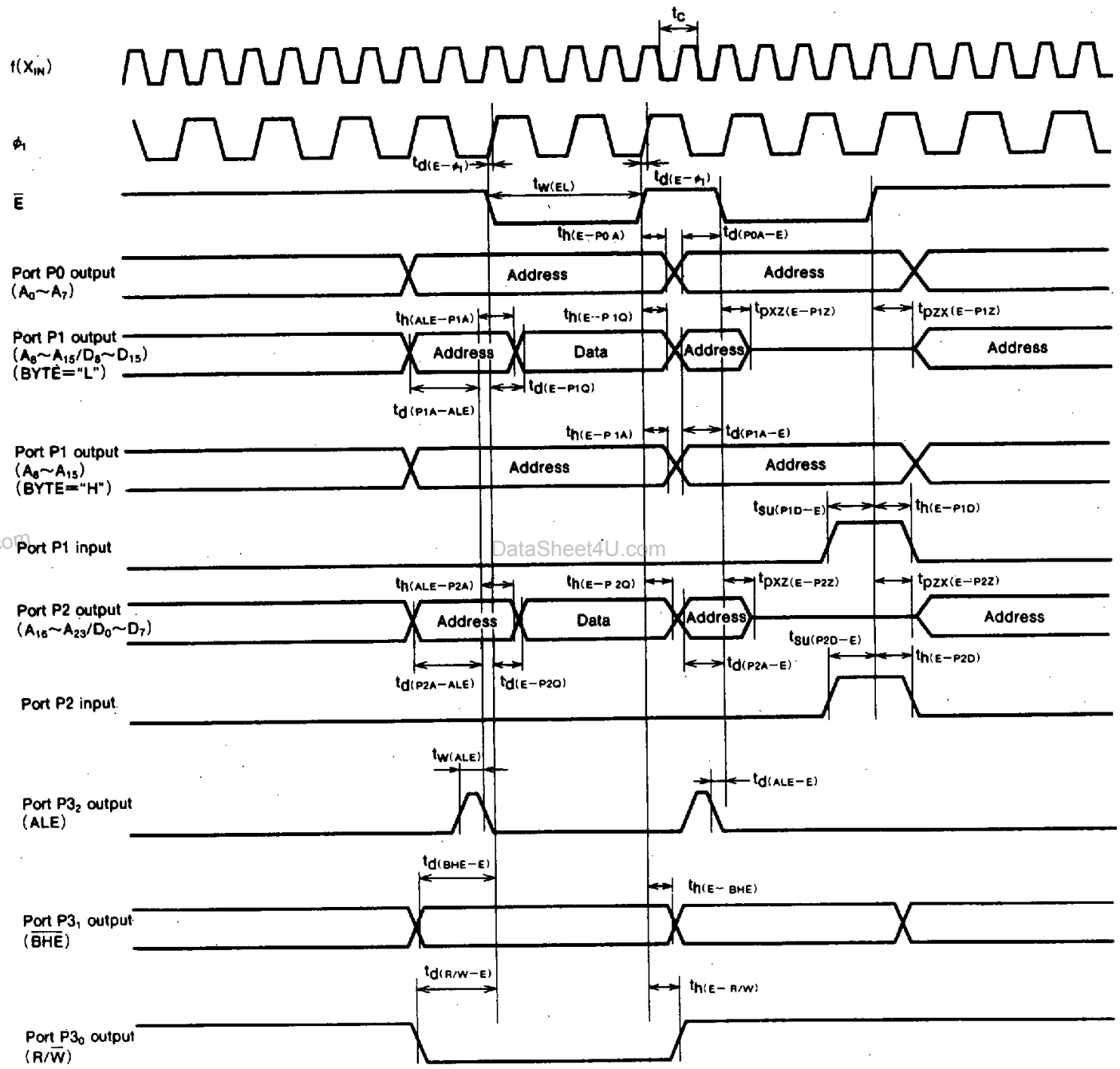
Test conditions

- V_{CC}=5V±10%
- Output timing voltage : V_{OL}=0.8V, V_{OH}=2.0V
- Ports P1, P2 input : V_{IL}=0.8V, V_{IH}=2.5V

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

(When wait bit = "0", wait selection bit = "1", and external memory area is accessed)



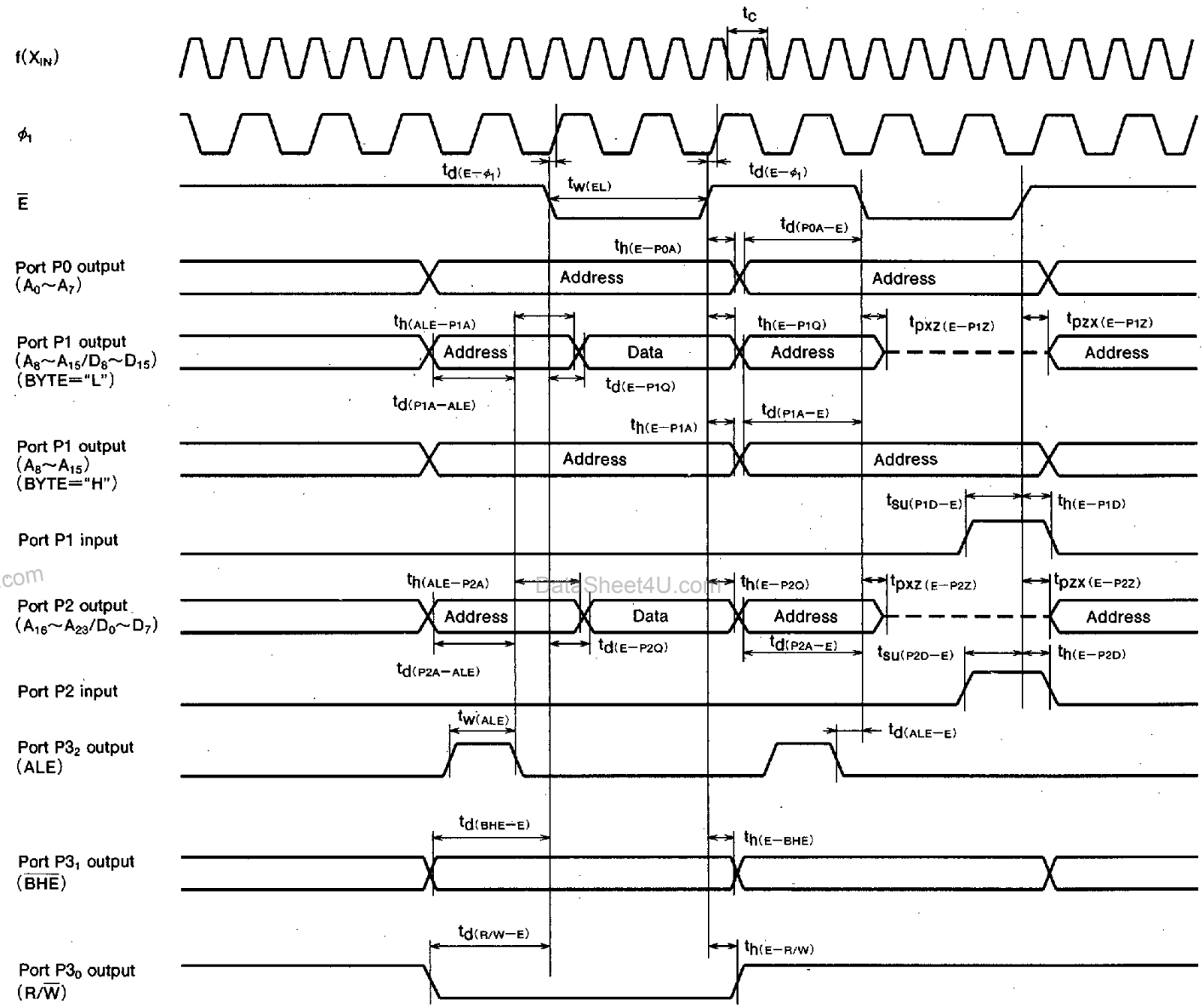
Test conditions

- V_{CC}=5V±10%
- Output timing voltage : V_{OL}=0.8V, V_{OH}=2.0V
- Ports P1, P2 input : V_{IL}=0.8V, V_{IH}=2.5V

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

Memory expansion mode and microprocessor mode

(When wait bit = "0", wait selection bit = "0", and external memory area is accessed)



Test conditions

- V_{CC}=5V±10%
- Output timing voltage : V_{OL}=0.8V, V_{OH}=2.0V
- Ports P1, P2 input : V_{IL}=0.8V, V_{IH}=2.5V

8/16-bit Data Bus Flash Memory Card

MF84M1-G1EATXX

Connector Type

Two-piece 68-pin

DESCRIPTION

The MF84M1-G1EATXX is a flash memory card which uses sixteen two-megabit flash electrically erasable and programmable read only memory IC's.

FEATURES

- 68 pin JEIDA/PCMCIA
- 8/16 controllable data bus width
- Buffered interface
- TTL interface level
- Program/erase operation by software command control
- Program/erase voltage 12V
- 10,000 program/erase cycles
- Write protect switch

APPLICATIONS

- Note book computers
- Printers
- Industrical machines

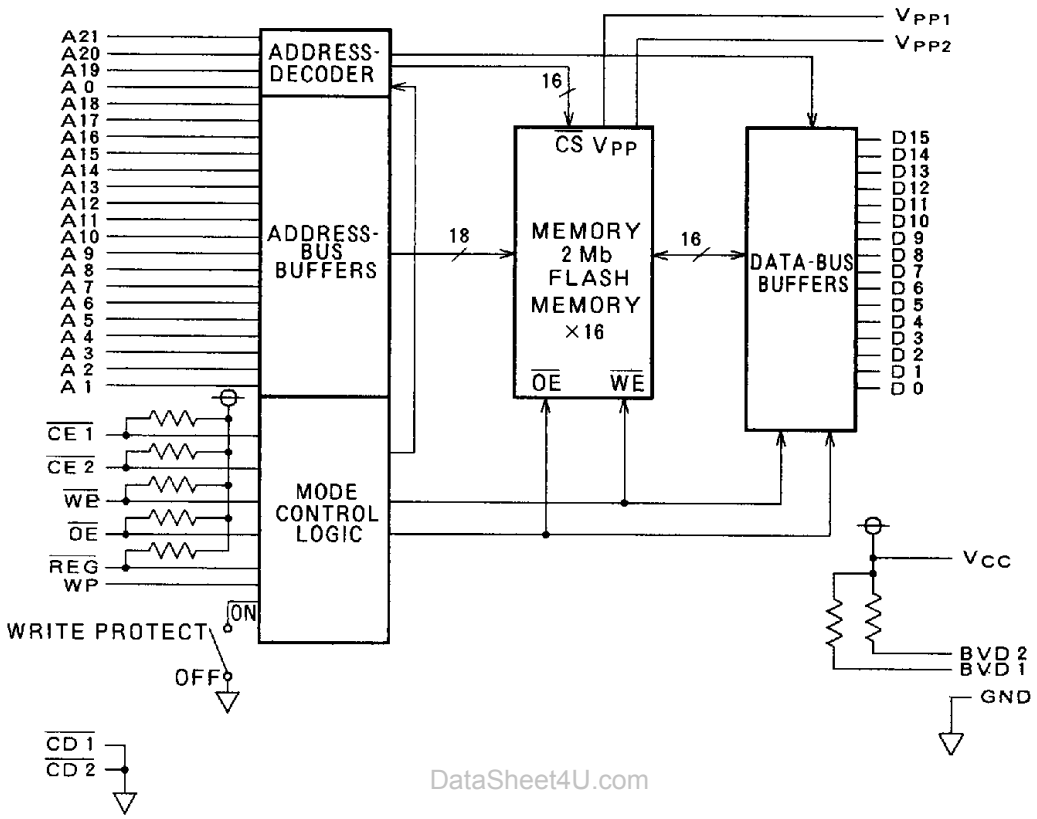
PRODUCT LIST

Item / Type name	Memory capacity	Data bus width (bits)	Access time (ns)	Connector type	Number of pins	Outline drawing
MF84M1-G1EATXX	4 MB	8/16	250	Two-piece	68	68P-002

PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	GND	Ground	35	GND	Ground
2	D 3	Data I/O	36	$\overline{CD\ 1}$	Card detect 1
3	D 4		37	D11	Data I/O
4	D 5		38	D12	
5	D 6		39	D13	
6	D 7		40	D14	
7	$\overline{CE\ 1}$	Card enable 1	41	D15	
8	A10	Address input	42	$\overline{CE\ 2}$	Card enable 2
9	$\overline{OE}$	Output enable	43	NC	No connection
10	A11	Address input	44	NC	
11	A 9		45	NC	
12	A 8		46	A17	Address input
13	A13		47	A18	
14	A14		48	A19	
15	$\overline{WE}$	Write enable	49	A20	
16	NC	No connection	50	A21	
17	V_{CC}	Power supply voltage	51	V_{CC}	Power supply voltage
18	V_{PP} 1	Programming supply voltage 1	52	V_{PP} 2	Programming supply voltage 2
19	A16	Address input	53	NC	No connection
20	A15		54	NC	
21	A12		55	NC	
22	A 7		56	NC	
23	A 6		57	NC	
24	A 5		58	NC	
25	A 4		59	NC	
26	A 3		60	NC	
27	A 2		61	$\overline{REG}$	Attribute memory select
28	A 1		62	BVD 2	Battery voltage detect 2
29	A 0		63	BVD 1	Battery voltage detect 1
30	D 0	Data I/O	64	D 8	Data I/O
31	D 1		65	D 9	
32	D 2		66	D10	
33	WP	Write protect	67	$\overline{CD\ 2}$	Card detect 2
34	GND	Ground	68	GND	Ground

BLOCK DIAGRAM (MF84M1-G1EATXX)



FUNCTIONAL DESCRIPTION

The operating mode of the card is determined by five active low control signals ($\overline{REG}$, $\overline{CE1}$, $\overline{CE2}$, $\overline{OE}$, $\overline{WE}$), three supply voltages (V_{CC}, V_{PP1}, V_{PP2}) and control registers located in each memory IC.

Common memory function

When the $\overline{REG}$ signal is set to a high level common memory is selected.

Read only mode

When the voltages applied to both V_{PP1} and V_{PP2} are less than the voltage applied to V_{CC} (i.e. V_{PP} = 0V to V_{CC}), the control registers of each memory IC are set to read only mode.

Operation of the card then depends on the four possible combinations of $\overline{CE1}$ and $\overline{CE2}$ (note/WE should be set to a high level when the device is in read only mode except during combination (4) where it's condition is unimportant) :

(1) If $\overline{CE1}$ is set to a low level and $\overline{CE2}$ is set to a high level, the card will work as an eight bit data bus width card. Data can be accessed via the lower half of the data bus (D0 to D7).

(2) If both $\overline{CE1}$ and $\overline{CE2}$ are set to a low level, data will be accessible via the full sixteen bit data bus width of the card. In this mode LSB of address bus (A0) is ignored.

(3) If $\overline{CE1}$ is set to a high level and $\overline{CE2}$ is set to a low level the odd bytes (only) can be accessed through upper half of the data bus (D8 to D15). This mode is useful when handling the odd (upper) bytes in a sixteen bit interface system. Note that A0 is also ignored in this operating condition.

(4) If $\overline{CE1}$ and $\overline{CE2}$ are set to a high level, the card will be in standby mode where it consumes low power. The data bus is kept high impedance.

When $\overline{OE}$ is set to a low level data can be read from the card, depending on the address applied and the setting of $\overline{CE1}$ and $\overline{CE2}$ as mentioned above, except under combination (4).

When $\overline{OE}$ is set to a high level and $\overline{WE}$ is set to a high level the card is in an output disable mode and the data bus will be in a high impedance state regardless of the condition of $\overline{CE1}$ and $\overline{CE2}$..

Read/write mode

When a programming voltage ($V_{PP}H$) is applied to either or both of $V_{PP}1$ and $V_{PP}2$, read/write mode is enabled for the corresponding banks of memory IC's inside the card. $V_{PP}1$ enables the Even Byte bank and $V_{PP}2$ enables the Odd Byte bank.

By using the 4 combinations of $\overline{CE1}$ and $\overline{CE2}$ as descibed under Read only mode above the appropriate Data Out and Command/Data In bus selection can be made.

If $\overline{OE}$ is set to a high level and $\overline{WE}$ set to a low level, the control register will latch command data applied at the rising edge of the $\overline{WE}$ signal. Note that more than one bus cycle may be required to latch the command and/or the related data – please refer to the Command Definition table.

If $\overline{OE}$ is set to a low level and $\overline{WE}$ is set to a high level the card data can be read from the card depending on the condition of the control register.

After latching the command data, the card will go into programming, erasure or other operation mode. For details please refer to the Command Definition table, each individual command's definition and the programming and erasure algorithms.

Attribute memory

When $\overline{REG}$ is set to a low level attribute memory is selected.

The card then outputs FFh on the lower half of the data bus (D0 to D7) when the following conditions are applied :

(1) $\overline{CE1}$: low level, $\overline{CE2}$: high level, $\overline{OE}$: low level, $\overline{WE}$: high level, A0 : low level
(2) $\overline{CE1}$: low level, $\overline{CE2}$: low level, $\overline{OE}$: low level, $\overline{WE}$: high level.

Write protect mode

The card has a write protect switch on the opposite edge to the connector edge. When it is switched on, the card will be placed into a write protect mode, where data can be read from the card but it cannot be written to it. The WP output pin is set to a high level when the card is in write protect mode and V_{CC} is applied. When the card is not in write protect mode the WP output pin is set to a low level when V_{CC} is applied. By reading the state of the WP output the host system can easily check whether the card is in write protect mode or not.