

HYUNDAI
SEMICONDUCTOR
HYM59256A

256K×9-Bit CMOS DRAM MODULE

M451202B-OCT91

T-46-23-17

DESCRIPTION

The HYM59256AM is a 256K words by 9bits dynamic RAM module and consists of Fast Page mode CMOS DRAMs of two HY534256J in 20/26 pin SOJ and one HY53C256LF in 18 pin PLCC mounted on a 30 pin glass-epoxy printed circuit board. 0.22μF decoupling capacitors are mounted under all the DRAMs.

HYM59256AM is suitable for easy interchange and addition of 256K bytes memory with parity RAM.

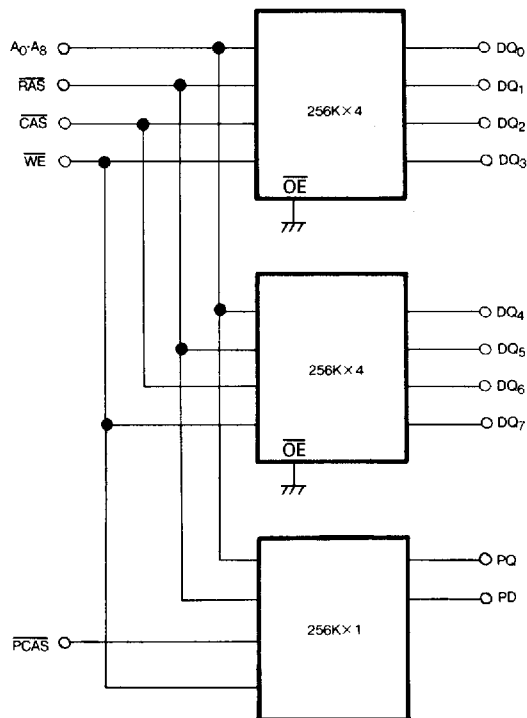
FEATURES

- Fast Page Mode operation
- Fast Access Time

	t _{RAC}	t _{CAC}	t _{PC}
HYM59256AM-70	70	20	50
HYM59256AM-80	80	25	55
HYM59256AM-100	100	25	60

- Single power supply of 5V±10%
- CAS Before RAS, RAS only, Hidden Refresh.
- Low power operating
 - 1.26W max (HYM59256AM-70)
 - 1.10W max (HYM59256AM-80)
 - 0.93W max (HYM59256AM-100)
- TTL compatible inputs and outputs
- 512 refresh cycles / 8ms

BLOCK DIAGRAM

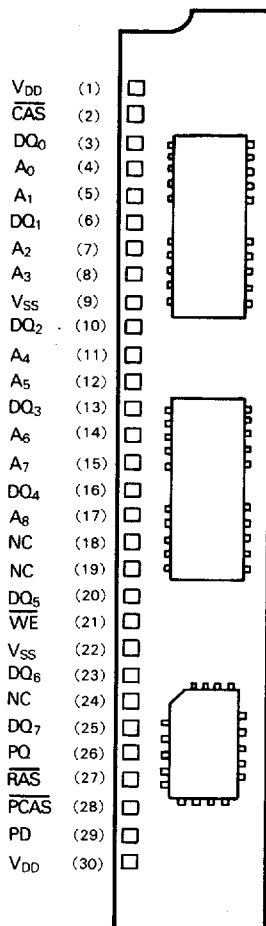


PIN NAMES

A ₀ -A ₈	ADDRESS INPUT
DQ ₀ -DQ ₇	DATA INPUT/OUTPUT
PD	DATA IN FOR PARITY
PQ	DATA OUT FOR PARITY
RAS	ROW ADDRESS STROBE
CAS	COLUMN ADDRESS STROBE
PCAS	CAS FOR PARITY
WE	WRITE ENABLE
V _{DD}	POWER(+5V)
V _{SS}	GROUND

HYM59256A 262,144×9-Bit CMOS DRAM MODULE**PIN CONNECTIONS**

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HYM59256AM**NOTES :**

1. Common $\overline{\text{CAS}}$ control for eight data-in and data-out lines (DQ₀-DQ₇).
2. Separate $\overline{\text{PCAS}}$ control for one separate pair of data-in (PD) and data-out (PQ) lines.
3. The common I/O feature dictates the use of only early write operations to prevent contention on data-in and data-out (DQ₀-DQ₇).

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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature(Plastic)	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	-1.0 to 7.0	V
V_{DD}	Voltage on V_{DD} Relative to V_{SS}	-1.0 to 7.0	V
I_{OS}	Short Circuit Output Current	50	mA
P_T	Power Dissipation	1.8	W

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

 $(T_A = 0^\circ\text{C to } 70^\circ\text{C})$

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.4	—	$V_{DD} + 1$	V
V_{IL}	Input Low Voltage	-1.0	—	0.8	V

NOTE : All voltages are reference to V_{SS} .

DC CHARACTERISTICS

 $(T_A = 0^\circ\text{C to } 70^\circ\text{C}, V_{DD} = 5V \pm 10\%, V_{SS} = 0V, \text{ unless otherwise noted.})$

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED	HYM59256AM		UNIT	NOTE
				MIN.	MAX.		
$ I_{LI} $	Input Leakage Current(any input pin)	$V_{SS} \leq V_{IN} \leq V_{DD}$			30	μA	
$ I_{LO} $	Output Leakage Current for High Impedance State	$V_{SS} \leq D_{OUT} \leq V_{DD}$ $\overline{RAS}, \overline{CAS}$ at V_{IH}			10	μA	
I_{DD1}	V_{DD} Supply Current, Operating	$t_{RC} = t_{RC}(\text{min.})$	-70		230	mA	1, 2
			-80		200		
			-10		170		
I_{DD2}	V_{DD} Supply Current, TTL Standby	$\overline{RAS}, \overline{CAS}$ at V_{IH} other inputs $\geq V_{SS}$			6	mA	
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$ -only Refresh	$t_{RC} = t_{RC}(\text{min.})$	-70		230	mA	2
			-80		200		
			-10		170		
I_{DD4}	V_{DD} Supply Current, Fast Page Mode	Minimum Cycle	-70		165	mA	1, 2
			-80		140		
			-10		115		
I_{DD5}	V_{DD} Supply Current, CMOS Standby	$\overline{RAS} \geq V_{DD} - 0.2V, \overline{CAS} = V_{IH}, \text{ other inputs } \geq V_{SS}$			3	mA	
I_{DD6}	V_{DD} Supply Current, $\overline{CAS}$ -Before- $\overline{RAS}$ Refresh	$t_{RC} = t_{RC}(\text{min.})$	-70		230	mA	2
			-80		200		
			-10		170		
V_{OL}	Output Low Voltage	$I_{OL} = 4.2\text{mA}$			0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -5\text{mA}$		2.4		V	

NOTES :

- I_{DD} is dependent on output loading when the device output is selected, Specified $I_{DD}(\text{max.})$ is measured with the output open.
- I_{DD} is dependent upon the number of address transitions. Specified $I_{DD}(\text{max.})$ is measured with a maximum of two transitions per address cycle in fast page mode.

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AC CHARACTERISTICS

(T_A=0°C to 70°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted.)

#	SYMBOL	PARAMETER	HYM59256AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	t _{RAS}	RAS Pulse Width	70	10K	80	10K	100	10K	ns	
2	t _{RC}	Random Read or Write Cycle Time	130		150		180		ns	
3	t _{RP}	RAS Precharge Time	50		60		70		ns	
4	t _{ASR}	Row Address Set-up Time	0		0		0		ns	
5	t _{RAH}	Row Address Hold Time	15		15		15		ns	
6	t _{RAL}	Column Address to $\overline{\text{RAS}}$ Lead Time	35		40		50		ns	
7	t _{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	20	50	20	60	25	75	ns	1
8	t _{ASC}	Column Address Set-up Time	0		0		0		ns	
9	t _{CAH}	Column Address Hold Time	15		15		20		ns	
10	t _{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	25	55	25	60	25	75	ns	2
11	t _{RAC}	Access Time from $\overline{\text{RAS}}$		70		80		100	ns	3,4,5
12	t _{AA}	Access Time from Column Address		35		40		50	ns	5,7
13	t _{CAC}	Access Time from $\overline{\text{CAS}}$		20		25		25	ns	5,6
14	t _{CAS}	$\overline{\text{CAS}}$ Pulse Width	20		25		30		ns	
15	t _{RSH}	$\overline{\text{RAS}}$ Hold Time	25		25		30		ns	
16	t _{RCS}	Read Command Set-up Time	0		0		0		ns	
17	t _{RCH}	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	5		5		5		ns	8
18	t _{RRH}	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	5		5		5		ns	8
19	t _{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	15		15		15		ns	
20	t _{HZ}	$\overline{\text{CAS}}$ to Output High Impedance	0	20	0	25	0	30	ns	11
21	t _{WP}	Write Command Pulse Width	15		15		20		ns	
22	t _{CP}	$\overline{\text{CAS}}$ Precharge Time	15		15		20		ns	
23	t _{AR}	Column Address Hold Time from $\overline{\text{RAS}}$	55		60		75		ns	
24	t _{WCR}	Write Command Hold Time from $\overline{\text{RAS}}$	55		60		75		ns	
25	t _{WCS}	Write Commnad Set-up Time	0		0		0		ns	9
26	t _{WCH}	Write Command Hold Time	15		15		20		ns	
27	t _{DS}	Data In Set-up Time	0		0		0		ns	10
28	t _{DH}	Data In Hold Time	15		15		20		ns	10

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#	SYMBOL	PARAMETER	HYM59256AM						UNIT	NOTE
			70		80		10			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
29	tDHR	Data-In Hold Time Referenced to $\overline{\text{RAS}}$	55		60		75		ns	
30	tCPA	Access Time from Column Precharge		35		40		50	ns	12
31	tPC	Fast Page Mode Read or Write Cycle Time	50		55		60		ns	
32	tRWL	Write Command to $\overline{\text{RAS}}$ Lead Time	20		25		30		ns	
33	tCWL	Write Command to $\overline{\text{CAS}}$ Lead Time	20		25		30		ns	
34	tRPC	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Precharge Time	0		0		0		ns	
35	tCSR	$\overline{\text{CAS}}$ Set-up Time($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle)	5		5		5		ns	
36	tCHR	$\overline{\text{CAS}}$ Hold Time($\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Cycle)	20		25		30		ns	
37	tT	Transition Time(Rise and Fall)	3	50	3	50	3	50	ns	13
38	tREF	Refresh Interval(512 Cycle)		8		8		8	ms	16
39	tRASP	$\overline{\text{RAS}}$ Pulse Width(Fast Page Mode)	70	100K	80	100K	100	100K	ns	
40	tCPT	$\overline{\text{CAS}}$ Precharge Time(CBR Counter Test Cycle)	40		40		50		ns	
41	tCLZ	$\overline{\text{CAS}}$ to Output Low Impedance	0		0		0		ns	3

NOTES :

- Operation within the t_{RAD}(max.) limit insures that t_{TRAC}(max.) can be met. t_{TRAD}(max.) is specified as a reference point only. If t_{TRAD} is greater than the specified t_{RAD}(max.) limit, then the access time is controlled by t_{AA} and t_{CAC}.
- Operation within the t_{TRCD}(max.) limit insures that t_{TRAC}(max.) can be met. t_{TRCD}(max.) is specified as a reference point only. If t_{TRCD} is greater than the specified t_{TRCD}(max.) limit, then access time is controlled by t_{CAC}.
- Assume t_{TRAD} ≤ t_{TRAD}(max.). If t_{TRAD} is greater than t_{TRAD}(max.) then t_{TRAC} will increase by the amount that t_{TRAD} exceeds t_{TRAD}(max.).
- Assume t_{TRCD} ≤ t_{TRCD}(max.). If t_{TRCD} is greater than t_{TRCD}(max.) then t_{TRAC} will increase by the amount that t_{TRCD} exceeds t_{TRCD}(max.).
- Measured with a load equivalent to two TTL loads and 100pF.
- Assumes that t_{RCD} ≥ t_{RCD}(max.) and t_{TRAD} ≤ t_{TRAD}(max.).
- Assumes that t_{RCD} ≤ t_{RCD}(max.) and t_{TRAD} ≤ t_{TRAD}(max.).
- Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.
- t_{WCS} is not a restrictive operating parameter. This is included in the data sheet as a electrical characteristic only. If t_{WCS} ≥ t_{WCS}(min.), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle.
- t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{\text{CAS}}$ or $\overline{\text{WE}}$.
- t_{HZ} defines the time at which the data output achieves the open circuit condition and is not referenced to the output voltage levels.
- Access time is determined by the longer of t_{AA}, t_{CAC} or t_{CPA}.
- t_f is measured between V_{IH}(min.) and V_{IL}(max.) and AC Measurements assume t_f=5ns.
- An initial pause of 200μs is required after power-up and followed at least 8 initialization cycles(any combination of cycles containing a $\overline{\text{RAS}}$ clock such as $\overline{\text{RAS}}$ -only Refresh). 8 initialization cycles are required after extended periods of bias without clocks.

CAPACITANCE

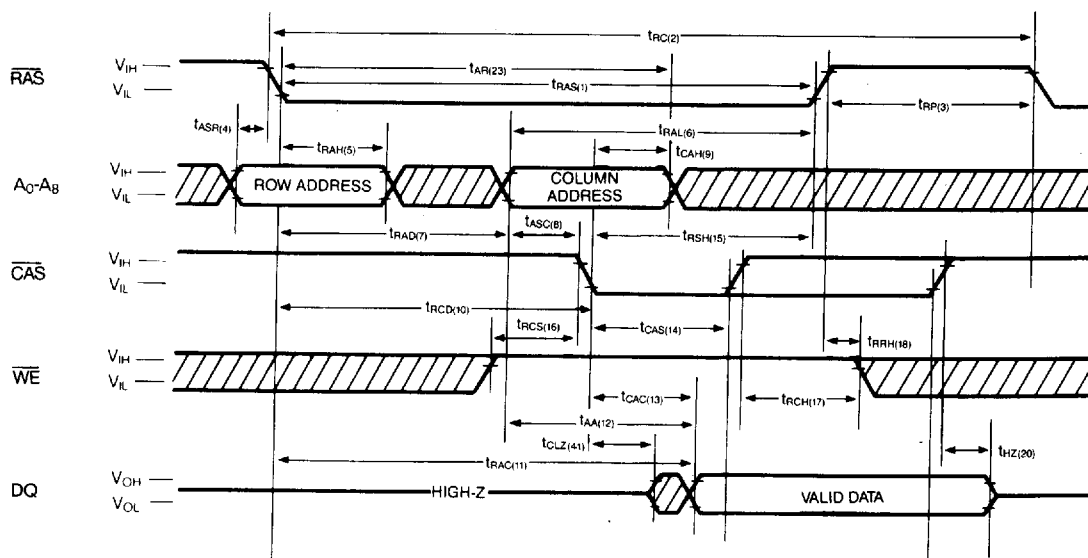
(T_A=25°C, V_{DD}=5V±10%, V_{SS}=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
C _{IN1}	Input Capacitance(A ₀ -A ₈ , $\overline{\text{WE}}$, $\overline{\text{CAS}}$, $\overline{\text{RAS}}$)	—	25	pF
C _{IN2}	Input Capacitance(PD, $\overline{\text{PCAS}}$)	—	10	pF
C _{DQ}	I/O Capacitance(DQ ₀ -DQ ₇)	—	15	pF
C _{PQ}	Output Capacitance(PQ)	—	10	pF

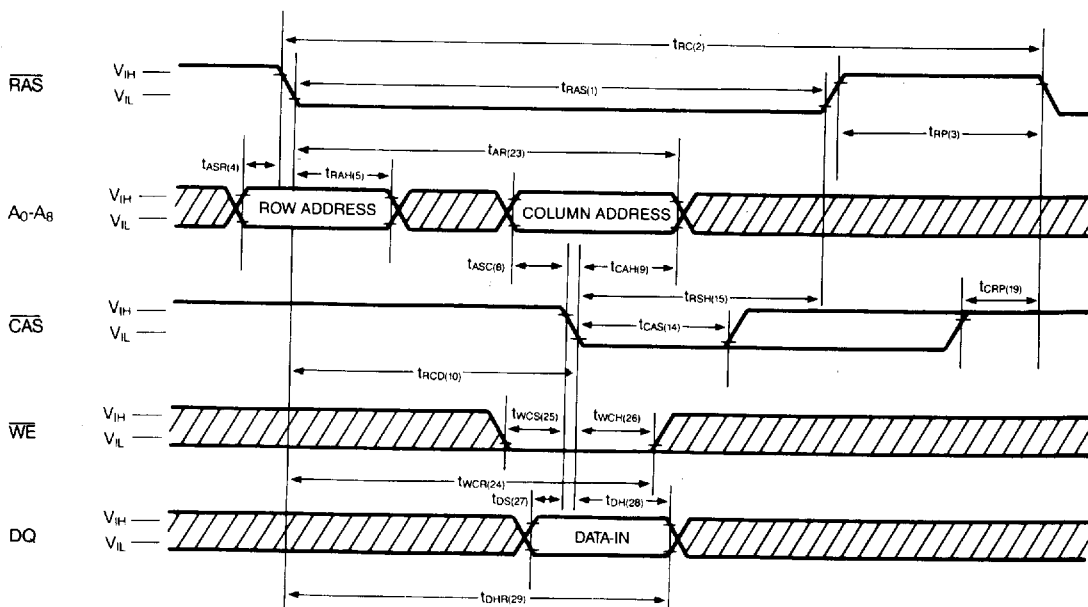
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TIMING DIAGRAM

READ CYCLE

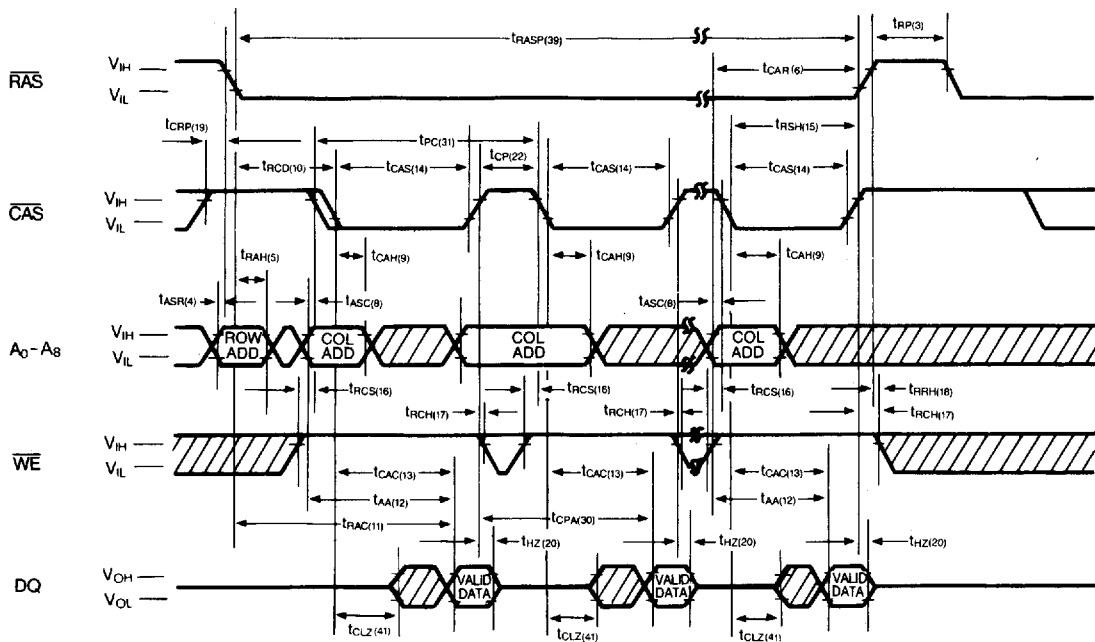


EARLY WRITE CYCLE

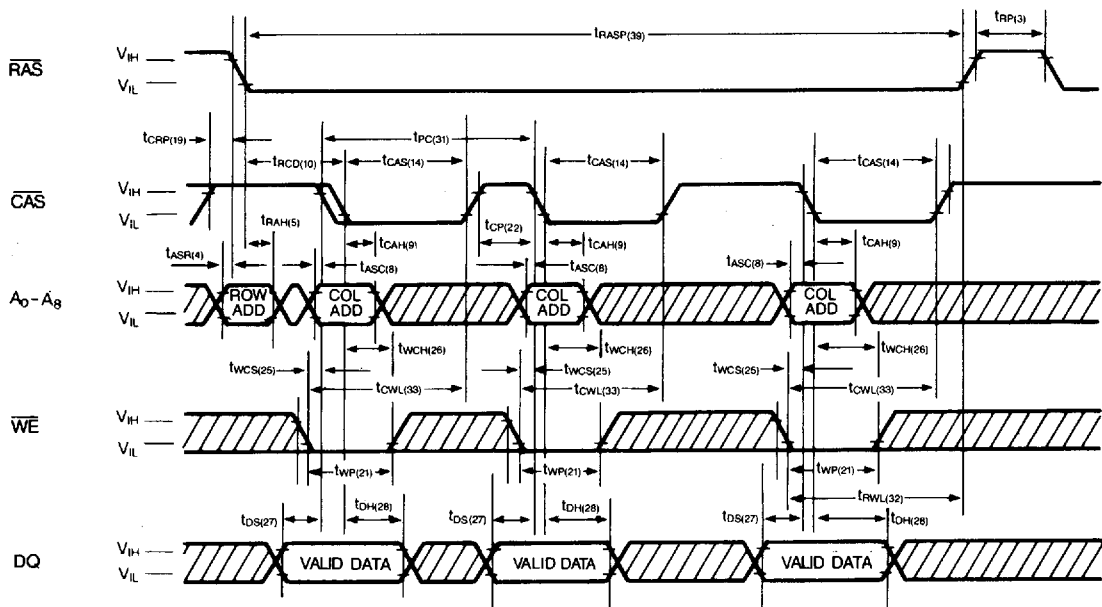


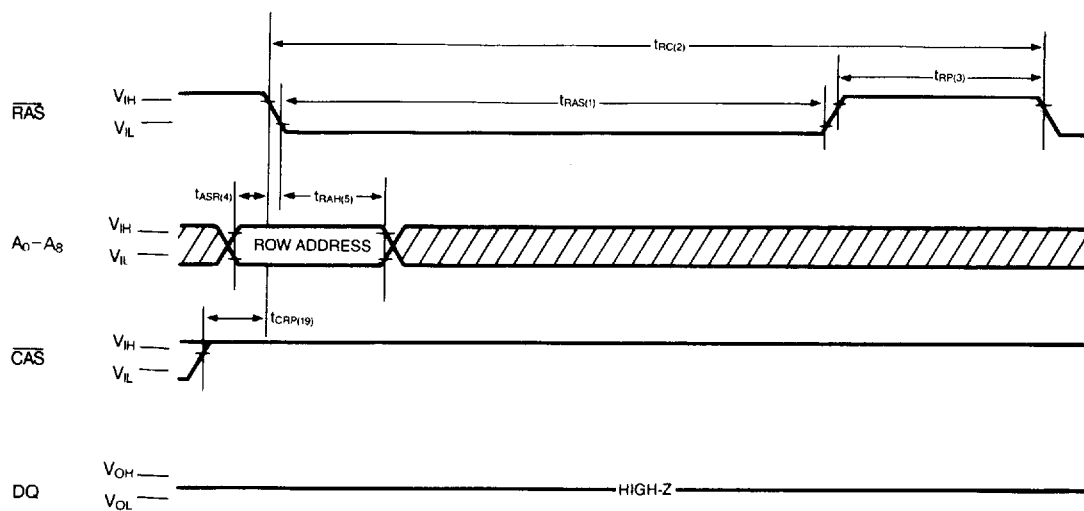
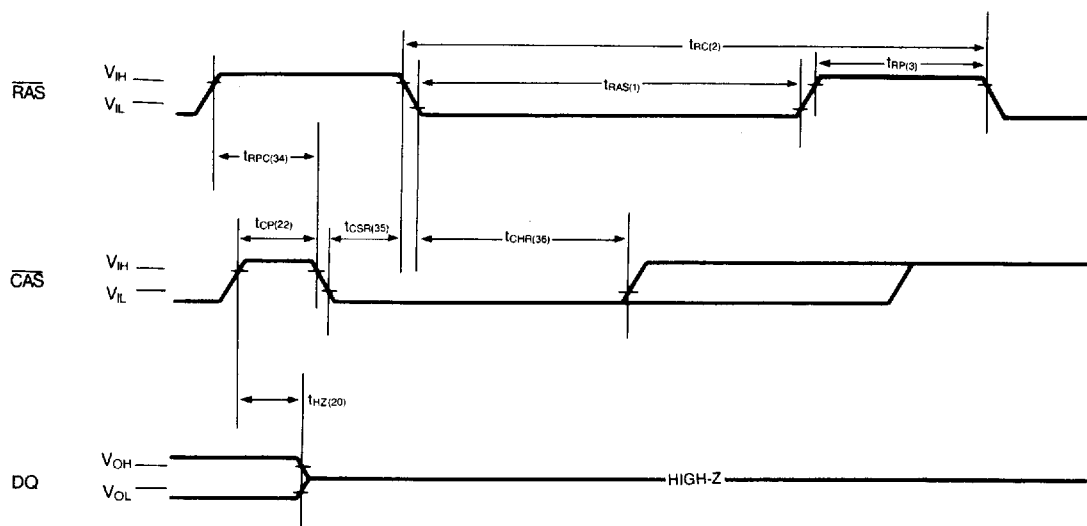
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FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE

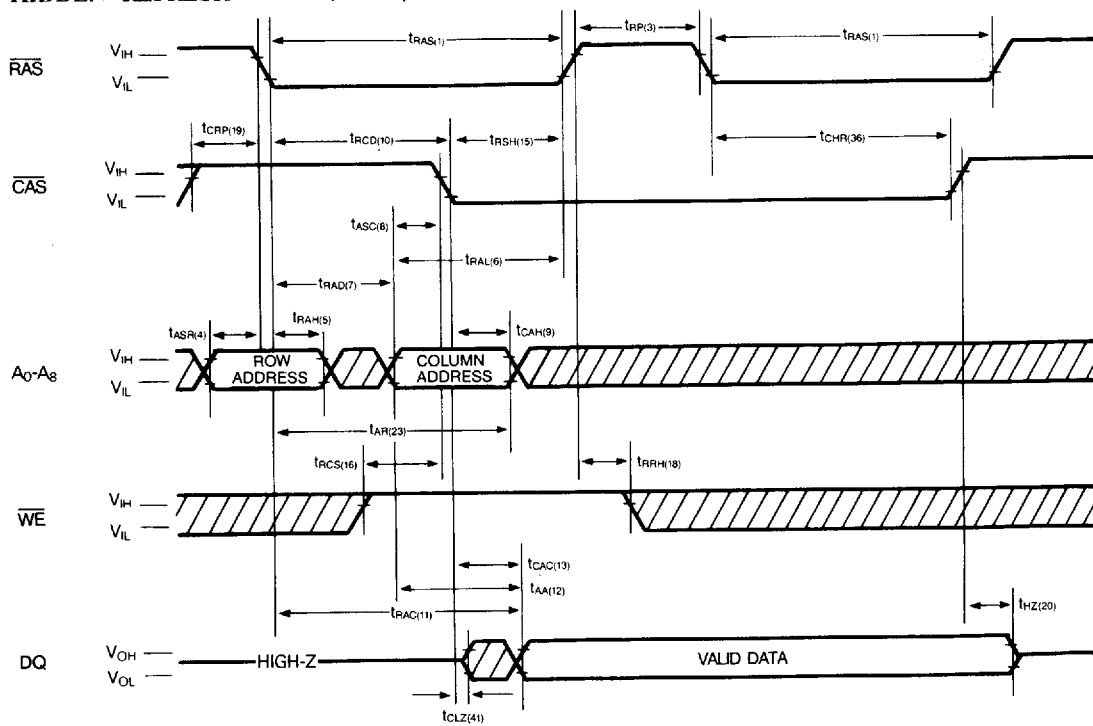


RAS-ONLY REFRESH CYCLE**CAS-BEFORE-RAS REFRESH CYCLE**

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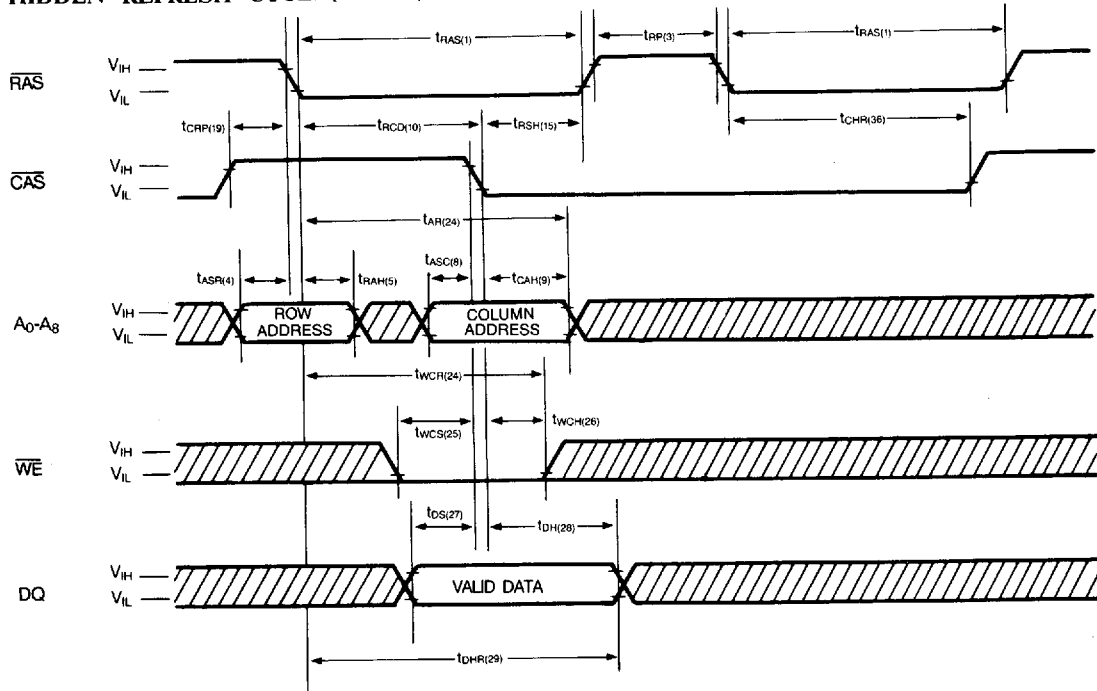
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HIDDEN REFRESH CYCLE(READ)



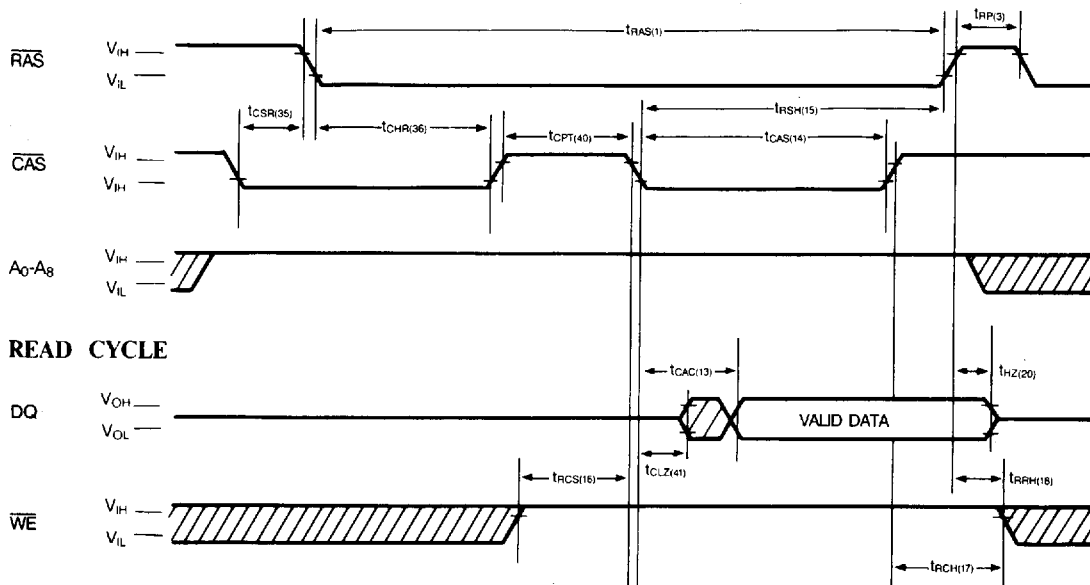
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HIDDEN REFRESH CYCLE(WRITE)

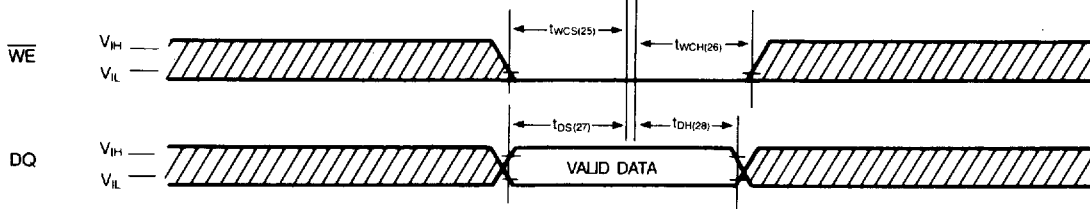


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 $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ REFRESH COUNTER TEST CYCLE

WRITE CYCLE



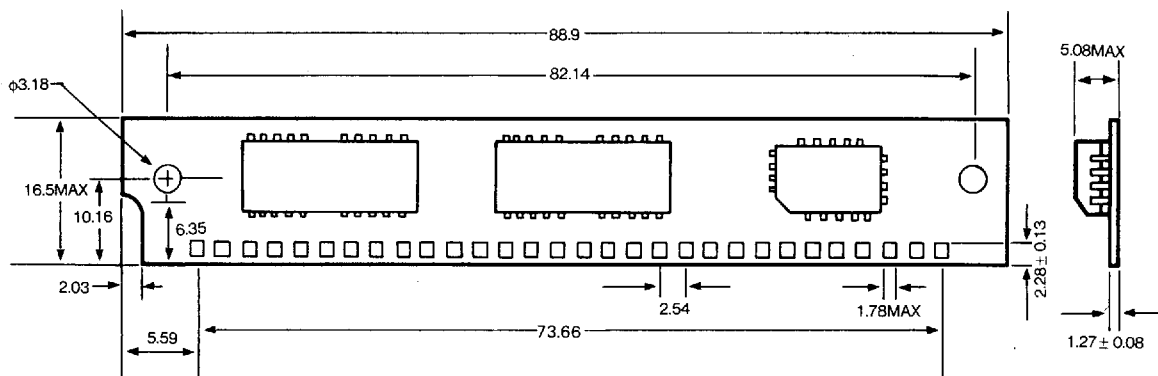
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PACKAGE INFORMATION

HYM59256AM

UNIT : mm



* DETAIL OF CONTACTS

