Preliminary

Product Hardware Specification

AHA361-PCIX

2.0 Gbps Internet Protocol Accelerator

This product is covered under mulitple patents pending.

PS361-PCIX_HW_0404

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1.0 INTRODUCTION

This document provides a high level technical description of the AHA361-PCIX GZIP Compression Accelerator printed circuit board (PCB). General software and programming information can be found in the AHA361-PCIX *Hardware Interface Specification.*

The AHA361-PCIX is a PCI-X plug-in card that adds GZIP compression to internet data streams. This card supports GZIP compression with data transfer rates up to 2.0 Gigabits/sec. The AHA361-PCIX offers compression throughput several orders of magnitude beyond that available from software-based solutions. The average compression ratio permits twice as much data to be transmitted on a link. Efficient use of bandwidth maximizes the use of expensive links.

Reducing download time for web content is a challenge facing many companies. Data compression is a powerful method for reducing bandwidth requirements consumed by data-intensive dynamic websites and high volume traffic. The AHA361-PCIX board performs GZIP compression so that the minimal CPU bandwidth is consumed during software compression. Through the use of GZIP compression hardware, websites with dynamic data can quickly be compressed and sent through the internet pipeline with minimal 'wait time' to users and without loading down the host CPU.

1.1 FEATURES

PERFORMANCE

- Open standard compression algorithm (GZIP/ Deflate)
- Full duplex links can be created with a combination of hardware and software.
- Uses patented hardware compression integrated circuits
- PCI-X, 64-bit, 100 MHz edge card interface
- Compresses at a throughput rate of 2.0 Gbps
- HTML compresses greater than 2:1
- Unlimited sessions, files, or streams

SOFTWARE SUPPORT

- Linux reference drivers with source code
- Demonstration software

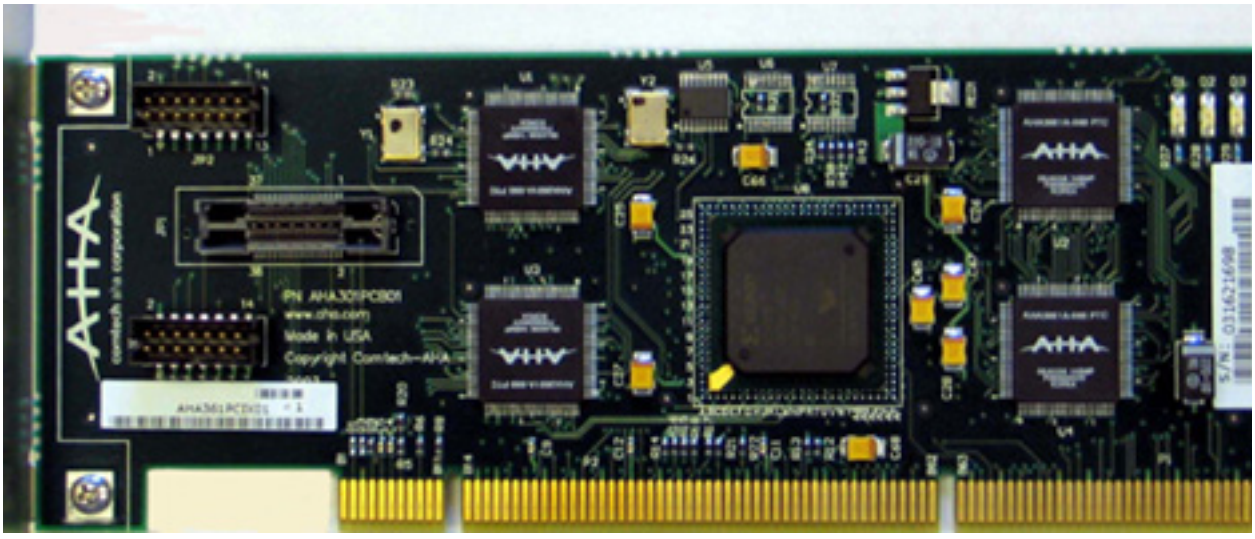
PHYSICAL:

- Operating Voltage 3.3V
- PCB size is half height, short PCI-X card (2.5" x 6.5")
- Field upgradability of on-board FLASH memory (Not Yet Implemented).

1.2 SYSTEM REQUIREMENTS

The AHA361-PCIX PCB requires that the host computer have a PCI-X interface bus. The operating voltage is 3.3V. PCI-X clock speed can be slower than 100 MHz.

Figure 1: AHA361-PCIX PCB



1.3 DEFINITIONS

File/stream A coherent set of data made up of one or more blocks.

Block An input block or output block. Output blocks are compressed and are also called Deflate blocks. Currently, a block contains one chunk.

Chunk A set of data no bigger than 4096 (4K) Bytes. Should be set to maximum PCI transfer size for system for highest performance.

Channel A data path for one AHA3601 compression/decompression engine. The AHA361-PCIX has from one to four channels.

2.0 FUNCTIONAL DESCRIPTION

2.1 OVERVIEW

The AHA361-PCIX Compression Accelerator is a PCI-X 2.0 compliant printed circuit board that provides high-speed data compression to its host. It uses four AHA3601 compression coprocessors and a controller to sustain uncompressed input data rates up to 2.0 Gigabits/sec.

The AHA361-PCIX compression accelerator is designed to off-load data compression tasks from the host processor. The PCI-X interface is constructed for minimum processor interaction and maximum throughput. The local bus between the PCI-X interface and the stream multiplexer/ demultiplexer does not degrade the performance of the PCI-X bus.

The AHA361-PCIX board acts as a master for writing compressed data back to a target. The device can be a master or target for the uncompressed data transaction. If the device is to act as the master, the driver is required to setup the device to do a Direct Memory Access (DMA) read. If the device will be the target, data is transferred by writing it to an address in the space of Base Address Register 0 (BAR0).

The DMA stream is demultiplexed and fed to four separate compression channels on the board. Data is transferred to the AHA3601 hardware compression engines to be compressed. The compressed data is then re-multiplexed back together for DMA transfer back to the host over the PCI-X bus.

For more information on the DMA transfers and the driver software, please refer to the AHA361-PCIX Product Hardware Interface Specification.

2.2 BOARD CONFIGURATION FLASH

The AHA361-PCIX uses a Xilinx FLASH SPROM to hold the FPGA configuration program. The program in the SPROM is updated by downloading a bit file using JTAG and the JP3 interface connector. The signal connections for this are given below. Each time the board is power cycled the FPGA loads its configuration program from the FLASH memory.

Table 1: JP3 (JTAG) SIGNAL CONNECTIONS

SIGNAL	*PIN*
VDD 3.3V	2
TMS	4
TCK	6
TDO	8
TDI	10

Note: All odd pins on JP3 are connected to ground.

3.0 GENERAL SPECIFICATIONS

3.1 CLOCKS

- PCI/PCI-X: 100 MHz maximum
- On-board local clock: 80 MHz
- JTAG clock: 33 MHz

3.2 LEDS

- D3: indicates FPGA configured properly
- D2: diagnostics
- D1: diagnostics

3.3 JTAG

Chain order:

- Xcfo4s SPROMs, U4, U5, U6, U7. Unused SPROMs are bypassed
- Xilinx FPGA U8

3.4 POWER

3.3V only. Power dissipation TBD.