010722

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Convert to military drawing format. Changes to table I. Add vendor CAGE 50088. Change code identification number to 67268.	1987 NOV 9	
B	Table I, change I_{IH2} test conditions and delete t_{s2}, t_{h2}, t_{s7}, t_{h7}, t_{pd5}, and t_{pd6}. Change figure 2. Editorial changes throughout.	1988 DEC 2	

CURRENT CAGE CODE 67268

REV STATUS OF SHEETS																		
REV	B	B	B	B	B	B	B	B	A	B	B	A	A	B	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Greg A. Pitz

CHECKED BY Ray Monnin

APPROVED BY

DRAWING APPROVAL DATE 19 FEBRUARY 1986

REVISION LEVEL B

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, 4-BIT, BIPOLAR, MICROPROGRAM SEQUENCER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	86028

SHEET 1 OF 17

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5962-E1001

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

86028	01	R	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device type. The device type shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	2911A	Microprogram sequencer

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200"), dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage range - - - - - - - - - - - - - - - - -	-0.5 V dc to +7.0 V dc
Input voltage range- - - - - - - - - - - - - - - - - -	-0.5 V dc to +5.5 V dc
Storage temperature range- - - - - - - - - - - - - -	-65°C to +150°C
Maximum power dissipation (P_D) 1/- - - - - - - - - -	.770 W
Lead temperature (soldering, 10 seconds) - - - - - -	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	
Case R -	See MIL-M-38510, appendix C
Junction temperature (T_J)- - - - - - - - - - - - - - -	+175°C
DC output current, into inputs - - - - - - - - - - - -	+30 mA
DC input current - - - - - - - - - - - - - - - - - - -	-30 mA to +5.0 mA

1.4 Recommended operating conditions.

Supply voltage (V_{CC}) - - - - - - - - - - - - - - - - -	4.5 V dc minimum to 5.5 V dc maximum
Minimum high level input voltage (V_{IH}) - - - - - - - -	2.0 V dc
Maximum low level input voltage (V_{IL})- - - - - - - -	0.8 V dc
Case operating temperature range (T_C)- - - - - - - -	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^\circ C \le T_C \le +125^\circ C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified		Group A subgroups	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = minimum, $I_{OH} = -1.0$ mA $V_{IN} = V_{IH}$ or V_{IL}		1, 2, 3	2.4		V
Output low voltage	V_{OL}	V_{CC} = minimum, $I_{OL} = 16$ mA $V_{IN} = V_{IH}$ or V_{IL}		1, 2, 3		0.5	V
Input high level	V_{IH}			1, 2, 3	2.0		V
Input low level	V_{IL}			1, 2, 3		0.8	V
Input clamp voltage	V_{IC}	V_{CC} = minimum, $I_{IN} = -18$ mA		1, 2, 3		-1.5	V
Input low current	I_{IL}	V_{CC} = maximum, $V_{IN} = 0.4$ V	C_n	1, 2, 3		-1.08	mA
			Push/pop, $\overline{OE}$, Di	1, 2, 3		-0.72	
			Others			-0.36	
Input high current	I_{IH1}	V_{CC} = maximum, $V_{IN} = 2.7$ V	C_n			40	µA
			Push/pop, $\overline{OE}$, Di	1, 2, 3		40	
			Others			20	
Input high current	I_{IH2}	V_{CC} = maximum, $V_{IN} = 5.5$ V	C_n, push/pop, Di	1, 2, 3		0.2	mA
			Others			0.1	
Output short circuit current 1/	I_{OS}	$V_{CC} = 6$ V, $V_{OUT} = 0.5$ V	$Y_0 - Y_3$	1, 2, 3	-30	-100	mA
			$C_n + 4$		-30	-85	
Power supply current	I_{CC}	V_{CC} = maximum 2/	$T_C = -55^\circ C$ to $+125^\circ C$	1, 2, 3		140	mA
			$T_C = +125^\circ C$	2		110	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Output OFF current	I_{OZL}	V_{CC} = maximum, $\overline{OE}$ = 2.7, Y_{0-3}, V_{OUT} = 0.4 V	1, 2, 3		-20	µA
	I_{OZH}	V_{OUT} = 2.7 V			20	
Functional testing		See 4.3.1c	7, 8			
Set-up time 1 $\overline{RE}$	t_{s1}	See figures 4 and 5, C_L = 50 pF	9, 10, 11	19		ns
Hold time 1 $\overline{RE}$	t_{h1}		9, 10, 11		5	ns
Set-up time 3 PUP	t_{s3}		9, 10, 11	27		ns
Hold time 3 PUP	t_{h3}		9, 10, 11		5	ns
Set-up time 4 $\overline{FE}$	t_{s4}		9, 10, 11	27		ns
Hold time 4 $\overline{FE}$	t_{h4}		9, 10, 11		5	ns
Set-up time 5 C_n	t_{s5}		9, 10, 11	18		ns
Hold time 5 C_n	t_{h5}		9, 10, 11		5	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Set-up time 6 D_i	t_{s6}	See figures 4 and 5, C_L = 50 pF	9, 10, 11	25		ns
Hold time 6 D_i	t_{h6}		9, 10, 11		0	ns
Set-up time 8 S_0, S_1	t_{s8}		9, 10, 11	29		ns
Hold time 8 S_0, S_1	t_{h8}		9, 10, 11		0	ns
Set-up time 9 $\overline{ZERO}$	t_{s9}		9, 10, 11	29		ns
Hold time 9 $\overline{ZERO}$	t_{h9}		9, 10, 11		0	ns
Propagation delay 1-2 from (input): D_i to (output): Y	t_{pd1}		9, 10, 11		20	ns
to (output): C_{n+4}	t_{pd2}				25	ns
Propagation delay 3-4 from (input): S_0, S_1 to (output): Y	t_{pd3}		9, 10, 11		29	ns
to (output): C_{n+4}	t_{pd4}				34	ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ V_{CC} = 4.5 V to 5.5 V unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay 7 from (input): C_n to (output): C_n +4	t_{pd7}	See figures 4 and 5, C_L = 50 pF	9, 10, 11		16	ns
Propagation delay 8-9 from (input): $\overline{ZERO}$ to (output): Y	t_{pd8}		9, 10, 11		30	ns
to (output): C_n+4	t_{pd9}				35	ns
Propagation delay 10 from (input): $\overline{OE}$ low (enable) to (output): Y	t_{pd10}		9, 10, 11		25	ns
Propagation delay 11 from (input): $\overline{OE}$ high (disable) to (output): Y	t_{pd11}	See figures 4 and 5, C_L = 5 pF	9, 10, 11		25	ns
Propagation delay 12-13 from (input): Clock S_1, S_0 = LH to (output): Y	t_{pd12}	See figures 4 and 5, C_L = 50 pF	9, 10, 11		45	ns
to (output): C_n+4	t_{pd13}				50	ns
Propagation delay 14-15 from (input): Clock S_1, S_0 = LL to (output): Y	t_{pd14}		9, 10, 11		45	ns
to (output): C_n+4	t_{pd15}				50	ns

See footnotes at end of table.

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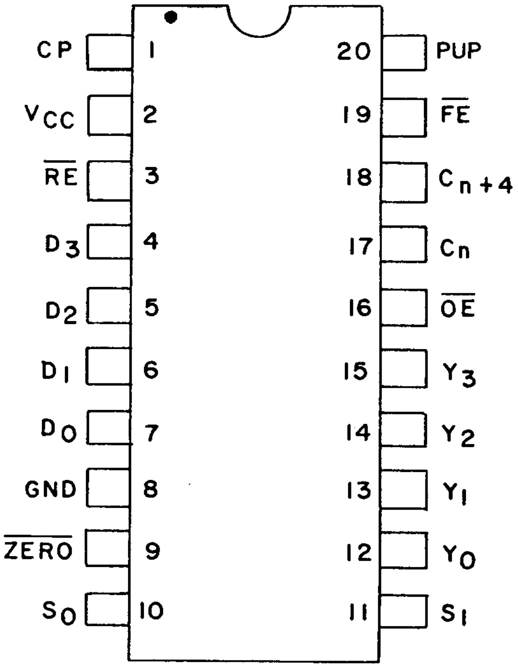
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ $V_{CC} = 4.5$ V to 5.5 V unless otherwise specified	Group A subgroups	Limits Min	Limits Max	Unit
Propagation delay 16-17 from (input): Clock S_1, S_0 = HL to (output): Y	t_{pd16}	See figures 4 and 5, $C_L = 50$ pF	9, 10, 11		53	ns
to (output): C_{n+4}	t_{pd17}				58	ns
Minimum clock low time	t_{CL}		9, 10, 11	20		ns
Minimum clock high time	t_{CH}		9, 10, 11	20		ns

1/ Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

2/ Apply GND to C_n, D_0, D_1, D_2, and D_3. Other inputs high. All outputs open. Measured after low to high clock transition.

Case R



NOTE: Pin 1 is marked for orientation.

FIGURE 1. Terminal connections.

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Address selection

S_1	S_0	Source for Y outputs	Symbol
L	L	Microprogram counter	μPC
L	H	Address/holding register	AR
H	L	Push/pop stack	STKO
H	H	Direct inputs	D_i

Output control

$\overline{\text{ZERO}}$	$\overline{\text{OE}}$	Y_i
X	H	Z
L	L	L
H	L	H
H	L	Source selected by S_0, S_1

Synchronous stack control

$\overline{\text{FE}}$	PUP	Push/pop stack change
H	X	No change
L	H	Increment stack pointer, then push current PC onto STKO
L	L	Pop stack (decrement stack pointer)

H = High
L = Low
X = Don't care
Z = High impedance

FIGURE 2. Truth tables.

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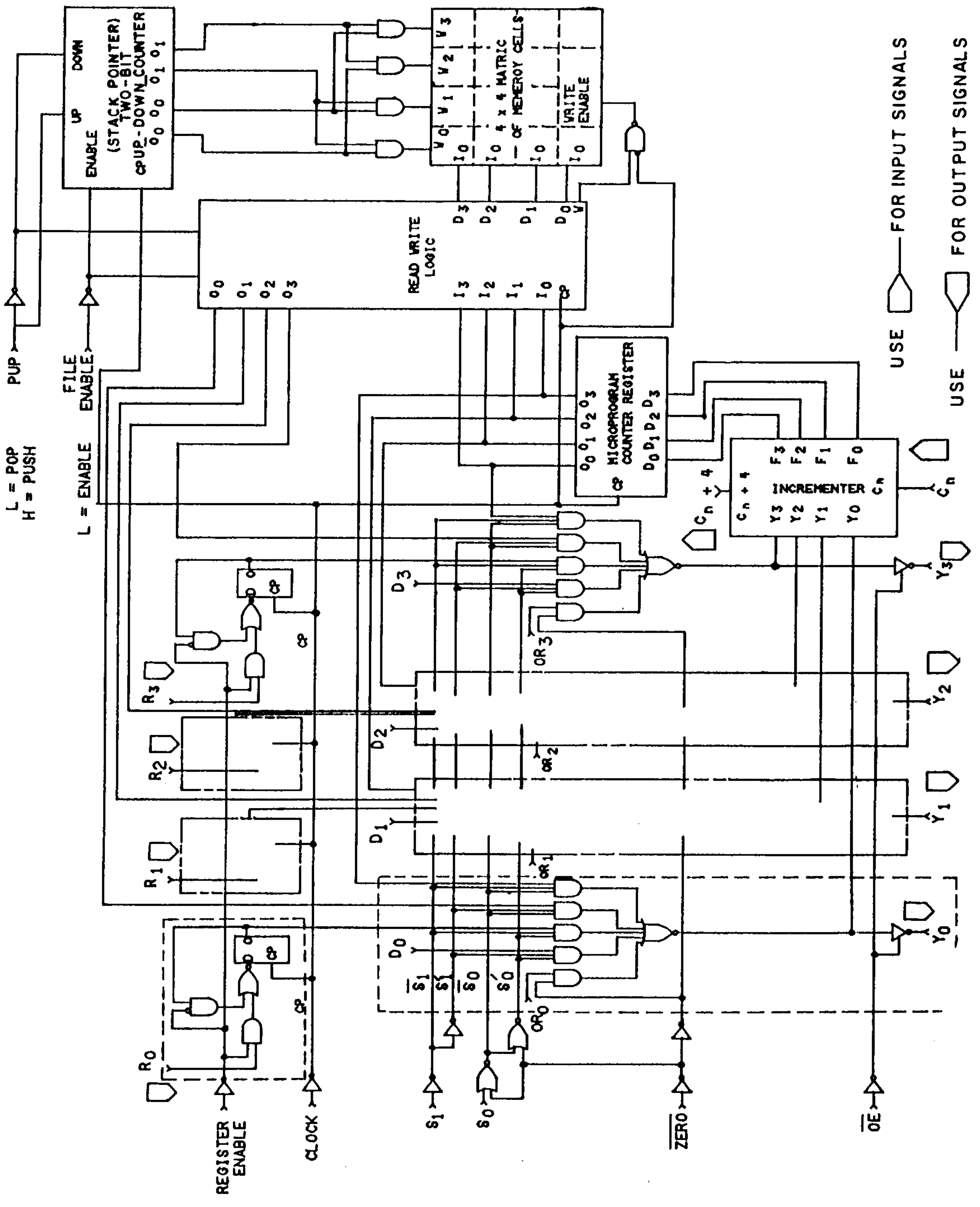

NOTE: R_i and D_i connected together and OR_i removed.

FIGURE 3. Microprogram sequence logic diagram.

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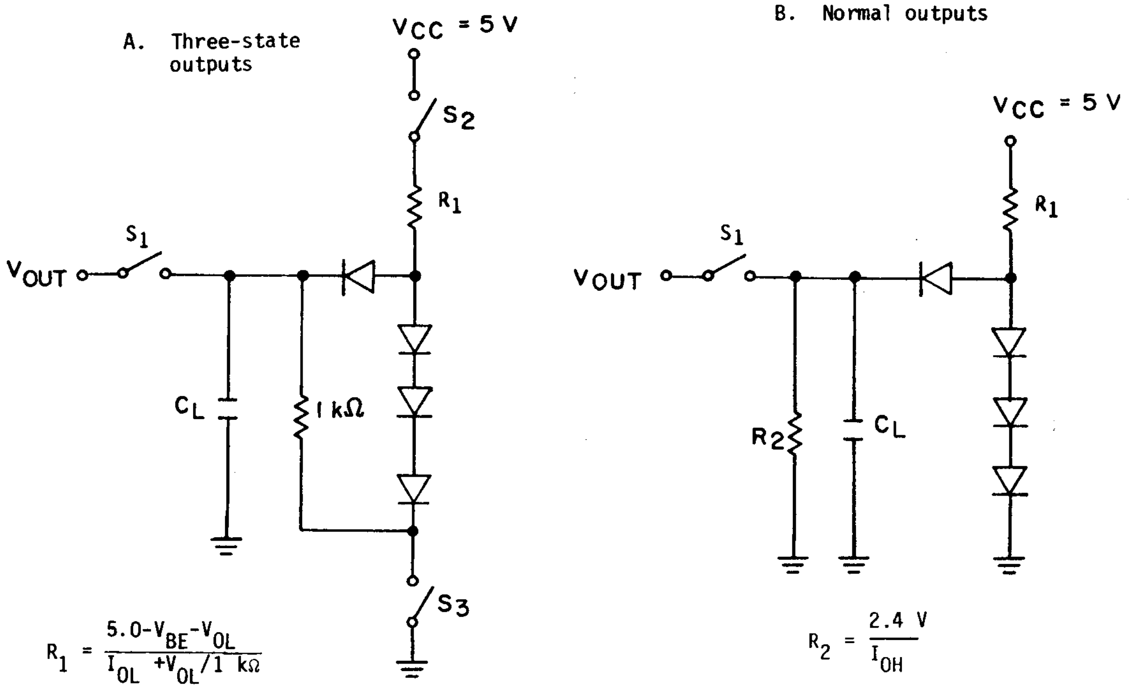

A. Three-state outputs

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/1\ \text{k}\Omega}$$

B. Normal outputs

$$R_2 = \frac{2.4\ \text{V}}{I_{OH}}$$

$$R_1 = \frac{5.0 - V_{BE} - V_{OL}}{I_{OL} + V_{OL}/R_2}$$

Test output loads

Pin no.	Pin label	Test circuit	R1	R2
12-15	Y_{0-3}	A	220	1 kΩ
18	C_{n+4}	B	220	2.4 kΩ

NOTES:
1. C_L = 50 pF includes scope probe, wiring and stray capacitances without device in test fixture.
2. S_1, S_2, and S_3 are closed during function tests all and AC test except output enable tests.
3. S_1 and S_3 are closed while S_2 is open for t_{pd10} high test. S_1 and S_2 are closed while S_3 is open for t_{pd10} low test.
4. C_L = 5.0 pF for output disable tests.

FIGURE 4. Switching test circuits.

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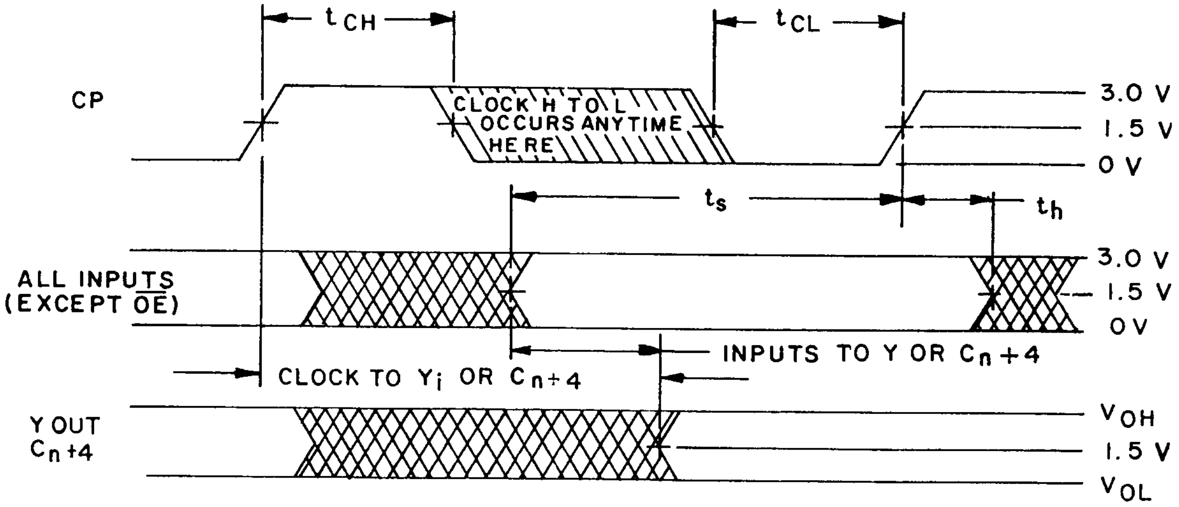

FIGURE 5. Switching waveforms.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

   (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

   (2) $T_A = +125^\circ C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 shall verify the truth table specified on figure 2.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

   (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

   (2) $T_A = +125^\circ C$, minimum.

   (3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Pin descriptions.

Name	I/O	Description
S_1, S_0	I	Control lines for address source selection.
$\overline{FE}$, PUP	I	Control lines for push/pop stack.
$\overline{RE}$	I	Enable line for internal address register.
$\overline{ZERO}$	I	Logic and input on the output lines.
$\overline{OE}$	I	Output enable. When $\overline{OE}$ is high, the Y outputs are off (high impedance).
C_n	I	Carry-in to the incrementer.
D_i	I	Direct inputs to the multiplexer.
CP	I	Clock input to the AR and μPC register and push/pop stack.
Y_i	0	Address outputs from device (address inputs to control memory).
$C_n + 4$	0	Carry out from the incrementer.

6.5 Approved sources of supply. Approved sources of supply are listed herein. Additional sources will be added as they become available. The vendors listed herein have agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor 1/ similar part number
8602801RX	34335	AM2911A/BRA
	50088	TS2911AMCB/C
	50088	TS2911AMJB/C

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

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Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Incorporated 901 Thompson Place P. O. Box 3453 Sunnyvale, CA 94088
50088	Thomson Components-Mostek Corporation 1310 Electronics Drive Carrollton, TX 75006

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