

8-BIT NMOS D/A CONVERTER

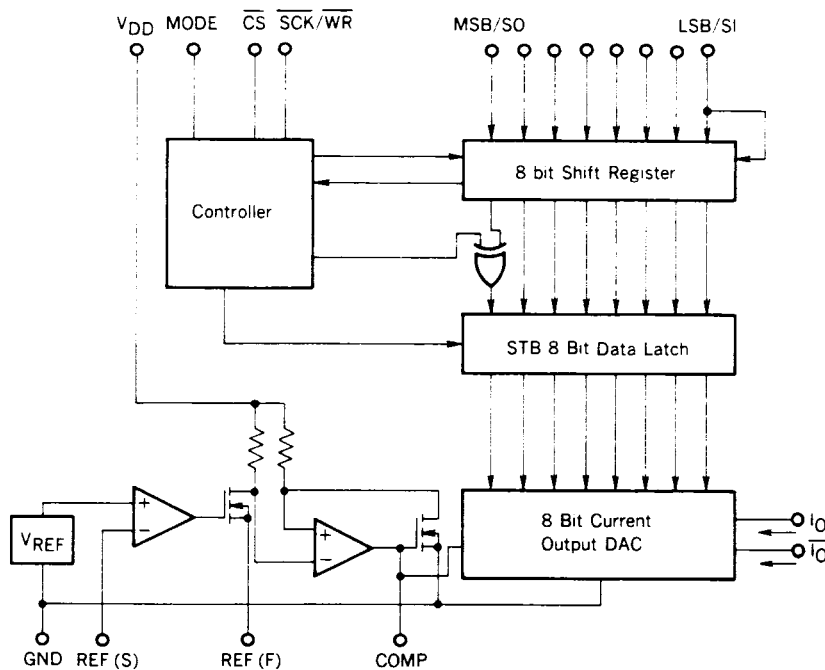
The  $\mu$ PD7011 is a low cost 8-bit NMOS digital-to-analog converter using Enhancement Depletion (ED) technology. The  $\mu$ PD7011 features single +5 V power supply operation and on board voltage reference.

The serial interface option allows easy interface to the  $\mu$ COM-87, and -75 series of single chip microcomputers and the  $\mu$ PD7720 Signal Processing chip (SPI). In parallel mode the  $\mu$ PD7011 is easily connected to the 8080 and 8085 type bus structures by the bus interface facilities.

FEATURES

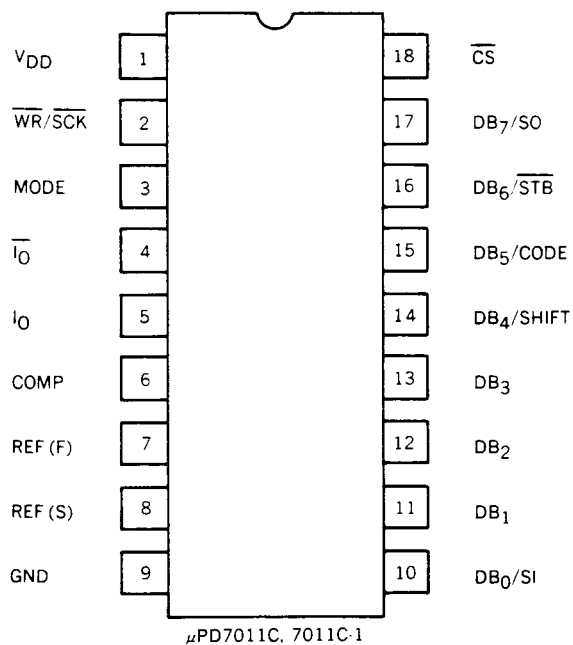
- E/D NMOS monolithic
- Internal voltage reference
- Serial interface with  $\mu$ COM-87, -75 and  $\mu$ PD7720 (SPI)
- Bus interface with 8080 and 8085A-2
- Pure binary and 2's complement code available in serial mode
- Two performance ranges linearity error:  $\mu$ PD7011C, 1 LSB;  $\mu$ PD7011C-1, 1/2 LSB
- Single +5 V power supply
- 18-pin plastic DIP (300 mil)

BLOCK DIAGRAM



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CONNECTION DIAGRAM (Top View)



ABSOLUTE MAXIMUM RATINGS ( $T_a = 25^\circ\text{C}$ )

Operating Temperature	-20 to +70	$^\circ\text{C}$
Storage Temperature	-65 to +150	$^\circ\text{C}$
Power Supply Voltage	-0.3 to +7.0	V
All Input Voltages	-0.3 to $V_{DD} + 0.3$	V
Power Dissipation	300	mW
SO Pin Pull-up Voltage	$V_{DD} + 0.3$	V
$I_O/\bar{I}_O$ Output Pull-up Voltage	+10	V

**RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = +25 °C)**

PARAMETER	SYMBOL	LIMITS			UNIT
		MIN.	TYP.	MAX.	
Supply Voltage	V <sub>DD</sub>	4.75	5.0	5.25	V
Reference Current	I <sub>REF</sub>	225	250	275	μA
Full-Scale Current	I <sub>FS</sub>	0.9	1.0	1.1	mA
Reference Force Terminal Voltage	V <sub>REF(F)</sub>	2.65	2.7	2.75	V
Low-Level Logic Input	V <sub>IL</sub>	0		0.8	V
High-Level Logic Input	V <sub>IH</sub>	2.0		V <sub>DD</sub>	V
Analog Output Pull-up Voltage		2.4		3.0	V
SO Pin 17 Output Pull-up Voltage			V <sub>DD</sub>		V
Frequency Compensation Capacitor (See Note)	C <sub>COMP</sub>	0.01	0.1	1.0	μF

**Note:** Using a frequency compensation capacitor larger than 1 μF will promote low noise operation of the μPD7011C. However, the turn-on time at initial power on will increase.

DC CHARACTERISTICS (V<sub>DD</sub> = 5±0.25 V, T<sub>a</sub> = 25 °C, I<sub>FS</sub> = 1 mA, C<sub>COMP</sub> = 0.1 μF)

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Resolution		8	8	8	Bits	-20 °C to +70 °C
Nonlinearity, 7011C-1	NL		0.25	0.5	LSB	-20 °C to +70 °C
Nonlinearity, 7011C	NL		0.5	1	LSB	-20 °C to +70 °C
Differential Nonlinearity	DNL		0.1	1.0	LSB	-20 °C to +70 °C
Zero-Scale Error				0.5	LSB	-20 °C to +70 °C
Zero-Scale Symmetry		-1.5	-1.0	-0.5	LSB	Note 1
Gain Error, 7011C-1				3	%FSR	
Gain Error, 7011C				5	%FSR	Note 2
Full-Scale Symmetry		-1.5	-1.0	-0.5	LSB	Note 3
Reference Voltage	V <sub>REF(S)</sub>	1.41	2.0	2.59	V	
Power Supply Current	I <sub>DD</sub>		7	13	mA	
Logic Input Leakage	I <sub>I LEAK</sub>		0.1	10	μA	0 ≤ V <sub>I</sub> ≤ V <sub>DD</sub>
Low-Level Output Voltage	V <sub>OL</sub>			0.5	V	SO (Pin 17) I <sub>SINK</sub> = 2 mA
Output Leakage	I <sub>OH</sub>		0.1	10	μA	SO (Pin 17) V <sub>O</sub> = V <sub>DD</sub>
Full-Scale Drift			70		PPM/°C	ΔI <sub>O</sub> (FS)/ΔT
Supply Voltage 7011C-1 Rejection Ratio	SVRR			0.8	%FSR/V	ΔI <sub>O</sub> (FS)/ΔT
Supply Voltage 7011C Rejection Ratio	SVRR			1.2	%FSR/V	ΔI <sub>O</sub> (FS)/ΔV <sub>DD</sub>
Analog Output Compliance		2.4		8.0	V	ΔI <sub>O</sub> (FS) ≤ 1 LSB

- Notes:**
1. Zero-scale symmetry is defined as follows:  
 $255(I_{O(ZS)} - \overline{I_{O(ZS)}})/I_{O(FS)}$
  2. Gain error is defined as follows:  
 $100(I_{O(FS)} \times 256/255 - 4I_{REF})/4I_{REF}$
  3. Full-scale symmetry is defined as follows:  
 $255(I_{O(ZS)} - \overline{I_{O(ZS)}})/I_{O(FS)}$

AC RECOMMENDED CONDITIONS ( $T_a = 25\text{ }^\circ\text{C}$ ,  $V_{DD} = 5\pm 0.25\text{ V}$ , Note 1)

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Serial Mode						
Serial Clock Setup Time	t <sub>SKCS</sub>	30			ns	$\overline{\text{SCK}} \uparrow \rightarrow \overline{\text{CS}} \downarrow$
CS Setup Time	t <sub>SCSK</sub>	300			ns	$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{SCK}} \uparrow$
Data Setup Time	t <sub>SIK</sub>	120			ns	$\text{SI} \rightarrow \overline{\text{SCK}} \uparrow$
Data Hold Time	t <sub>HKI</sub>	50			ns	$\overline{\text{SCK}} \uparrow \rightarrow \text{SI}$
High-Level Serial Clock Pulse Width	t <sub>WHK</sub>	300			ns	
Low-Level Serial Clock Pulse Width	t <sub>WLK</sub>	300			ns	
Strobe Hold Time	t <sub>HKST</sub>	100			ns	$\overline{\text{SCK}} \uparrow \rightarrow \overline{\text{STB}} \uparrow$
High-Level Strobe Pulse Width	t <sub>WHST</sub>	200			ns	
Low-Level Strobe Pulse Width	t <sub>WLST</sub>	200			ns	
Chip Select Hold Time	t <sub>HKCS</sub>	0			ns	$\overline{\text{SCK}} \uparrow \rightarrow \overline{\text{CS}} \uparrow$
Serial Clock Hold Time	t <sub>HCSK</sub>	100			ns	$\overline{\text{CS}} \uparrow \rightarrow \overline{\text{SCK}} \downarrow$
Strobe Setup Time	t <sub>SSTCS</sub>	300			ns	$\overline{\text{STB}} \uparrow \rightarrow \overline{\text{CS}} \downarrow$
Parallel Mode						
Address Setup Time	t <sub>AW</sub>	0			ns	$\overline{\text{CS}} \downarrow \rightarrow \overline{\text{WR}} \downarrow$
Low-Level WR Pulse Width	t <sub>WW</sub>	200			ns	
Address Hold Time	t <sub>WA</sub>	0			ns	$\overline{\text{WR}} \uparrow \rightarrow \overline{\text{CS}} \uparrow$
Data Setup Time	t <sub>DW</sub>	180			ns	$\overline{\text{DB}} \rightarrow \overline{\text{WR}} \uparrow$
Data Hold Time	t <sub>WD</sub>	0			ns	$\overline{\text{WR}} \uparrow \rightarrow \overline{\text{DB}}$

Note:  $t_r, t_f \leq 50\text{ ns}$ .

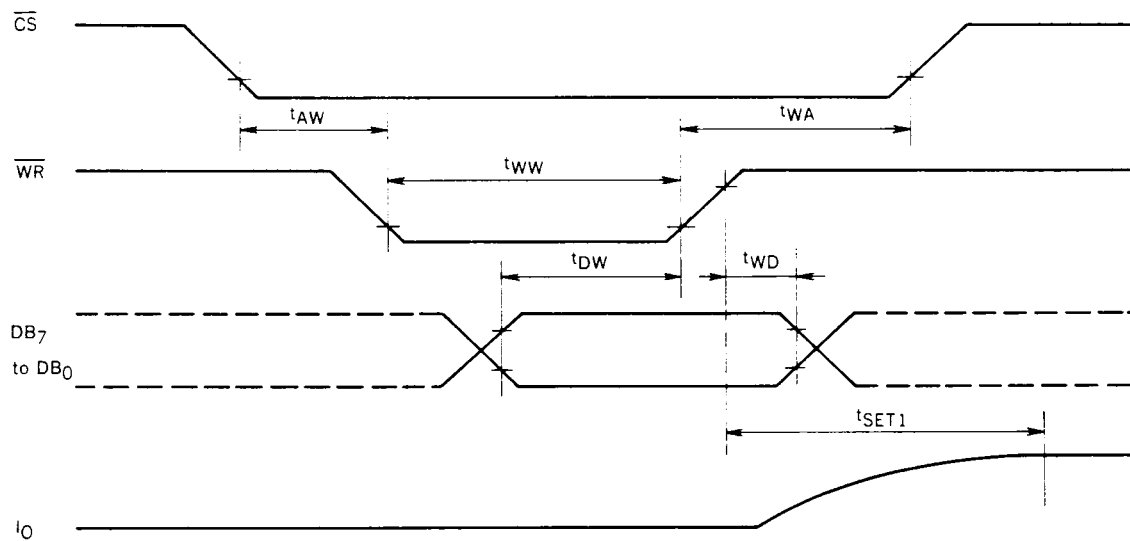
AC CHARACTERISTICS ( $T_a = 25^\circ\text{C}$ ,  $V_{DD} = 5 \pm 0.25\text{ V}$ )

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN.	TYP.	MAX.		
Analog Output Setting Time	tSET1		1	3	μs	Parallel Mode, Note 1
	tSET2		1	3	μs	Serial Mode, Note 2
Serial Data Delay Time	tDKO			450	ns	SCK : - SO, Note 2
Delay Time $T_D$ Floating SO	tFCSO			250	ns	CS * - SO, High Impedance

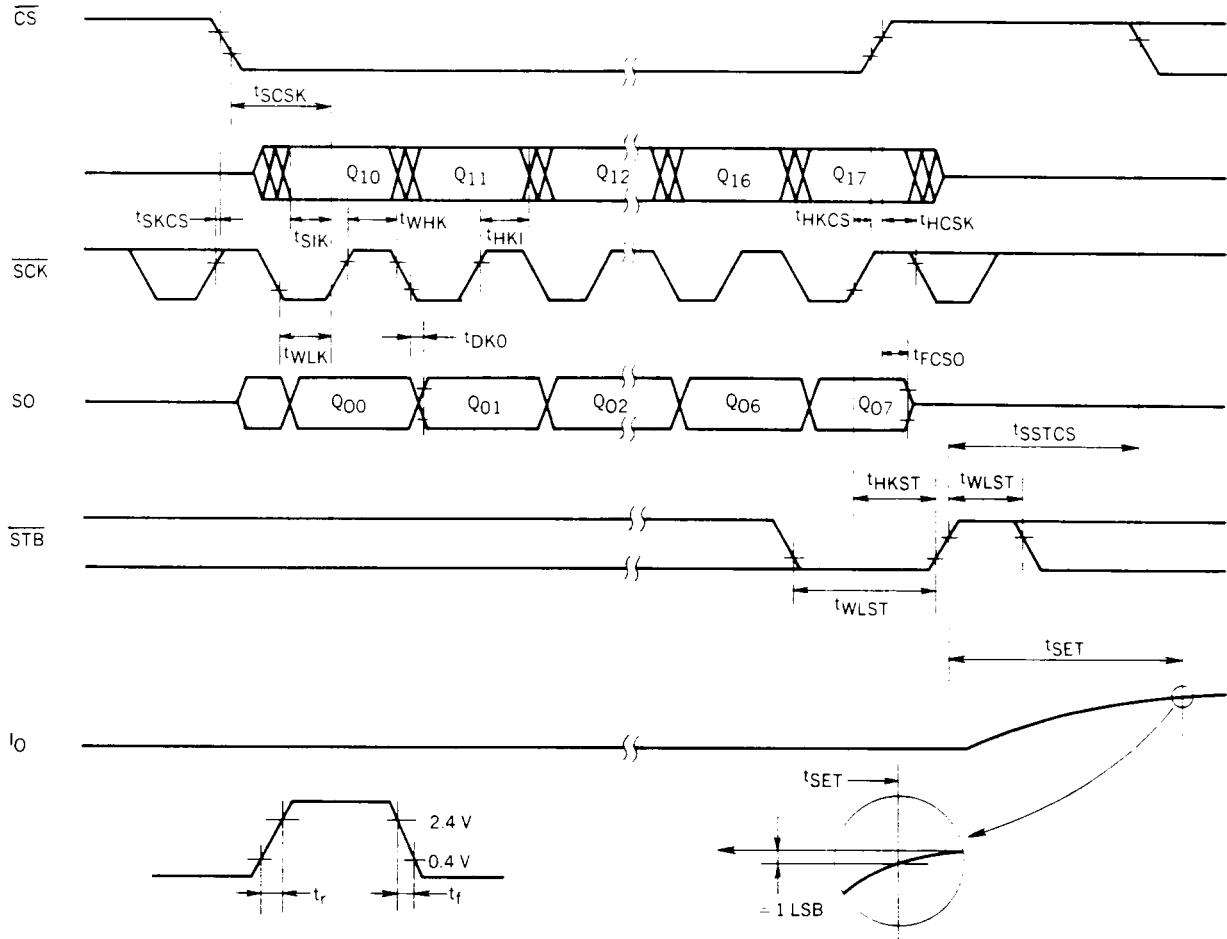
Notes: 1.  $R_L = 2\text{ k}\Omega$ ;  $C_L = 20\text{ pF}$ .  
 2.  $R_L = 2\text{ k}\Omega$ ;  $C_L = 20\text{ pF}$ .

TIMING CHART

1. Parallel Mode (MODE = L)

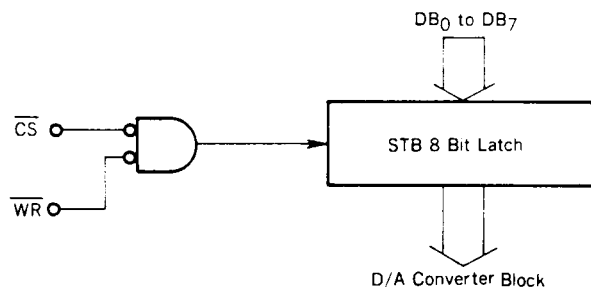


2. Serial Mode (MODE = H)

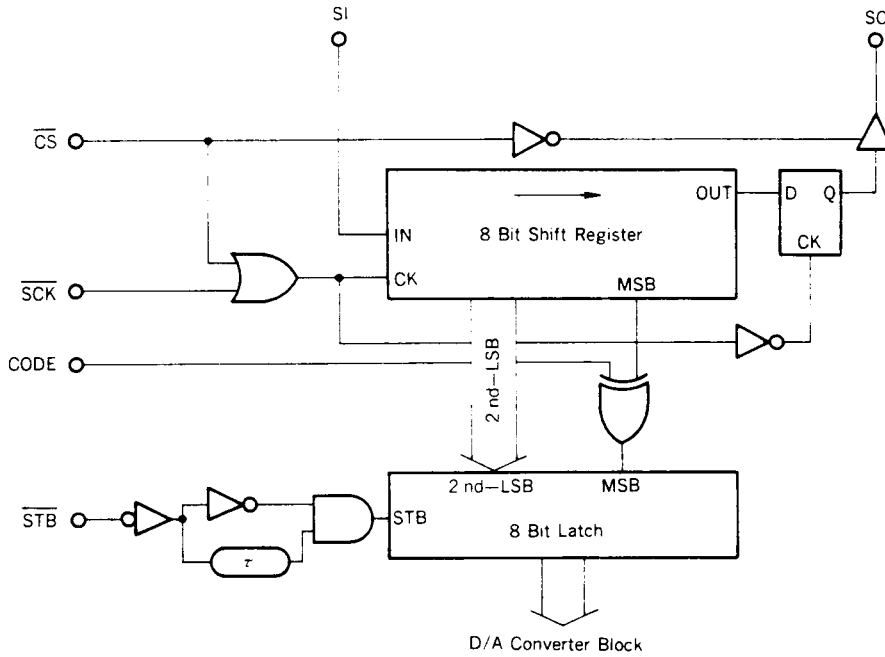


CONTROL BLOCK OPERATION

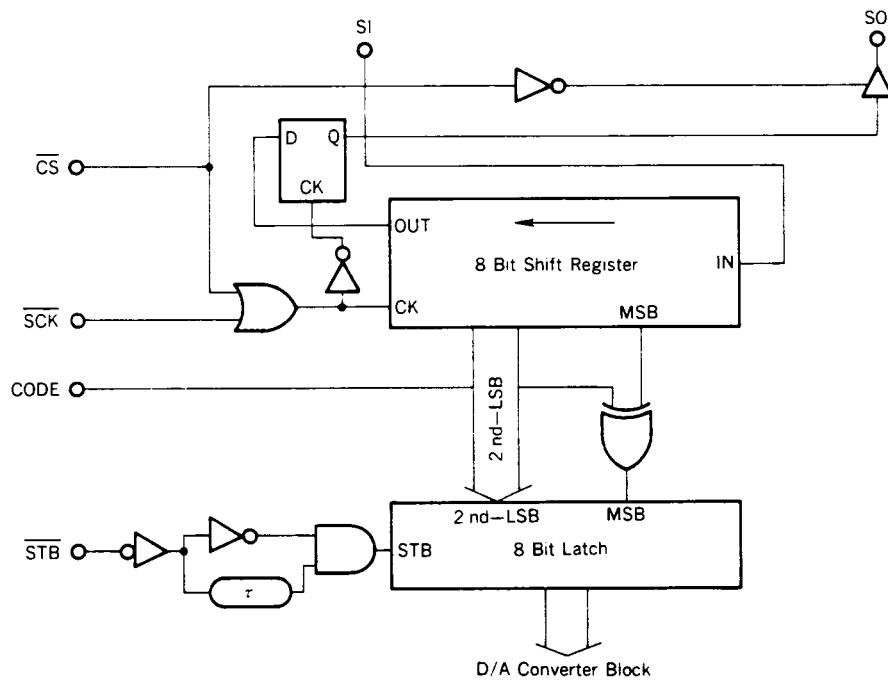
1. Parallel Mode (MODE = LOW)



2. Serial Mode, MSB First (SHIFT = MODE = High)



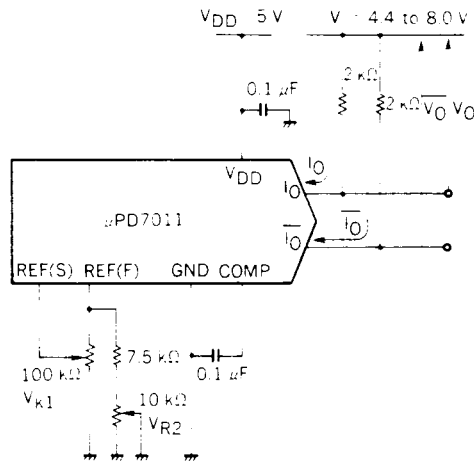
3. Serial Mode, LSB First (SHIFT = Low, MODE = High)





TYPICAL APPLICATIONS

Correction Diagram



( $V_{DD} = 5\text{ V}$ ,  $V^+ = 5\text{ V}$ )

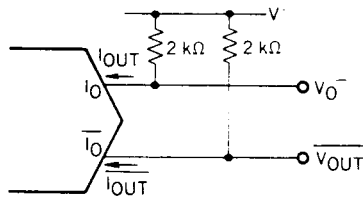
Digital Input		$I_{OUT}$	$\overline{I_{OUT}}$	$V_O(V)$	$\overline{V_O}(V)$
MSB	LSB	(mA)	(mA)		
1	1	0.996	0.004	1.992	0.008
1	1	0.992	0.008	1.984	0.016
⋮	⋮	⋮	⋮	⋮	⋮
1	0	0.504	0.496	1.008	0.992
1	0	0.500	0.500	1.000	1.000
0	1	0.496	0.504	0.992	1.008
⋮	⋮	⋮	⋮	⋮	⋮
0	0	0.004	0.996	0.008	1.992
0	0	0.000	1.000	0.000	2.000

Adjustment Procedure

- a. Set  $V_{REF(F)} = 2.7\text{ V}$  by  $V_{R1}$
- b. After latching full-scale digital input, set  $V_O = 2.0\text{ V}$  by  $V_{R2}$

- Notes:
1. Both  $I_O$  and  $\overline{I_O}$  must use pull-up resistors.
  2. Use resistors of 1 % accuracy.
  3. Capacitive load at  $V_{REF(F)}$  pin should be less than 15 pF.

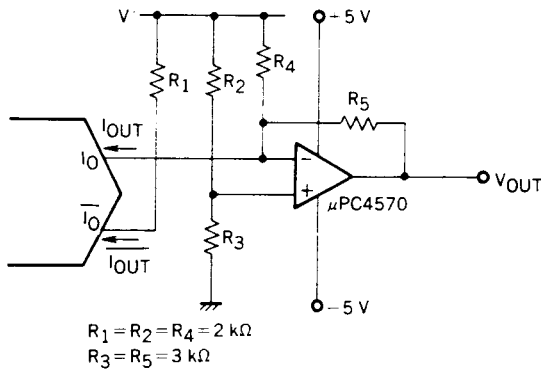
(1)  $V_{OUT} = 3$  to  $5$  V,  $\overline{V_{OUT}} = 5$  to  $3$  V



( $V_{DD} = V^+ = 5$  V)

Digital Input		$I_{OUT}$	$\overline{I_{OUT}}$	$V_{OUT}$	$\overline{V_{OUT}}$
MSB	LSB	(mA)	(mA)	(V)	(V)
1	1	0.996	0.004	3.008	4.992
1	1	0.992	0.008	3.016	4.984
⋮	⋮	⋮	⋮	⋮	⋮
1	0	0.500	0.500	4.000	4.000
⋮	⋮	⋮	⋮	⋮	⋮
0	0	0.004	0.996	4.992	3.008
0	0	0.000	1.000	5.000	3.000

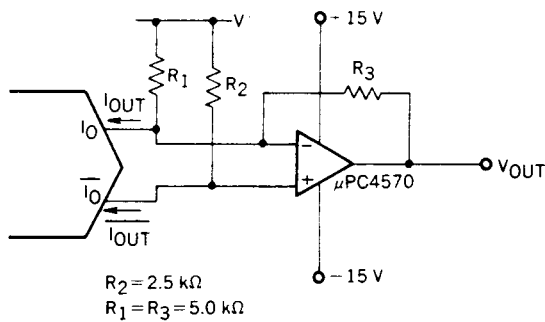
(2)  $V_{OUT} = 0$  to  $3$  V



( $V_{DD} = V^+ = 5$  V)

Digital Input		$I_{OUT}$	$\overline{I_{OUT}}$	$V_{OUT}$
MSB	LSB	(mA)	(mA)	(V)
1	1	0.996	0.004	2.988
1	1	0.992	0.008	2.976
⋮	⋮	⋮	⋮	⋮
1	0	0.500	0.500	1.500
⋮	⋮	⋮	⋮	⋮
0	0	0.004	0.996	0.012
0	0	0.000	1.000	0.000

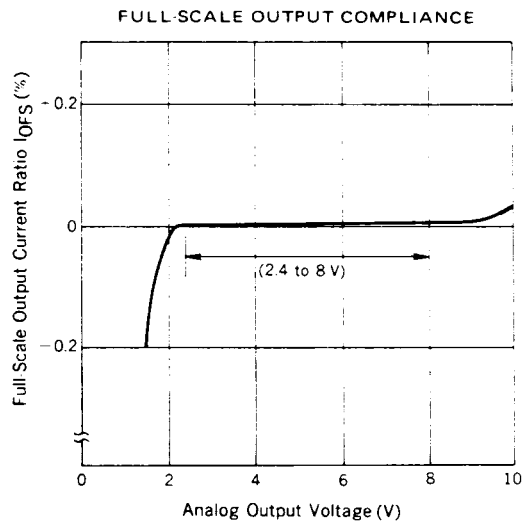
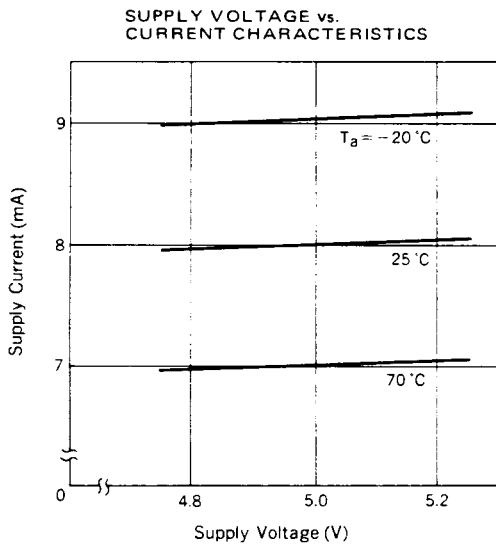
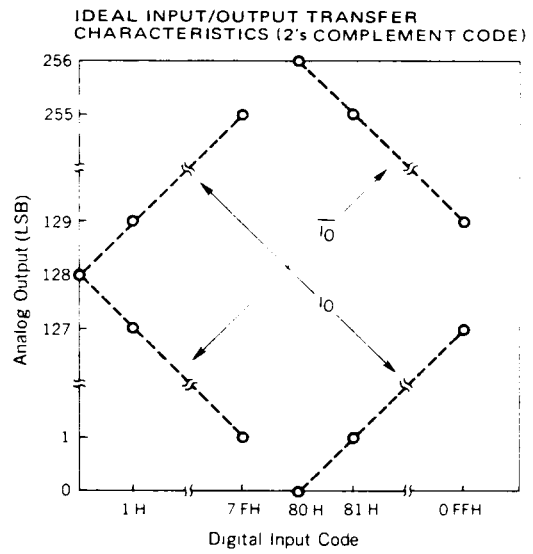
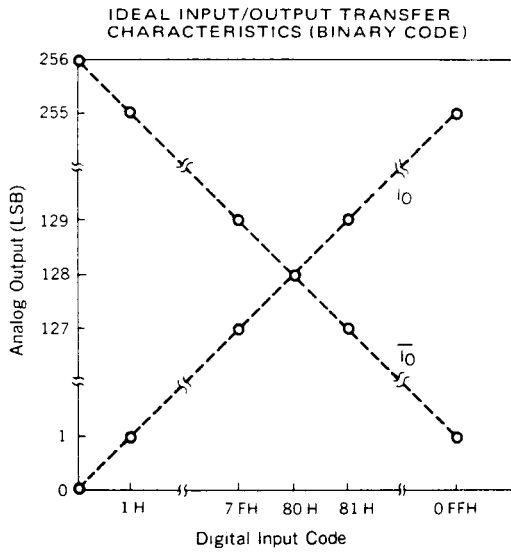
(3)  $V_{OUT} = 0$  to  $10$  V



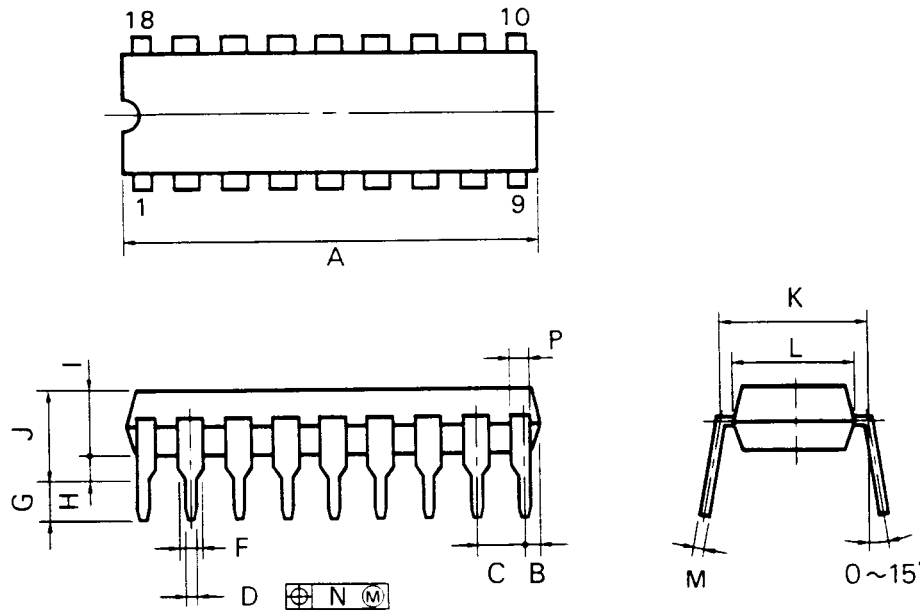
( $V_{DD} = V^+ = 5$  V)

Digital Input		$I_{OUT}$	$\overline{I_{OUT}}$	$V_{OUT}$
MSB	LSB	(mA)	(mA)	(V)
1	1	0.996	0.004	9.96
1	1	0.992	0.008	9.92
⋮	⋮	⋮	⋮	⋮
1	0	0.500	0.500	5.00
⋮	⋮	⋮	⋮	⋮
0	0	0.004	0.996	0.04
0	0	0.000	1.000	0.00

OPERATING CHARACTERISTICS (T<sub>a</sub> = 25 °C)



18PIN PLASTIC DIP (300 mil)



P18C-100-300A.C

NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	22.86 MAX.	0.900 MAX.
B	1.27 MAX.	0.050 MAX.
C	2.54 (T.P.)	0.100 (T.P.)
D	0.50 <sup>+0.10</sup>	0.020 <sup>+0.004</sup>
F	1.2 MIN.	0.047 MIN.
G	3.5 <sup>+0.3</sup>	0.138 <sup>+0.012</sup>
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.4	0.252
M	0.25 <sup>+0.10</sup>	0.010 <sup>+0.004</sup>
N	0.25	0.01
P	1.0 MIN.	0.039 MIN.