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SSI 32H6521
Embedded Servo Controller

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DESCRIPTION

The SSI 32H6521 Embedded Servo Controller is a CMOS monolithic integrated circuit housed in a 44-lead SO and operates on a single +5.0 volt supply. It provides one 10-bit A/D converter with 2.5 µs conversion time, and two 10-bit D/A converters with 2.5 µs digital delay. In addition, it includes bus interface logic to support DSP-based, such as TMS320C25, digital servo applications.

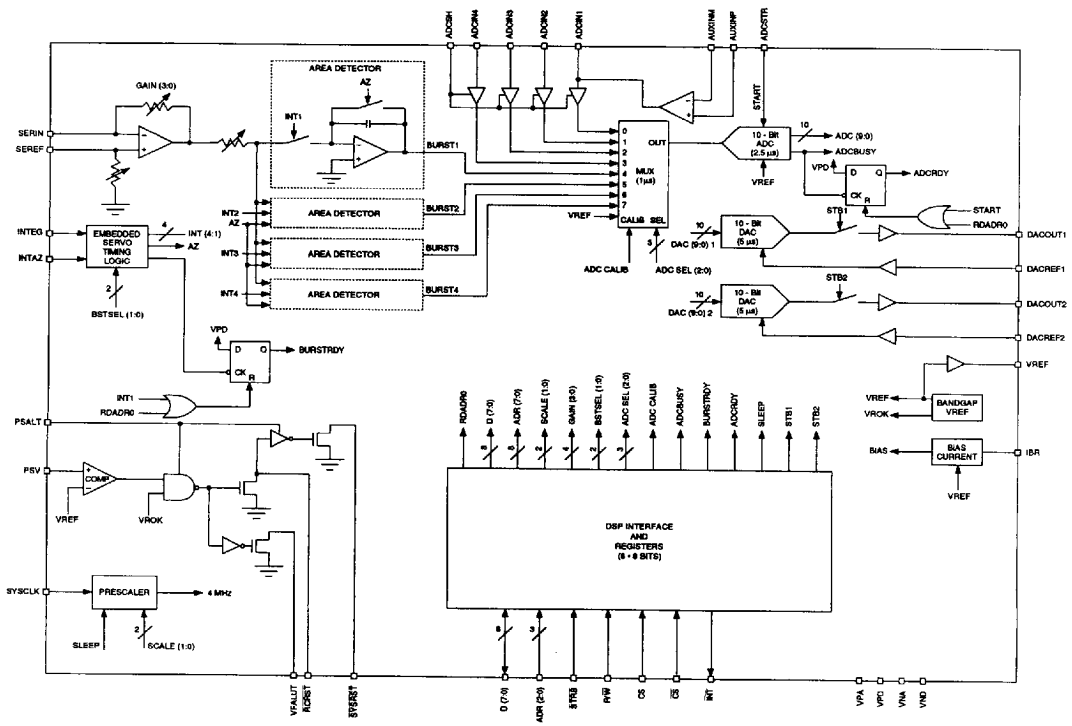
FEATURES

Embedded Servo Burst Processor

- Servo control for Winchester disk drives with embedded servo sectors
- For use in DSP-based digital servo applications
- Pulse area detects and S/H circuits for up to four embedded servo bursts
- Programmable gain adjustment from -2.8 dB to 3.2 dB

(continued)

BLOCK DIAGRAM



FEATURES (continued)

Data Acquisition and DSP Bus Interface

- Bus interface logic to support DSP-based digital servo applications
- Eight internal registers and address decoding
- Two 10-bit D/A converters with 2.5 µs digital delay
- One 8-channel 10-bit A/D converter with 2.5 µs conversion time

General Functions

- Voltage fault detection
- Low power CMOS design

FUNCTIONAL DESCRIPTION

The SSI 32H6521 can be divided into four major sections: embedded servo burst processor, voltage fault detector/logic, data acquisition and DSP bus interface.

EMBEDDED SERVO BURST PROCESSOR

The embedded servo burst processor extracts the head position error information from the embedded servo bursts using an area detection technique. The area detection technique provides improved noise immunity over peak detection. The embedded servo burst processor contains a differential/gain amplifier, four pulse area detectors and required timing logic. First, a full wave-rectified analog signal from a read data channel, such as SSI 32P4622, is provided at SERIN through an external resistor equal to Rint and a DC reference level for the full wave-rectified analog signal at SEREF through another external resistor equal to Rint. To accommodate a wide dynamic range of servo burst amplitudes and process variations of the integration capacitor Cint, the differential signal between SERIN and SEREF is scaled under DSP control. The gain of the differential amplifier ranges from -2.8 dB to 3.2 dB in a step of 0.4 dB, as defined in the SERVO GAIN CONTROL register. The output of the differential/gain amplifier is then provided to four pulse area detectors whose outputs are proportional to the area above the DC reference level during time intervals defined by an external timing source through INTEG. Each area detector applies an on-chip capacitor Cint equal to 10 pF to integrate the incoming pulses during the integration interval and then hold the integrated voltage outputs thereafter. Note that the max ±20% tolerance of on-chip capacitors can be calibrated out by adjusting the gain of the preceding amplifier. Finally, the integrated voltage outputs at BURST1, BURST2, BURST3 and BURST4 are provided to a 10–bit A/D converter under DSP control and will be discharged during a time interval defined by an external timing source through INTAZ. For proper operatons, the time interval defined by the INTAZ must be no less than 0.5 µs and be applied only once per servo frame preceding the integration pulses defined by the INTEG.

Limited timing logic is included to generate all the timing signals required for the embedded servo burst processor, per Figure 1. These timing signals control the integration, sample/hold of the pulse area detectors. The number of embedded servo bursts supported by this circuit are two, three or four. The BSTSEL0 and BSTSEL1 bits in the SERVO CONTROL register configure the internal timing logic to generate a servo burst ready interrupt after the last servo burst is captured.

VOLTAGE FAULT DETECTOR/LOGIC

The voltage fault detector monitors the power supply applied at PSV through an external resistor divider, which defines the trigger level for power supply failure. An open-drain output VFAULT is pulled HIGH by an external resistor when a power supply failure is sensed by the PSV comparator. The user-defined trigger level for voltage failure is applied at PSV. Another open-drain output, opposite logic polarity as the pin VFAULT and with an additional RC delay, is provided at $\overline{\text{SYSRST}}$. The amount of $\overline{\text{SYSRST}}$ delay is determined by an external RC connected to the pin, $\overline{\text{RCRST}}$.

DATA ACQUISITION

The A/D converter is multiplexed to eight different analog inputs by programming the ADC SEL0, ADC SEL1, and ADC SEL2 bits in the ADC ADDRESS register by the DSP. The eight analog inputs multiplexed to the A/D converter are four embedded servo processor outputs at BURST1, BURST2, BURST3 and BURST4 and four external analog inputs through four T/H amplifiers. These T/H amplifiers sample external analog inputs during the time interval defined by an external timing source applied at ADCSH. If the sampling of four external analog inputs is not necessarily synchronized, ADCSH must be tied to HIGH. The A/D

conversions on these external analog inputs are always referenced to the internal voltage reference at 2.23 volts. An operational amplifier with uncommitted inputs is provided to implement a level shifting function for the external analog input applied to AUXINP. The output of the operational amplifier is tied to ADCIN1.

The A/D converter starts to acquire a new analog input whenever the conversion is completed. A minimum of 1 µs is required to acquire an analog input to the A/D converter. Actual conversion is started by reading the A/D MSB register or by an external timing source applied to ADCSTR. The A/D address lines ADC SEL0, ADC SEL1, and ADC SEL2 will be incremented by one after the A/D conversion is started. The automatic increment of the address lines is employed to eliminate repetitive write operations by the DSP to the ADC ADDRESS register required for converting the consecutive analog inputs.

The A/D converter runs synchronously with the internal 4 MHz clock which is used for various circuits on the SSI 32H6521 and divided down from the system clock SYSCLK by a prescaler. Therefore there would be a maximum of 0.25 µs of latency between a conversion request and the actual start of the conversion. The output is coded in 2's complement.

Do not read from the device during A/D conversion. Digital noise generated by the read cycle may be coupled into the A/D converter. Coupled noise can prevent 10-bit accuracy.

Similarly, the D/A converters run synchronously with the internal 2 MHz clock and the conversion is started by writing to the corresponding D/A input register. The output of the first D/A converter is referenced to an external analog input, DACREF1 and the output of the second D/A converter is referenced to an external analog input, DACREF2. In the "normal" mode when STBEN1 (STBEN2) bit in the ADC ADDRESS register is reset, the D/A output will be automatically applied to DACOUT1 (DACOUT2) during the conversion. In the "strobe" mode, the D/A output will be applied to DACOUT1 (DACOUT2) at the falling edge of $\overline{RD}$ for a read to the corresponding D/A MSB DATA register.

DSP BUS INTERFACE

The SSI 32H6521 provides interface logic for a direct connection to TMS320CXX DSP. It contains an 8-bit data bus and 3 address lines for communicating with eight internal registers. Bus control signals are $\overline{CS}$, CS, $\overline{STRB}$ and R/$\overline{W}$. The address lines are internally latched when the device is selected ($\overline{CS}$ active low and CS active high). The timing requirements for the DSP bus interface are depicted in Figure 2.

Avoid accessing this device while the servo burst capture, D/A or A/D conversion is in progress. Digital bus noise will couple into the signal path through the substrate and corrupt the signal. To maintain signal integrity, it is recommended that read operations be avoided during servo burst capture, and sufficient time be allowed for the last A/D conversion to be completed.

REGISTER DESCRIPTIONS

The 32H6521 contains eight 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 3-bit register address which is latched from inputs at ADR0(LSB), ADR1, and ADR2(MSB) while the device is selected. The registers 0, 2, and 3 are read/write memory, and the registers 1, 4, 5, 6, and 7 are write only memory. The registers are summarized in Table 2.

TABLE 2: Register Descriptions

ADDRESS	TYPE	REGISTER NAME
0	R/W	INTERRUPT MASK/STATUS
1	W	SERVO GAIN CONTROL & PRESCALER
2	R/W	ADC LSB DATA
3	R/W	ADC ADDRESS & MSB DATA
4	W	DAC1 LSB DATA
5	W	DAC1 MSB DATA
6	W	DAC2 LSB DATA
7	W	DAC2 MSB DATA

INTERRUPT MASK/STATUS REGISTER

Address: 0
Access: Read/Write
Reset: Bit 0, 1 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0	BURST INT	When set HIGH, interrupt is enabled on the embedded servo position bursts ready.
1	ADC INT	When set HIGH, interrupt is enabled on the completion of the A/D conversion.
2 - 7		Unused.

Register contents when Read:

BIT	NAME	DESCRIPTION
0	BURSTRDY	Active high indicates that the embedded servo bursts are ready.
1	ADCRDY	Active high indicates that the A/D conversion is completed.

Each interrupt event status will be reset after the DSP reads this register. The interrupt control register determines if the event will actually cause a latched assertion of the DSP signal $\overline{INT}$.

SERVO GAIN CONTROL & PRESCALER REGISTER

Address: 1
Access: Write
Reset: 00

BIT	NAME	DESCRIPTION
0 1	SCALE0 SCALE1	SYSCLK Prescaler. To accommodate different system clocks, the prescaler selects a proper divider to generate a fixed clock at 4 MHz per table below:

SCALE1	SCALE0	SYSCLK(MHz)	Divider
0	0	16	4
0	1	12	3
1	0	8	2
1	1	4	1

BIT	NAME	DESCRIPTION
2 3 4 5	GAIN0 GAIN1 GAIN2 GAIN3	Servo Burst Amplitude Gain Select. These four bits define the gain setting for the differential/gain amplifier per table below:

GAIN3	GAIN4	GAIN3	GAIN0	Gain, dB
0	0	0	0	-2.8
0	0	0	1	-2.4
0	0	1	0	-2.0
0	0	1	1	-1.6
0	1	0	0	-1.2
0	1	0	1	-0.8
0	1	1	0	-0.4
0	1	1	1	+0.0
1	0	0	0	+0.4
1	0	0	1	+0.8
1	0	1	0	+1.2
1	0	1	1	+1.6
1	1	0	0	+2.0
1	1	0	1	+2.4
1	1	1	0	+2.8
1	1	1	1	+3.2

BIT	NAME	DESCRIPTION
6 7	BSTSEL0 BSTSEL1	Burst Number Select. These two bits define the number of embedded servo bursts per sector.

BSTSEL1	BSTSEL0	# of Bursts
0	0	2
0	1	3
1	0	4

ADC LSB DATA REGISTER

Address: 2
Access: Read/Write
Reset: Bit 5, 6, 7 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0 - 4		Unused.
5	SLEEP	Power-down Mode Enable. When set HIGH, the device is in the sleep mode where all analog circuitry are de-biased, the clock is disabled, and the bandgap voltage, reference voltage fault logic and processor interface stay active.
6	STBEN1	When set HIGH, the analog output of the DAC1 is transferred and held onto DACOUT1.
7	STBEN2	When set HIGH, the analog output of the DAC2 is transferred and held onto DACOUT2.

Register contents when Read:

Description: After A/D conversion, the least significant 2 bits of the 10-bit digital word is stored into the register.

0 - 5		Unused. Logic LOW is provided to these bits.
6,7	ADC0, ADC1	The LSB 2 bits of the A/D converter output in 2's complement format.

ADC ADDRESS & MSB DATA REGISTER

Address: 3
Access: Read/Write
Reset: Bits 0, 1, 2, and 3 only

Description: When Written, the least significant 3 bits of the register define the analog input to the 10-bit A/D converter. After conversion, the most significant 8 bits of the 10-bit digital word is stored into the register.

Register contents when Written:

0 1 2	ADC SEL0 ADC SEL1 ADC SEL2	A/D Converter Input Select. These 3 bits define the analog input to the A/D converter per table below:

BIT2	BIT1	BIT0	ADC INPUT
0	0	0	ADCIN1
0	0	1	ADCIN2
0	1	0	ADCIN3
0	1	1	ADCIN4
1	0	0	BURST1
1	0	1	BURST2
1	1	0	BURST3
1	1	1	BURST4

ADC ADDRESS & MSB DATA REGISTER (continued)

BIT	NAME	DESCRIPTION
3	ADC CALIB	When set HIGH, VREF (2.23 volts) is applied to the A/D converter input.
4 - 7		Unused.

Register contents when Read:

0 - 7	ADC2 - 9	The MSB 8 bits of the A/D converter output in 2's complement. ADC9 is the sign bit.

DAC1 LSB DATA REGISTER

Address: 4
Access: Write
Reset: 00

0 - 5		Unused.
6, 7	DAC0, DAC1	The LSB 2 bits to the DAC1 in 2's complement.

DAC1 MSB DATA REGISTER

Address: 5
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC1 in 2's complement, DAC9 is the sign bit.

DAC2 LSB DATA REGISTER

Address: 6
Access: Write
Reset: 00

0 - 5		Unused.
6 7	DAC0, DAC1	The LSB 2 bits to the DAC2 in 2's complement.

DAC2 MSB DATA REGISTER

Address: 7
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC2 in 2's complement. DAC9 is the sign bit.

PIN DESCRIPTION

POWER SUPPLIES

NAME	DESCRIPTION
VPA	Analog +5V supply.
VPD	Digital +5V supply. It must be shorted to analog +5V supply externally.
VNA	Analog ground.
VND	Digital ground. It must be shorted to analog ground externally.
PSALT	Alternate Voltage Supply to power the voltage fault logic during a voltage fault. This power supply should be taken from the system +5V supply through a Schottky diode and be connected to a capacitor, which is used to hold up PSALT briefly during a voltage fault.

EMBEDDED SERVO BURST PROCESSOR

NAME	TYPE	DESCRIPTION
SERIN	I	Servo Burst Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts.
SEREF	I	Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN.
INTEG	I	Pulse Area Detector Enable - This TTL compatible input, when HIGH, activates the pulse area detectors.
INTAZ	I	Integrator Capacitor Reset - This TTL compatible input, when HIGH, discharges the holding capacitors, Cint.

VOLTAGE FAULT DETECTION

PSV	I	Fault Voltage Comparator Input - A voltage input for the low voltage comparator. This input should be connected to an external resistor divider. The resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.23 volts.
VREF	O	VREF Output - A buffered voltage reference at 2.23 volts.
IBR	O	Pin for connection to an external resistor (from GND) to establish a reference current for bias currents required for analog circuits.
VFAULT	O	Voltage Fault Indication - An open-drain output which is pulled HIGH when a supply voltage fault is detected.
$\overline{\text{SYSRST}}$	O	Reset Output - An open-drain output which is pulled LOW with an amount of delay determined by an external RC connected to the pin RCRST when a supply voltage fault is detected.
$\overline{\text{RCRST}}$	O	Pin for connection to an external RC to implement the delay of active LOW $\overline{\text{SYSRST}}$.

DSP BUS INTERFACE

NAME	TYPE	DESCRIPTION
D0 - D7	I/O	8-Bit Bidirectional Data Bus. - These bidirectional data pins are in the high impedance state when the device is not selected
ADR0 - ADR2	I	3-bit address lines to select an internal register for I/O.
$\overline{STRB}$	I	Data Strobe. - The data on the data bus is written to the addressed register at the rising edge of $\overline{STRB}$.
R/$\overline{W}$	I	READ/$\overline{WRITE}$ Enable. - When low, the data is to be written to the addressed register. Otherwise, the contents of the addressed register are placed on the data bus.
$\overline{CS}$, CS	I	2-Bit Chip Select Lines. - This device is selected when $\overline{CS}$ is low and CS is high.
$\overline{INT}$	O	Interrupt - An open-drain output which signals the DSP to respond to the device. It is released when all pending interrupts have been serviced by the DSP.
SYSCLK	I	System Clock Input - A TTL compatible input for the system clock which is divided down with a prescaler to generate internal timing signals.

DATA ACQUISITION

DACOUT1	O	DAC1 Output - A 10-bit D/A output which converts a digital word from the DSP into an analog signal.
DACREF1	I	DAC1 Output Reference - An external analog input to be provided to DAC1 as a reference voltage for DACOUT1.
DACOUT2	O	DAC2 Output - A 10-bit D/A output which converts a digital word from the DSP into an analog signal.
DACREF2	I	DAC2 Output Reference - An external analog input to be provided to DAC2 as a reference voltage for DACOUT2.
ADCIN1 ADCIN2 ADCIN3 ADCIN4	I	External A/D inputs.
ADCSH	I	A/D Analog Sampling Input Strobe - A TTL compatible control signal. During active HIGH, four track/hold amplifiers prior to the A/D converter will sample external A/D analog inputs.
ADCSTR	I	A/D Conversion Start Strobe - A TTL compatible control signal whose rising edge triggers the start of the A/D conversion.
AUXINP	I	Level Shifter Noninverting Input - Noninverting input to the level-shifting amplifier.
AUXINM	I	Level Shifter Inverting Input - Inverting input to the level-shifting amplifier.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

SYMBOL	PARAMETER	RATING
VDD	Supply voltage applied at VPA, VPD	-0.3 to 7.0V
GND	Signal ground applied at VNA, VND	0.0V
PSALT	Supply voltage applied at PSALT	-0.3 to 7.0V
VIND	Digital input voltages	-0.3 to VDD + 0.3V
VINA	Analog input voltages	-0.3 to VDD + 0.3V
Tstg	Storage temperature	-65 to 150 °C
Tl	Lead temperature (10 seconds)	300 °C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD	Supply voltage applied at VPA, VPD		4.5		5.25	V
GND	Signal ground applied at VNA, VND		0.0		0.0	V
PSALT	Supply voltage applied at PSALT		3.0		6.0	V
TA	Ambient temperature		0.0		70.0	°C
Fc	System clock (16MHz, Max)				±0.1	%
Tc	System clock duty cycle		40		60	%
CLOAD	Capacitive load on digital outputs				50	pF
RBIAS	Bias resistor (22.6 kΩ)				±1	%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IDD	Supply current Normal mode Sleep mode	VDD = 5.25V	 - -		 25 5	 mA mA
Voh	Output logic "1" voltage	Ioh = -0.4mA, VDD = 4.5V	2.4		-	V
Vol	Output logic "0" voltage	Iol = 1.6mA, VDD = 4.5V	-		0.4	V
Vih	Input logic "1" voltage	VDD = 4.5V	2.0		-	V
Vil	Input logic "0" voltage	VDD = 4.5V	-		0.8	V
Iih	Input logic "1" current	Vih = 5.25V, VDD = 5.25V	-		1	µA
Iil	Input logic "0" voltage	Vil = 0.0, VDD = 5.25V	-		-1	µA
Cin	Input capacitance		-		10	pF

FUNCTIONAL CHARACTERISTICS

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

SERIN with respect to GND		1.0	-	VDD	V
SEREF with respect to GND		1.0		3.0	V
SERIN input voltage	Servo gain = -2.8 dB	0.0	-	1.5	Vp
swing with respect to SEREF	Servo gain = 0 dB	0.0	-	1.0	Vp
Servo burst frequency		1.0	-	5.0	MHz
Input impedance at	Servo gain = -2.8 dB	15	20	25	kΩ
SERIN, SEREF	Servo gain = 0 dB	18	24	30	kΩ
Cin = 2 pF nominal	Servo gain = 3.2 dB	21	28	35	kΩ
C_{int} integration time, t_{INT}	Integrates to within 1% of	1.0			µs
C_{int} discharge time, t_{DISCH}		0.5			
Burst integration timing window separation, t_{NON}		0.1			µs
Servo burst ready, t_{RDY}		0.1			µs

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Servo channel ouput when SERIN shorted with SEREF	SEREF = 2V R_{int} = 63 kΩ	1.45	-	1.75	V
Servo channel gain step size	Guaranteed Monotonic	1.0	1.05	1.1	V/V
Servo channel slope deviation	SERIN from 0.2 V_p to 0.8 V_p R_{int} = 63 kΩ	-	-	±10	mV
Channel mismatch				100	mV

Note: Servo channel includes the servo burst capture circuit, A/D and D/A converters.

VOLTAGE REFERENCE AND VOLTAGE FAULT CIRCUIT

VPA voltage for $\overline{SYSRST}$ & RCRST in operation		2	-	5.25	V
On resistance at RCRST		-	-	100	Ω
RCRST input threshold	PSALT = 3V	0.8	-	1.6	V
IBR voltage with respect to VREF			-	±100	mV
VREF voltage	No load	2.16	2.23	2.30	V
Allowable load at VREF		10		-	kΩ
		-		100	pF
PSV comparator offset			-	±15	mV

A/D INPUT UNCOMMITTED OPERATIONAL AMPLIFIER

AUXINP Input Voltage	With respect to GND	1.25	-	3.25	V
Unit-gain bandwidth		1	-	-	MHz
Input-referred D.C. offset		-	-	±10	mV
Allowable load at ADCIN		5.0	-	-	kΩ
				40	pF

DATA ACQUISITION

A/D Converter

ADCIN full-scale voltage with respect to VREF		-	± (VREF/2)	-	V
Resolution		-	10	-	Bits
Acquisition time		-	1.0		µs
Conversion time		-	2.5		µs
LSB voltage		-	VREF/ 1024	-	V
Differential nonlinearity	Guaranteed Monotonic	-	-	±1.0	LSB

D/A Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DAC full-scale voltage with respect to DACREF		-	±(VREF/2)	-	V
Resolution		-	10	-	Bits
Digital delay		-	2.5	-	µs
Output settling time	To within ±1 LSB	-	5.0	-	µs
LSB voltage		-	VREF/ 1024	-	V
Differential nonlinearity	Guaranteed Monotonic	-	-	±1.0	LSB
DACREF1, DACREF2		1.5		2.3	V
DACOUT1, DACOUT2		0.3		3.5	V

DSP Interface Timing

The following timing specifications are applied for a DSP bus interface . Timing measurements are made at 50% VDD with 50 pF load capacitances for data pins, unless otherwise noted.

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SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{STRBS}	ADR0..2/CS/$\overline{CS}$/R/$\overline{W}$ setup time prior to $\overline{STRB}$ fall		10		-	ns
t_{DDR}	Read data delay time from $\overline{STRB}$ fall		-		50	ns
t_{DHR}	Read data hold time after $\overline{STRB}$ rise		0		20	ns
t_{DSW}	Write data setup time prior to $\overline{STRB}$ rise		20		-	ns
t_{DHW}	Write data hold time after $\overline{STRB}$ rise		10		-	ns

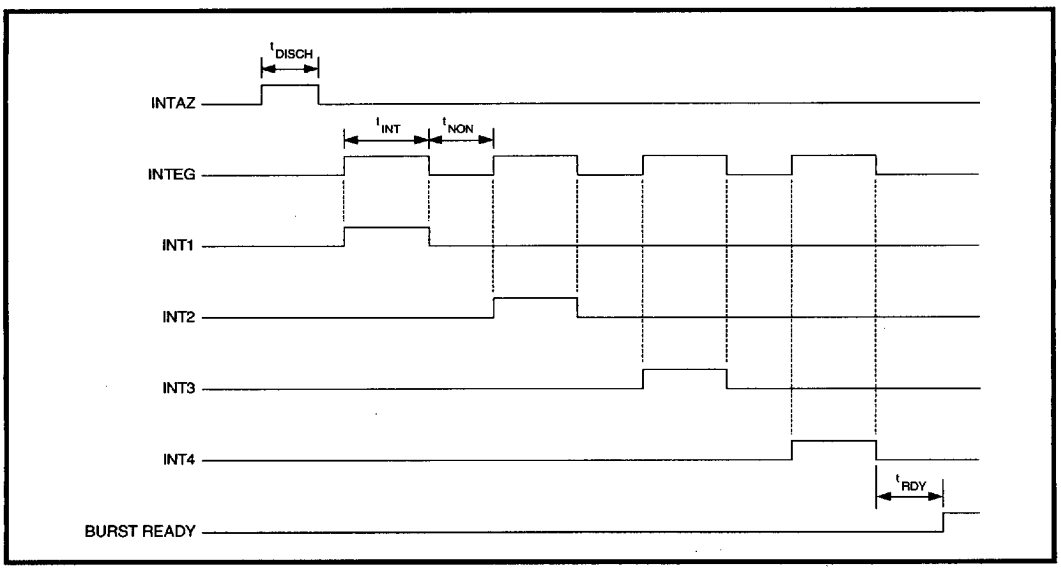


FIGURE 1: Embedded Servo Burst Processor Timing Diagram

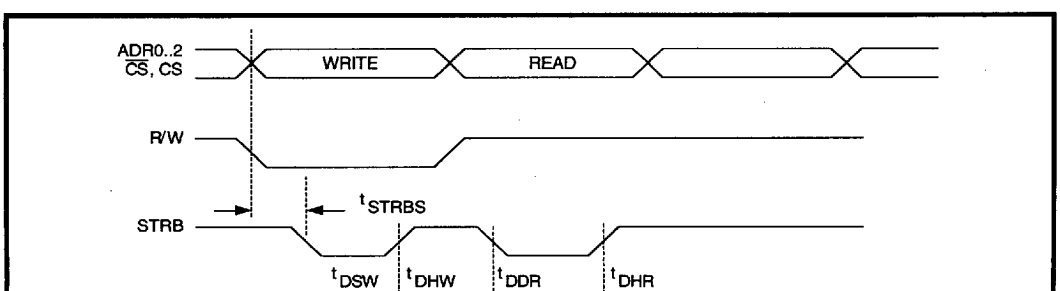


FIGURE 2: TMS320CXX DSP Bus Interface Timing Diagram

0: INTERRUPT MASK/STATUS			1: SERVO GAIN CONTROL & PRESCALER			2: ADC LSB DATA			3: ADC ADDRESS & MSB DATA		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0	BURST INT	BURSTRDY	0	SCALE0		0		'0'	0	ADC SEL0	ADC2
1	ADC INT	ADCRDY	1	SCALE1		1		'0'	1	ADC SEL1	ADC3
2			2	GAIN0		2		'0'	2	ADC SEL2	ADC4
3			3	GAIN1		3		'0'	3	ADC CALIB	ADC5
4			4	GAIN2		4		'0'	4		ADC6
5			5	GAIN3		5	SLEEP	'0'	5		ADC7
6			6	BSTSEL0		6	STBEN1	ADC0	6		ADC8
7			7	BSTSEL1		7	STBEN2	ADC1	7		ADC9

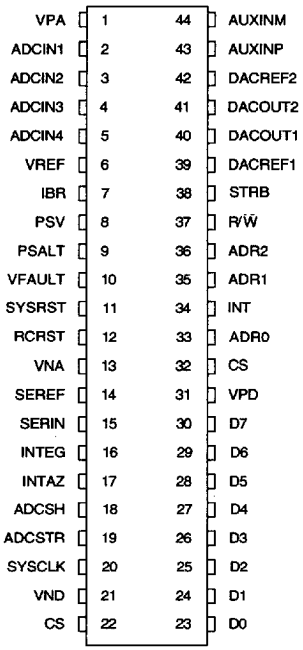
4: DAC1 LSB DATA			5: DAC1 MSB DATA			6: DAC2 LSB DATA			7: DAC2 MSB DATA		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0			0	DAC2 1		0			0	DAC2 2	
1			1	DAC3 1		1			1	DAC3 2	
2			2	DAC4 1		2			2	DAC4 2	
3			3	DAC5 1		3			3	DAC5 2	
4			4	DAC6 1		4			4	DAC6 2	
5			5	DAC7 1		5			5	DAC7 2	
6	DAC0 1		6	DAC8 1		6	DAC0 2		6	DAC8 2	
7	DAC1 1		7	DAC9 1		7	DAC1 2		7	DAC9 2	

FIGURE 5: SSI 32H6520 Embedded Servo Processor Register Map

SSI 32H6521
Embedded Servo Controller

PACKAGE PIN DESIGNATIONS

(Top View)



44-lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H6521 44-pin SOM	32H6521-CM	32H6521-CM

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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