QLU22108-PT280C Device Data Sheet

Utopia Level 2 to 1 Multiplexer

1.0 Utopia Level 2/1 Multiplexer Core Features

- Implements an Utopia L2 Slave and two to four Utopia L1 Masters providing a solution to aggregate Utopia Level 1 Slave devices to a Level 2 Master
- Compliant with ATM-Forum af-phy-0039.000 (Level 2) and af-phy-0017.000 (Level 1)
- Implements 8-bit data busses
- Level 2 interface implements MPHY mode with direct status indication
- Round Robin port arbitration independent for Egress (TX) and Ingress (RX) data pathes
- Level 2 interface meets 50MHz performance offering up to 400Mbps cell rate transfers
- Level 1 interface meets 25MHz performance offering up to 200Mbps cell rate transfers per Port
- Single chip solution with up to 3 east ports for improved system integration
- Supports cell level transfer mode
- Cell and clock rate decoupling with on chip FIFOs
- Up to 1 KByte of on chip FIFO per data direction
- Integrated management interface and built-in errored cell discard
- ATM Cell size programmable via external pins from 16 to 128 bytes
- Level 2 MPHY address programmable via external pins
- Optional Utopia parity generation/checking enable/disable via external pin
- Built in JTAG port (IEEE1149 compliant)
- Simulation model available for system level verification (Contact Quicklogic for details)
- Solution also available as flexible Soft-IP core, delivered with a full device modelization and verification testbenches

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2.0 Utopia Overview

The Utopia (Universal Test & Operations PHY Interface for ATM) interface is defined by the ATM Forum to provide a standard interface between ATM devices and ATM PHY or SAR (Segmentation And Re-assembly) devices.

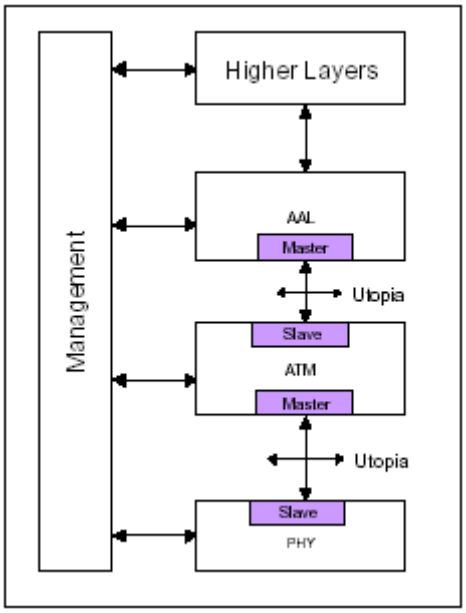

Figure 1: Utopia Reference Model

The Utopia Standard defines a full duplex bus interface with a Master/Slave paradigm. The Slave interface responds to the requests from the Master. The Master performs PHY arbitration and initiates data transfers to and from the Slave device.

The ATM forum has standardized the Utopia Levels 1 (L1) to 3 (L3). Each level extends the maximum supported interface speed from OC3, 155Mbps (L1) over OC12, 622Mbps (L2) to 3.2Gbit/s (L3).

The following Table 1 gives an overview of the main differences in these three levels.

Table 1: Utopia Level Differences

Utopia Level	Interface Width	Max. Interface Speed	Theoretic (typical) Throughput
1	8-bit	25 MHz	200 Mbps (typ. OC3 155 Mbps)
2	8-bit, 16-bit	50 MHz	800 Mbps (typ. OC12 622 Mbps)
3	8-bit, 32-bit	104 MHz	3.2 Gbps (typ. OC48 2.5 Gbps)

Utopia Level 1 implements an 8-bit interface running at up to 25MHz. Level 2 adds a 16 Bit interface and increases the speed to 50MHz. Level 3 extends the interface further by a 32 Bit word-size and speeds up to 104MHz providing rates up to 3.2 Gbit/s over the interface.

In addition to the differences in throughput, Utopia Level 2 uses a shared bus offering to physically share a single interface bus between one master and up to 31 slave devices (Multi-PHY or MPHY operation). This allows the implementation of aggregation units that multiplex several slave devices to a single Master device. The Level 1 and Level 3 are point-to-point only, whereas Level 1 has no notion of multiple slaves. Level 3 still has the notion of multiple slaves, but they must be implemented in a single physical device connected to the Utopia Interface.

3.0 Utopia L2 Slave to L1 Master Multiplexer Application

Utopia Level 2 offers the notion of multiple PHYs (MPHY) and a shared bus topology to connect several PHY devices to a single ATM Layer device, or use PHY devices with multiple ports.

The L2 Slave to L1 Master Multiplexer implements the necessary interfaces enabling to connect multiple Level 1 PHY devices to a Level 2 topology. The Multiplexer itself implements two or more Ports and aggregates them on the Level 2 interface.

As Utopia Level 2 allows for higher speed, at least two Level 1 devices can be aggregated into a single Level 2 interface without exceeding bandwidth. A bus extension to 16 bit on the L2 side can enable up to four Level 1 devices without exceeding the Level 2 interface bandwidth.

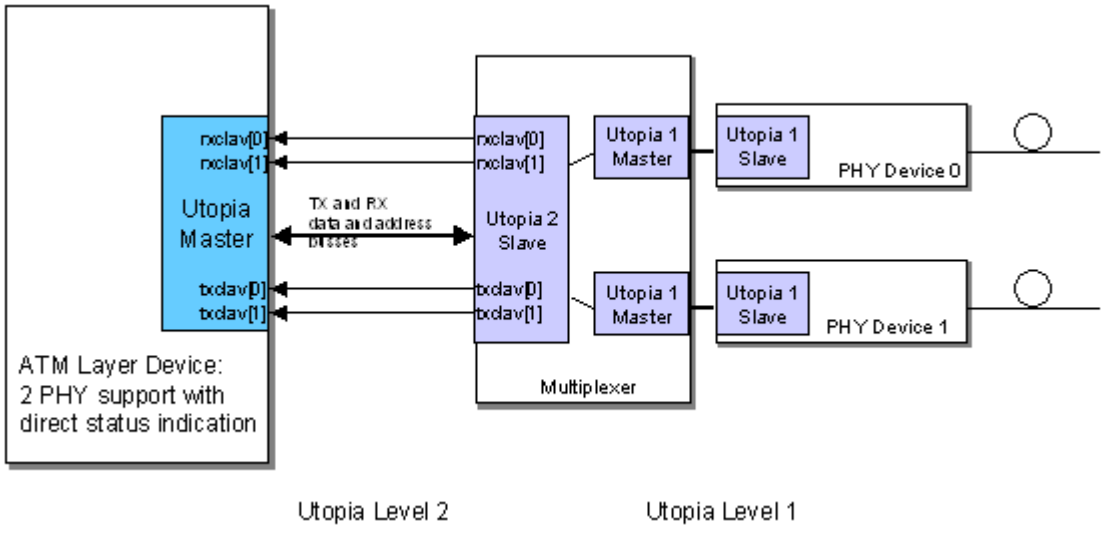

Figure 2: Utopia 2 Port Multiplexer Example

4.0 Application

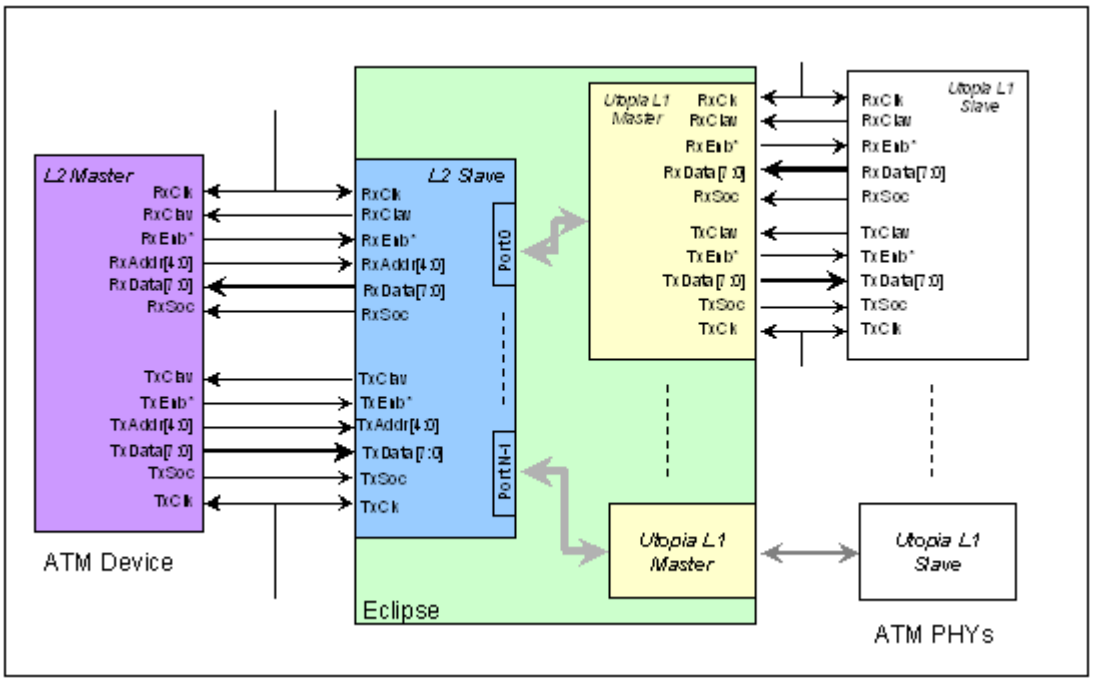

Figure 3: L2 to L1 Multiplexer

Data flows from the West side TX Interface to the corresponding TX Port on the east side of the multiplexer and the RX Ports to the RX Interface accordingly.

All Ports are served in a round-robin fashion, whereas the TX and RX sides are decoupled.

5.0 Core Pinout

On the Utopia interfaces, the Core implements all the required Utopia signals and provides all the Utopia optional signals (Indicated by an 'O' in the following tables). The optional Utopia signals are activated during the Core configuration and inactive Utopia signals should be left unconnected (Outputs) or tied to a zero logic level (inputs) as specified in the following Tables.

In addition to the Utopia Interface signals, error indication signals are available for error monitoring or statistics. An error indication always shows that a cell has been discarded by the multiplexer. Possible errors are parity or cell-length errors on the receive interface of the corresponding Utopia Interfaces.

All Utopia interfaces work in the same transfer mode (cell level). A mix is not possible.

To identify the sides of the core the notion "WEST" and "EAST" for the corresponding interfaces is used.

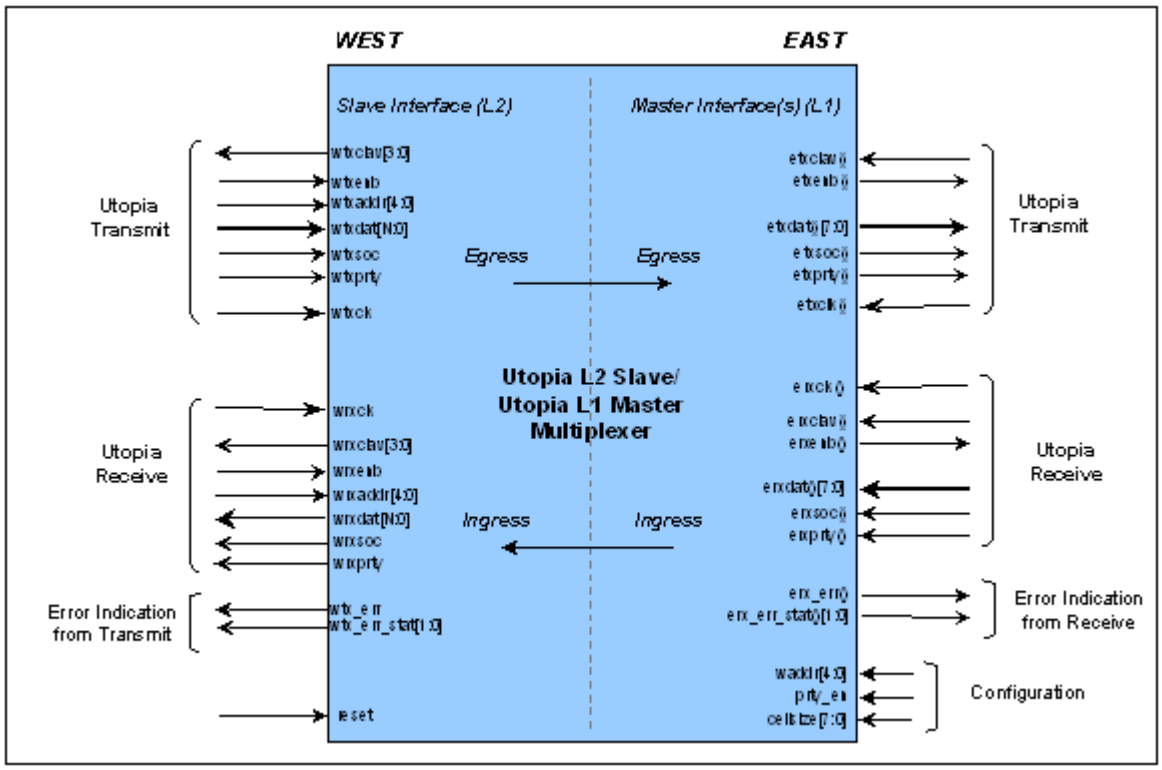

Figure 4: L2 to L1 Multiplexer Top Entity

5.1 Signal Descriptions

Table 2: Global Signal

Pin	Mode	Description
reset	In	Active high chip reset

Table 3: Device Management Interface

Pin	Mode	Description
wtx_err	Out	Transmit error indication on west interface. When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the west interface and is discarded.
wtx_err_stat(1:0)	Out	Transmit error status information for west interface. When wtx_err is driven, indicates the error status of the discarded cell: • wtx_err_stat(0) : When set to '1' indicates that a cell is discarded because of a parity error. • wtx_err_stat(1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).
erx_err(n)	Out	Receive error indication on east interface port n (n=0..3). When driven high, indicates that an errored cell (Wrong parity or wrong length) was received from the device connected to the corresponding east interface port.
erx_err_stat (2n+1:2n))	Out	Receive error status information for east receive interface port n (n=0..3). When etx_err is driven, indicates the error status of the discarded cell: • etx_err_stat(2n) : When set to '1' indicates that a cell is discarded because of a parity error. • etx_err_stat(2n+1) : When set to '1' indicates that a cell is discarded because it has a wrong length (Consecutive assertion of ut_tx_soc on the Utopia interface within less than a complete cell time).

NOTE: *wtx_.. signals are sampled with west transmit clock (wtxclk). etx_.. signals are sampled with west receive clock (wrxclk).*

Table 4: West Utopia Level 2 Slave Transmit Interface

Pin	Mode	Description
wtxclk	In	50MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
wtxdata[7:0]	In	Transmit data bus. The width of the data bus is be 8 Bit. N is the MSB.
wtxprty(O)	In	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be tied to '0'.
wtxsoc	In	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
wtxenb	In	Active low transmit data transfer enable.
wtxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.
wtxclav[3:1]	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected during the Core configuration, one txclav signal is implemented per PHY port. The maximum number of clav signals is limited to four.
wtxaddr[4:0]	In	Utopia transmit address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB.

NOTE: *(O) indicates optional signals.*

Table 5: West Utopia Level 2 Slave Receive Interface

Pin	Mode	Description
wrxclk	In	50MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
wrxdata[7:0]	Out	Receive data bus.
wrxprty (O)	Out	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
wrxsoc	Out	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
wrxenb	In	Active low transmit data transfer enable.
wrxclav[0]	Out	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.
wrxclav[3:1]	Out	Extra FIFO Full / Cell buffer available. In MPHY mode and when direct status indication is selected, one rxclav signal is implemented per PHY port. The maximum number of clav signals is limited to four. Not used and not available.
wrxaddr(4:0)	In	Utopia receive address. When the Core operates in MPHY mode, address bus used during polling and slave port selection. Bit 4 is the MSB.

Table 6: East Utopia Level 1 Master Transmit Interface (per Port, n=0..3)

Pin	Mode	Description
etxclk(n)	In	25MHz transmit byte clock. The Core samples all Utopia Transmit signals on txclk rising edge.
etxdata(n)[7:0]	Out	Transmit data bus.
erxprty(n) (O)	Out	Transmit data bus parity. Standard odd or non-standard even parity can be optionally checked by the connected Slave. When the parity check is disabled during the Core configuration, or not used in the design, the pin txprty should be left open.
erxsoc(n)	Out	Transmit start of cell. Asserted by the Master to indicate that the current word is the first word of a cell.
etxenb(n)	Out	Active low transmit data transfer enable.
etxclav(n)	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost full (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space to accept one cell.

NOTE: *(O) indicates optional signals.*

Table 7: East Utopia Level 1 Master Receive Interface (per Port, n=0..3)

Pin	Mode	Description
erxclk(n)	In	25MHz receive byte clock. The Core samples all Utopia Receive signals on rxclk rising edge.
erxdata(n)[7:0]	In	Receive data bus.
erxprty(n) (O)	In	Receive data bus parity. Standard odd or non standard even parity can be optionally generated by the Utopia Slave Core. When the parity generation is disabled during the Core configuration, the pin rxprty can be let unconnected.
erxsoc(n)	In	Receive start of cell. Asserted to indicate that the current word is the first word of a cell.
erxenb(n)	Out	Active low transmit data transfer enable.
erxclav(n)	In	Cell buffer available. Asserted in octet level transfers to indicate to the Master that the FIFO is almost empty (Active low) or, in cell level transfers, to indicate to the Master that the PHY port FIFO has space one cell available in the FIFO.

Table 8: Device Configuration Pins

Pin	Mode	Description
waddr[4:0]	In	Programs the Utopia L2 Slave address used on the west interfaces (tx and rx).
prty_en	In	Enable parity checking on the Utopia interface. If disabled (tied to 0), the wrx_err_stat(0) signal can be ignored and left open and the rx parity input should be tied to 0. Also the tx parity pins can be left open.
cellsize[7:0]	In	Define cellsize: sets the size in bytes of a cell. Binary value to be set usually by board wiring

The configuration pins are not intended for change during operation. They are usually board wired to configure the device for operation.

6.0 Global Signal Distribution

The externally provided Utopia Transmit and Receive clocks are connected to global resources to provide low skew and fast chip level distribution. In both data directions, the two corresponding Utopia Interfaces are decoupled by asynchronous FIFOs.

Therefore each interface runs completely independently each at its own tx and rx clocks which typically are up to 50 MHz on the WEST and up to 25 MHz on the EAST interface.

The Error indications of the two receive interfaces are always sampled within the west clock domains. The errors of the east rx interface is available on the erx_err signal, which is handled using the west clock domain (wrxclk). The west tx (receiving) error is directly derived from the west tx block (wtxclk).

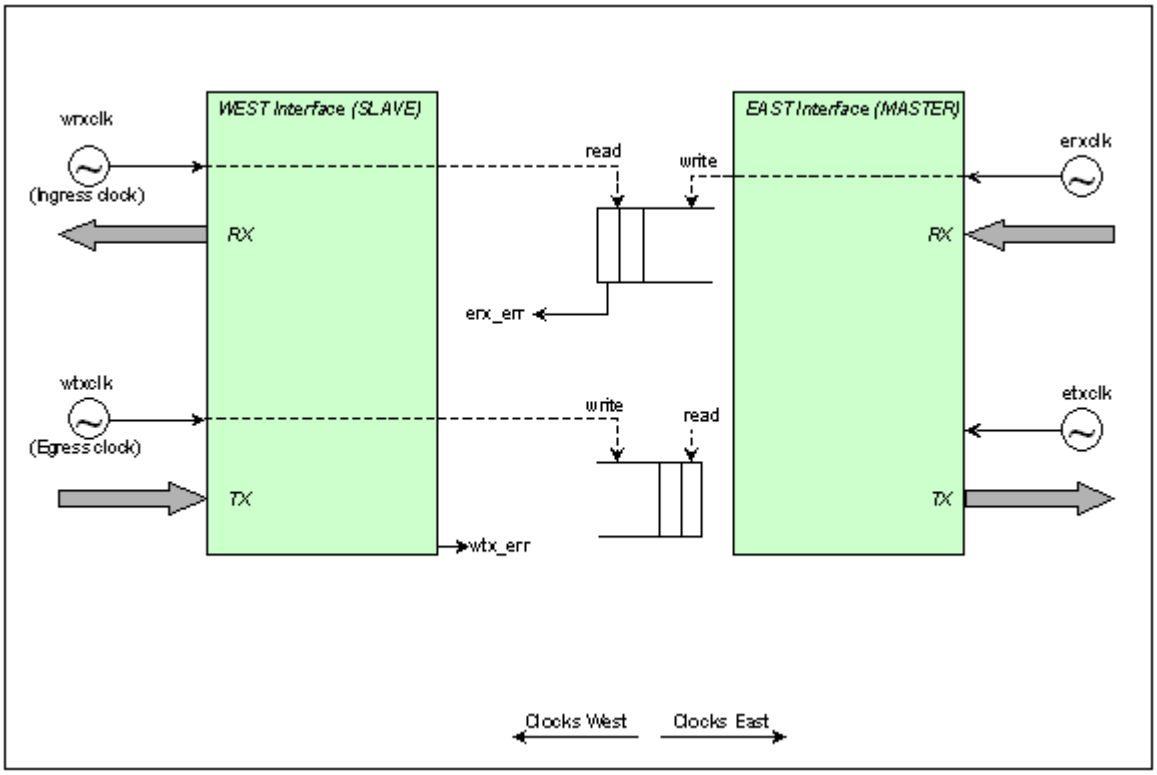

Figure 5: Slave/Master Multiplexer Clock Distribution (one east port shown)

7.0 Functional Description – Utopia Interface

The Utopia Multiplexer implements a single port on the west and separate single-PHY interfaces on the east.

The West Interface (Utopia L2) operates in MPHY mode with direct status indication. It implements a single clav signal per direction and port (t/rxclav[X]) and the address bus to select the device within a shared bus topology.

The East Interface (L1) has no notion of MPHY. It has a single clav signal and no address bus.

7.1 Utopia Interface Single PHY Transmit Interface (L1)

The Transmit interface is controlled by the Master.

The transmit interface has data flowing in the same direction as the ATM enable `ut_tx_enb`. The ATM transmit block generates all output signals on the rising edge of the `ut_txclk`.

Transmit data is transferred from the Master to Slave via the following procedure. The Slave indicates it can accept data using the `ut_txclav` signal, then the Master drives data onto `ut_txdat` and asserts `ut_txenb`. The Slave controls the flow of data via the `ut_txclav` signal.

7.1.1 Cell Level Transfer - Single Cell

The Slave asserts `ut_txclav` **1** when it is capable of accepting the transfer of a whole cell. The Master asserts `ut_txenb` (Low) to indicates that it drives valid data to the Slave **2**. Together with the first octet of a cell, the Master device asserts `ut_txsoc` for one clock cycle **3**.

To ensure that the Master does not cause transmit overrun, the Slave deasserts `ut_txclav` at least 4 cycles before the end of a cell if it cannot accept the immediate transfer of the subsequent cell **4**.

The Master can pause the cell transfer by de-asserting `ut_txenb` **5**. To complete the transfer to the Slave, the Master de-asserts `ut_tx_enb` **6**.

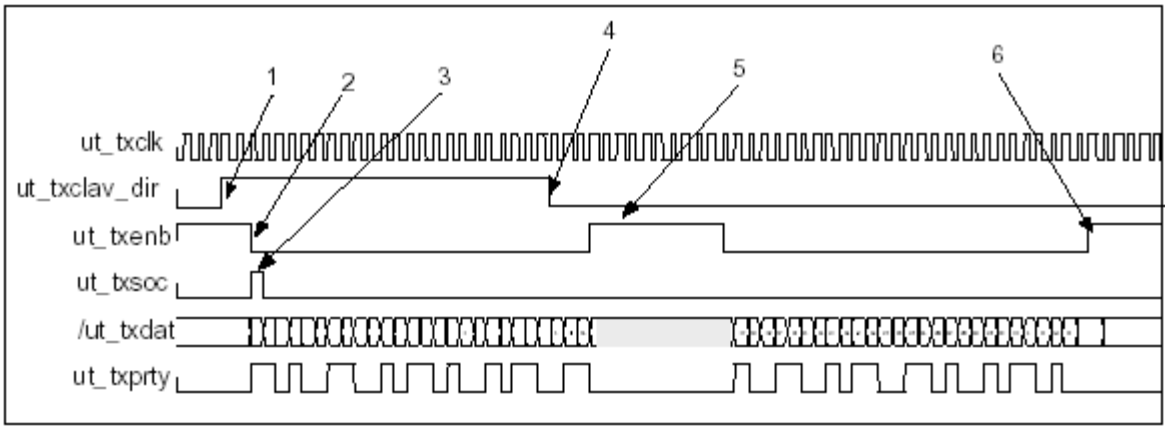

Figure 6: Single Cell Transfer – Cell Level Transfer

7.1.2 Cell Level Transfer – Back to Back Cells

When, during a cell transfer, the Slave is able to receive a subsequent cell, the Master can keep `ut_txenb` asserted between two cells **1** and asserts `ut_txsoc`, to start a new cell transfer, immediately after the last octet of the previous cell **2**.

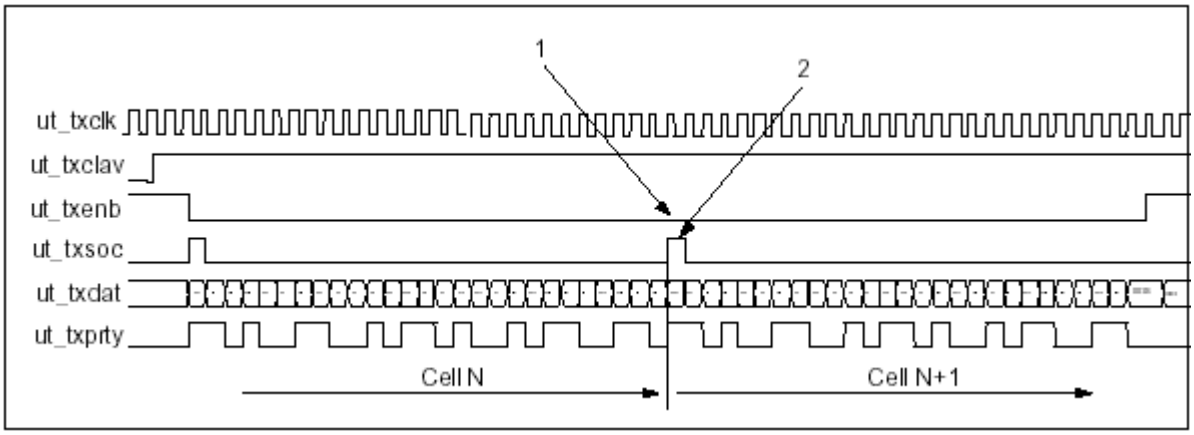

Figure 7: Back to Back Cell Transfer – Cell Level Transfer

7.2 Utopia Interface Single PHY Receive Interface (L1)

The Receive interface is controlled by the Master. The receive interface has data flowing in the opposite direction to the Master enable `ut_rxenb`.

Receive data is transferred from the Slave to Master via the following procedure. The Slave indicates it has valid data, then the Master asserts `ut_rxenb` to read this data from the Slave. The Slave indicates valid data (thereby controlling the data flow) via the `ut_rxclav` signal.

7.2.1 Cell Level Transfer - Single Cell

The Slave asserts `ut_rx_clav` when it is ready to send a complete cell to the Master device **1**. The Master interface asserts `ut_rxenb` to start the cell transfer. The Slave samples `ut_rxenb` and starts driving data **2**. The Slave asserts `ut_rxsoc` together with the cell first word to indicate the start of a cell **3**.

The Master can pause a transfer by de-asserting `ut_rxenb` **4**. The Slave samples high `ut_rxenb` and stops driving data **5**. To resume the transfer, the Master re-asserts `ut_rxenb` **6**. The Slave samples low `ut_rxenb` and starts driving valid data **7**.

The Master drives `ut_txenb` high one before the expected end of the current cell if the Slave has no more cell to transfer **8**. The Slave de-asserts `ut_rxclav` to indicate that no new cell is available **9**.

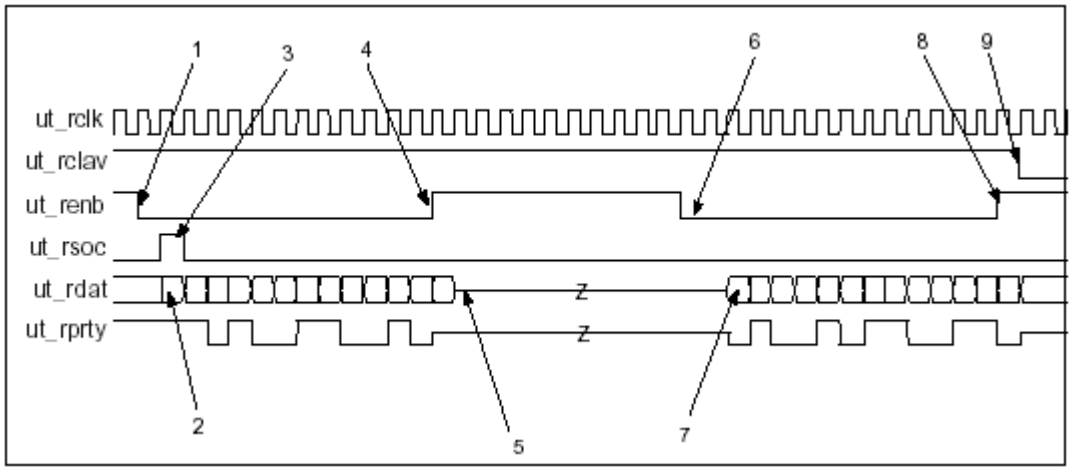

Figure 8: Single Cell Transfer - Cell Level Transfer

7.2.2 Cell Level Transfer - Back to Back Cells

If the Master keeps `ut_rxenb` asserted at the end of a cell transfer **1** and if the Slave has a new cell to send, the Slave keeps `ut_rxclav` asserted **2** and immediately drives the new cell asserting `ut_rxsoc` to indicate the start of a new cell **3**.

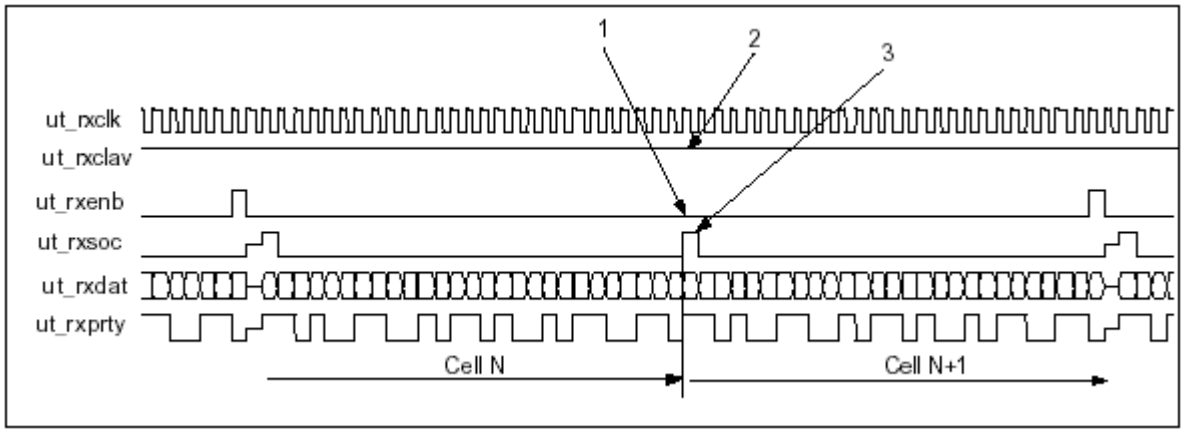

Figure 9: Back to Back Cells Transfer - Cell Level Transfer

NOTE: *If the Master keeps `ut_rxenb` asserted at the end of a packet and if the Slave does not have a new cell available, the Slave de-asserts `ut_rxclav` and the data of the bus `ut_rxdat` are invalid.*

7.3 Utopia Interface MPHY Transmit (L2)

When operating in MPHY mode, the Master checks, (Typically in a round robin fashion) the status of all the Slave ports. Two options are defined by the Utopia standard:

- Polled status indication with all the PHY ports using a shared single CLAV signal to report their status to the Master
- Direct status indication with one CLAV implemented per PHY port or per Utopia group.

In MPHY mode only one transmit PHY port is selected at a time for data transfers but the Master continuously polls the status of the Slave's other PHY ports.

The Bridge implements the second approach, using direct status indication.

7.3.1 MPHY Operation with Direct Status

For each PHY port, a status signal `ut_txclav` is permanently available. The Utopia Bus then supports up to four PHY ports, each using one CLAV signal (Slave port `ut_txclav_dir(n)`).

For each port independently, `ut_txclav_dir(n)` is asserted when enough space is available for a complete cell in the port FIFO 1 and `ut_txclav_dir(n)` is de-asserted when the corresponding port FIFO cannot receive the subsequent cell **2**.

Status signals and cell transfers are independent of each other for each port. No address information is needed to obtain status information. Address information must be valid only for selecting a PHY port prior to one or multiple cell transfers. To select a port, the Master de-asserts `ut_txenb` **3**, puts address port on `ut_txaddr(4:0)` **4**, the port is selected by the Slave when `ut_txenb` goes low (Re-asserted by the Master) **5**.

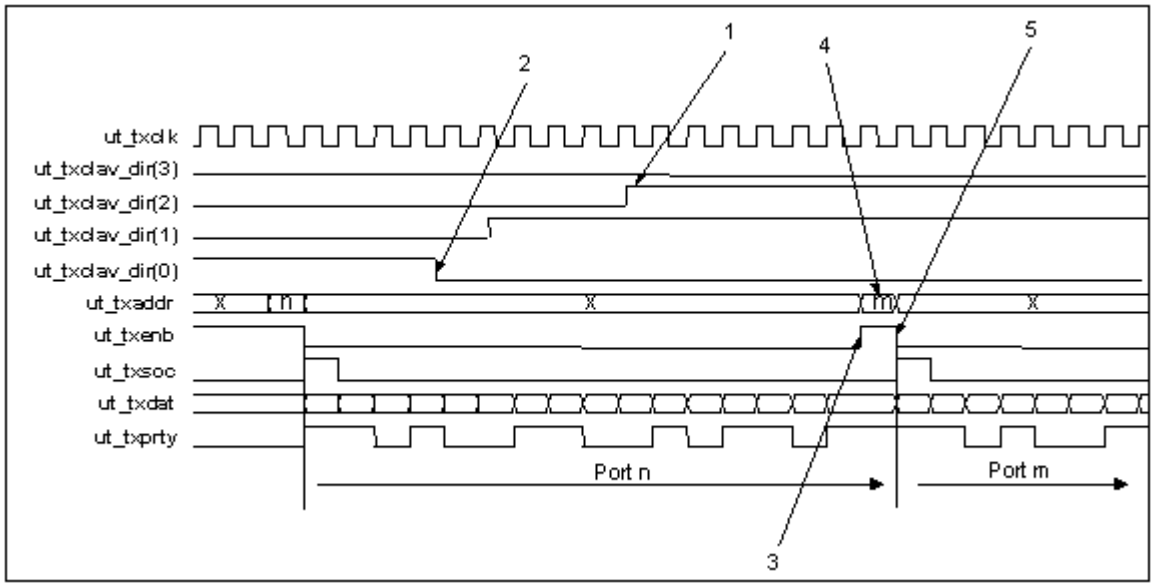

Figure 10: MPHY Transmit - Direct Status Indication

As defined for single CLAV Utopia Transmit, the Master can pause a transfer and implicitly re-select a PHY port.

7.4 Utopia Interface MPHY Receive (L2)

When operating in MPHY mode, the Master checks, (Typically in a round robin fashion) the status of all the Slave ports. Two options are defined by the Utopia standard:

- Polled status indication with all the PHY ports using a signal CLAV signal to report their status to the Master
- Direct status indication with one CLAV implemented per PHY port or per Utopia group.

In MPHY mode only one receive PHY port is selected at a time for data transfers but the Master can continuously polls the status of the Slave PHY ports.

7.4.1 MPHY Operation with Direct Status

For each PHY port, a status signal `ut_rxclav_dir(n)` is permanently available. For each port independently, `ut_rxclav_dir(n)` is asserted when the corresponding PHY port has a cell available in its FIFO 1 and `ut_rxclav_dir(n)` is de-asserted when the corresponding port FIFO cannot transmit a complete cell to the Master **2**.

Status signals and cell transfers are independent of each other for each port. No address information is needed to obtain status information. Address information must be valid only for selecting a PHY port prior to one or multiple cell transfers. To select a port, the Master de-asserts `ut_rxenb` **3**, puts address port on `ut_rxaddr(4:0)` **4**, the port is selected by the Slave when `ut_rxenb` goes low (Re-asserted by the Master) **5**.

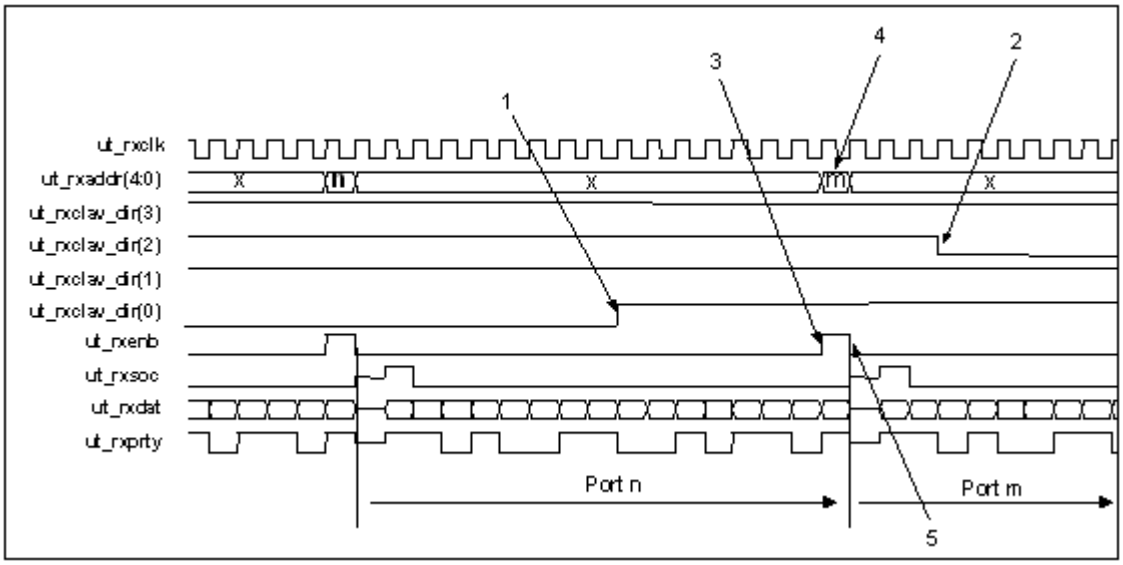

Figure 11: MPHY Receive - Direct Status Indication

8.0 Core Management and Error Handling

On Egress, the Core is designed to handle and report Utopia errors such as Parity error or wrong cell length. Errored cells are discarded with an error status indication provided to the user PHY application.

When an errored cell is received on the Utopia interface, the Core discards the complete cell and provides a cell discard indication to the User PHY application (Signal `eg_err(n)` asserted) **1** together with a cell discard status (Signal `eg_err_stat(1:0)`) **2**.

NOTE: *eg_err is routed to the corresponding `wtx_err` and `etx_err` respectively (see Figure 4).*

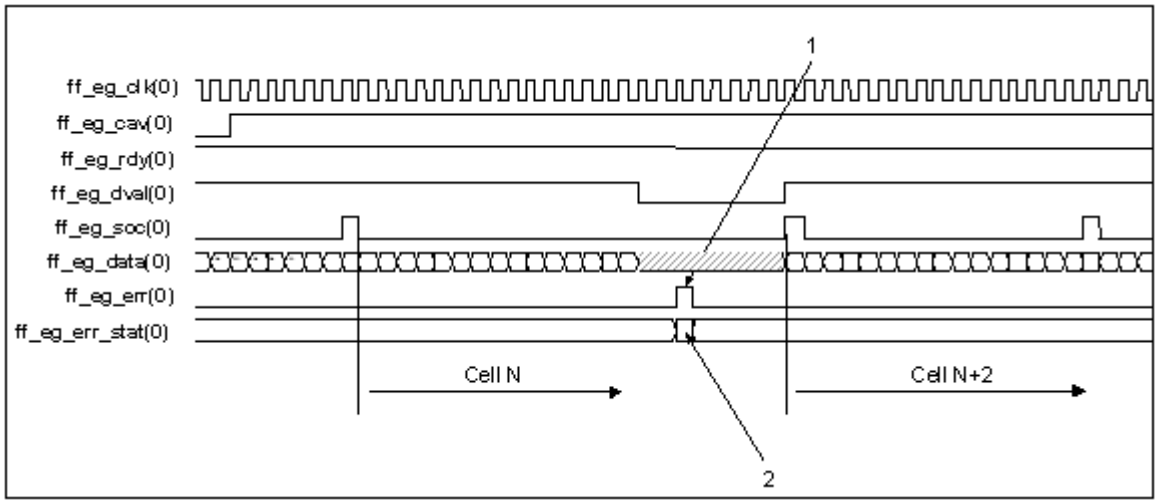

Figure 12: Cell Discard Indication

Table 9: Error Status Word Bit Coding

Error Status Bit	Name	Description
0	PARITY_ERR	Valid when wtx/etx_err is asserted. If set to one indicates that a cell is discarded with a parity error decoded by the Core.
1	LENGTH_ERR	Valid when wtx/etx_err is asserted. If set to one indicates that a cell is discarded with a cell length error detected on the Utopia interface.

The signals are sampled on the corresponding clocks from the west interface:

- erx_... sampled with wrxclk (west receive clock)
- wtx_... sampled with wtxclk (west transmit clock)

9.0 Complexity and Performance Summary

9.1 Timing Parameters Definition

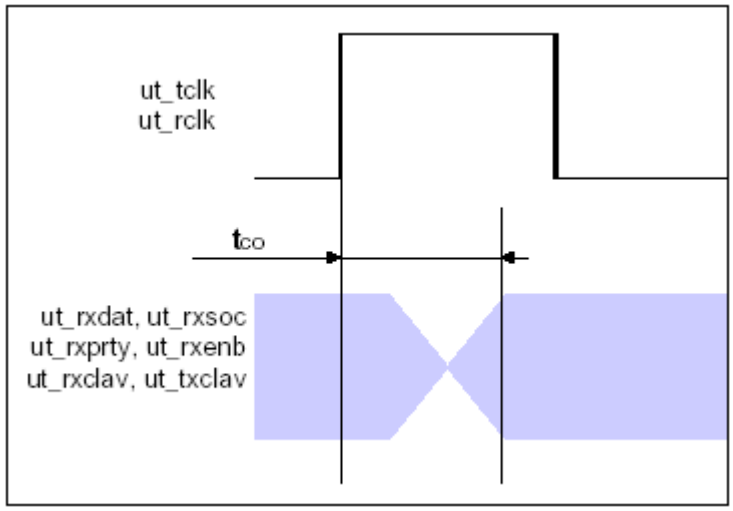

Figure 13: Tco Timing Parameter Definition

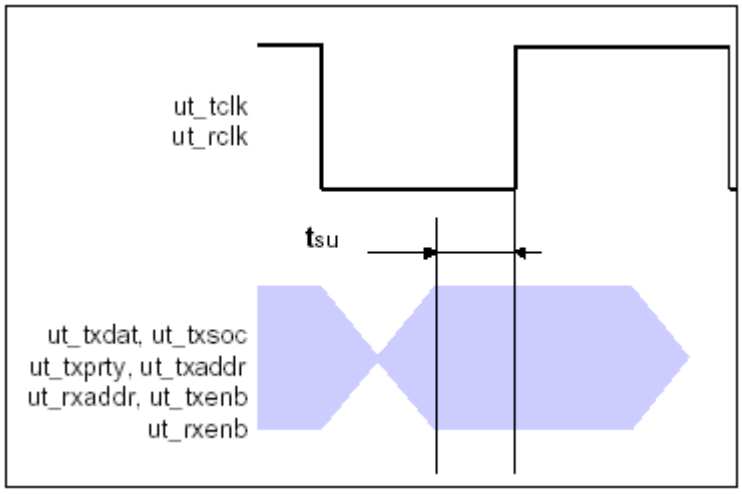

Figure 14: Tsu Timing Parameter Definition

Table 10: 8-Bit Utopia Interface Timing Characteristics

Parameter	typ	Max	Unit
tco	7.5	7.0	ns
tsu	2.5	2.4	ns
wrxclk		66	MHz
wtxclk		69	MHz
erxclk		62	MHz
etxclk		62	MHz
minimum reset time	50		ns

NOTE: *Timing model "worst" case is used.*

10.0 Device Pinout

10.1 Signals Overview

The table summarizes all signals. If less than 4 ports are implemented, the port numbers N vary from 0 to maximum port available.

Table 11: Signal Overview Table

Signals	Description
wrxclk, wrxclav, wrxenb*, wrxdat, wrxsoc, wrxaddr	West Utopia L2 Receive Interface.
wtxclk, wtxclav, wtxenb*, wtxdata, wtxsoc, wtxaddr	West Utopia L2 Transmit Interface.
wtx_err, wtx_err_stat	West Interface error indication (sampled with wtxclk).
erxclk[N], erxclav[N], erxenb[N]*, erxsoc[N], erxdataN[7:0]	East Utopia L1 Receive Interface. Port N (N=0..3)Note: the data port names are not indexed, instead, explicitly named erxdata0.. erxdata3 each consisting of 8 pins.
etxclk[N], etxclav[N], etxenb[N]*, etxsoc[N], etxdataN[7:0]	East Utopia L1 Transmit Interface. Port N (N=0..3) Note: the data port names are not indexed, instead, explicitly named erxdata0.. erxdata3 each consisting of 8 pins. Unused etxdatN[] signals of non-existing ports should be left open.
erx_err[0], erx_err_stat[1:0]	East Interface error indication Port 0 (sampled with wrxclk).
erx_err[1], erx_err_stat[3:2]	East Interface error indication Port 1 (sampled with wrxclk).
erx_err[2], erx_err_stat[5:4]	East Interface error indication Port 2 (sampled with wrxclk).
erx_err[3], erx_err_stat[7:6]	East Interface error indication Port 3 (sampled with wrxclk).
prty_en, cellsize, waddr	Configuration Pins to be board wired. Usual values for waddr are between 0 and 3.
reset	Active high device reset

Table 11: Signal Overview Table (Continued)

Signals	Description
GND	Ground
VCC	Device Power 2.5 V
clk(x)	unused clock inputs should be tied to GND
IOCTRL(x)	
VCCIO(x)	IO Power 3.0 V
INREF(x)	connect to GND
PLLRST(x)	connect to GND or VCC
PLLOUT(x)	connect to GND or VCC
VCCPLL(x)	
GNDPLL(x)	
TCK, TRSTB	JTAG signals. connect to GND
TMS, TDI	JTAG signals. connect to VCC
TDO	JTAG signal. leave open
iov	
nc	not connected. should be left open

*: active low signal

10.2 280 Pin FPBGA Device Diagram

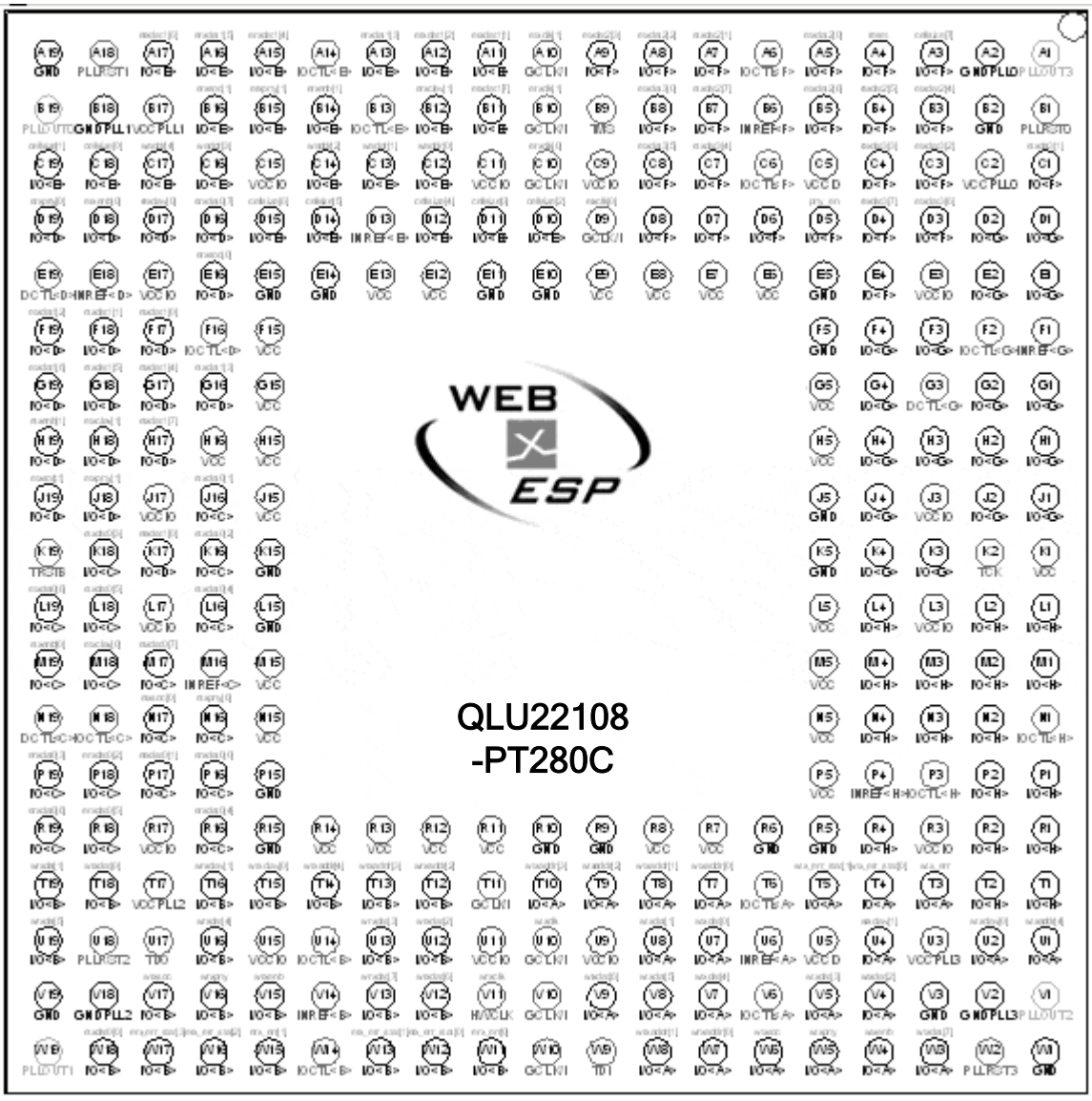

Figure 15: 280 Pin Bottom View

10.3 280 Pin FPBGA Pinout Table

Table 12: 280 Pin FPBGA Pinout Table

Pin	Function	Pin	Function	Pin	Function	Pin	Function	Pin	Function
A1	PLLOUT3	C19	cellsize[1]	G17	etxdat1[4]	N4	I/O<H>	U2	wtxclav[0]
A2	GNDPLL0	D1	I/O<G>	G18	etxdat1[5]	N5	VCC	U3	VCCPLL3
A3	cellsize[7]	D2	I/O<G>	G19	etxdat1[6]	N15	VCC	U4	wtxclav[1]
A4	reset	D3	etxdat3[6]	H1	I/O<G>	N16	etxprty[0]	U5	VCCIO
A5	etxdat2[0]	D4	etxdat3[7]	H2	I/O<G>	N17	etxsoc[0]	U6	INREF<A>
A6	IOCTL<F>	D5	prty_en	H3	I/O<G>	N18	IOCTL<C>	U7	wtxdat[0]
A7	etxdat2[1]	D6	I/O<F>	H4	I/O<G>	N19	IOCTL<C>	U8	wtxdat[1]
A8	etxdat2[2]	D7	I/O<F>	H5	VCC	P1	I/O<H>	U9	VCCIO
A9	etxdat2[3]	D8	I/O<F>	H15	VCC	P2	I/O<H>	U10	wtxclk
A10	etxclk[1]	D9	etxclk[0]	H16	VCC	P3	IOCTL<H>	U11	VCCIO
A11	erxdat1[1]	D10	cellsize[2]	H17	etxdat1[7]	P4	INREF<H>	U12	wrxdat[2]
A12	erxdat1[2]	D11	cellsize[3]	H18	etxclav[1]	P5	VCC	U13	wrxdat[3]
A13	erxdat1[3]	D12	cellsize[4]	H19	etxenb[1]	P15	GND	U14	IOCTL<B>
A14	IOCTL<E>	D13	INREF<E>	J1	I/O<G>	P16	erxdat0[0]	U15	VCCIO
A15	erxdat1[4]	D14	cellsize[5]	J2	I/O<G>	P17	erxdat0[1]	U16	wrxdat[4]
A16	erxdat1[5]	D15	cellsize[6]	J3	VCCIO	P18	erxdat0[2]	U17	(Floating)
A17	erxdat1[6]	D16	erxdat0[7]	J4	I/O<G>	P19	erxdat0[3]	U18	PLLRST2
A18	PLLRST1	D17	erxclav[0]	J5	GND	R1	I/O<H>	U19	wrxdat[5]
A19	GND	D18	erxenb[0]	J15	VCC	R2	I/O<H>	V1	PLLOUT2
B1	PLLRST0	D19	erxprty[0]	J16	etxdat0[1]	R3	VCCIO	V2	GNDPLL3
B2	GND	E1	I/O<G>	J17	VCCIO	R4	I/O<H>	V3	GND
B3	etxdat2[4]	E2	I/O<G>	J18	etxprty[1]	R5	GND	V4	wtxdat[2]
B4	etxdat2[5]	E3	VCCIO	J19	etxsoc[1]	R6	GND	V5	wtxdat[3]
B5	etxdat2[6]	E4	I/O<F>	K1	VCC	R7	VCC	V6	IOCTL<A>
B6	INREF<F>	E5	GND	K2	TCK	R8	VCC	V7	wtxdat[4]
B7	etxdat2[7]	E6	VCC	K3	I/O<G>	R9	GND	V8	wtxdat[5]
B8	etxdat3[0]	E7	VCC	K4	I/O<G>	R10	GND	V9	wtxdat[6]
B9	TMS	E8	VCC	K5	GND	R11	VCC	V10	clk(1)
B10	erxclk[1]	E9	VCC	K15	GND	R12	VCC	V11	wrxclk
B11	erxdat1[7]	E10	GND	K16	etxdat0[2]	R13	VCC	V12	wrxdat[6]
B12	erxclav[1]	E11	GND	K17	erxdat1[0]	R14	VCC	V13	wrxdat[7]
B13	IOCTL<E>	E12	VCC	K18	etxdat0[3]	R15	GND	V14	INREF<B>
B14	erxenb[1]	E13	VCC	K19	TRSTB	R16	erxdat0[4]	V15	wrxenb
B15	erxprty[1]	E14	GND	L1	I/O<H>	R17	VCCIO	V16	wrxprty
B16	erxsoc[1]	E15	GND	L2	I/O<H>	R18	erxdat0[5]	V17	wrxsoc
B17	VCCPLL1	E16	erxsoc[0]	L3	VCCIO	R19	erxdat0[6]	V18	GNDPLL2
B18	GNDPLL1	E17	VCCIO	L4	I/O<H>	T1	I/O<H>	V19	GND
B19	PLLOUT0	E18	INREF<D>	L5	VCC	T2	I/O<H>	W1	GND
C1	etxdat3[1]	E19	IOCTL<D>	L15	GND	T3	wtx_err	W2	PLLRST3
C2	VCCPLL0	F1	INREF<G>	L16	etxdat0[4]	T4	wtx_err_stat[0]	W3	wtxdat[7]
C3	etxdat3[2]	F2	IOCTL<G>	L17	VCCIO	T5	wtx_err_stat[1]	W4	wtxenb
C4	etxdat3[3]	F3	I/O<G>	L18	etxdat0[5]	T6	IOCTL<A>	W5	wtxprty
C5	VCCIO	F4	I/O<G>	L19	etxdat0[6]	T7	wtxaddr[0]	W6	wtxsoc
C6	IOCTL<F>	F5	GND	M1	I/O<H>	T8	wtxaddr[1]	W7	wrxaddr[0]
C7	etxdat3[4]	F15	VCC	M2	I/O<H>	T9	wtxaddr[2]	W8	wrxaddr[1]
C8	etxdat3[5]	F16	IOCTL<D>	M3	I/O<H>	T10	wtxaddr[3]	W9	TDI
C9	VCCIO	F17	etxdat1[0]	M4	I/O<H>	T11	PLLIN1	W10	PLLIN2
C10	erxclk[0]	F18	etxdat1[1]	M5	VCC	T12	wrxaddr[2]	W11	erx_err[0]
C11	VCCIO	F19	etxdat1[2]	M15	VCC	T13	wrxaddr[3]	W12	erx_err_stat[0]
C12	waddr[0]	G1	I/O<G>	M16	INREF<C>	T14	wrxaddr[4]	W13	erx_err_stat[1]
C13	waddr[1]	G2	I/O<G>	M17	etxdat0[7]	T15	wrxclav[0]	W14	IOCTL<B>
C14	waddr[2]	G3	IOCTL<G>	M18	etxclav[0]	T16	wrxclav[1]	W15	erx_err[1]
C15	VCCIO	G4	I/O<G>	M19	etxenb[0]	T17	VCCPLL2	W16	erx_err_stat[2]
C16	waddr[3]	G5	VCC	N1	IOCTL<H>	T18	wrxdat[0]	W17	erx_err_stat[3]
C17	waddr[4]	G15	VCC	N2	I/O<H>	T19	wrxdat[1]	W18	etxdat0[0]
C18	cellsize[0]	G16	etxdat1[3]	N3	I/O<H>	U1	wtxaddr[4]	W19	PLLOUT1

11.0 References

- ATM Forum, Utopia Level 1, af-phy-0017.000, 1994
- ATM Forum, Utopia Level 2, af-phy-0039.000, 1995

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