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MOTOROLA SEMICONDUCTOR TECHNICAL DATA

T-39-11

BUZ10L
MTP23N05L

Power Field Effect Transistor

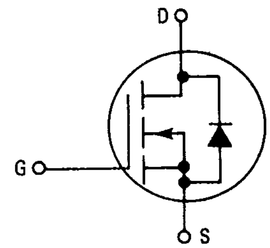
N-Channel Enhancement-Mode Silicon Gate

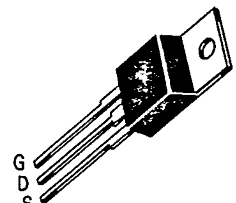
These TMOS Power FETs are designed for high speed, low loss power switching applications such as switching regulators, converters, motor controls, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds
- Low $r_{DS(on)}$ — 0.07 Ω max
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads
- Low Drive Requirement — $V_{GS(th)}$ = 2.5 V max
- Logic Level

TMOS™

LOGIC LEVEL
TMOS POWER FETs
23 AMPERES
$r_{DS(on)}$ = 0.07 OHM
50 VOLTS





CASE 221A-04
TO-220AB

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	50	Vdc
Drain-Gate Voltage (R_{GS} = 20 kΩ)	V_{DGR}	50	Vdc
Gate-Source Voltage — Continuous — Pulsed ($t_p \leq 50\ \mu s$)	V_{GS} V_{GSM}	±10 ±20	Vdc
Drain Current — Continuous (T_C = 25°C) — Pulsed	I_D I_{DM}	23 92	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 150	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.67 75	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 1.0 mA)	$V_{(BR)DSS}$	50	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 50 Volts, V_{GS} = 0) (V_{DS} = 50 Volts, V_{GS} = 0, T_J = 125°C)	I_{DSS}	 — —	 20 100	 250 1000	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	10	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	10	100	nAdc

(continued)

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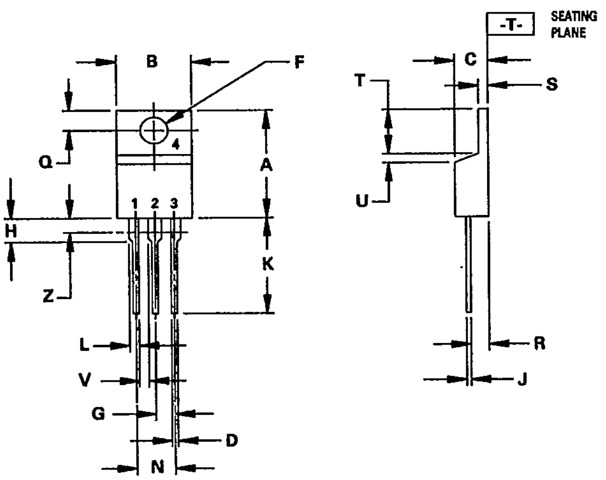
ELECTRICAL CHARACTERISTICS — continued (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mA)		$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Static Drain-Source On-Resistance (V_{GS} = 5.0 Vdc, I_D = 11.5 Adc)		$r_{DS(on)}$	—	0.06	0.07	Ohm
Forward Transconductance (V_{DS} = 25 V, I_D = 11.5 A)		g_{FS}	8.0	17	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	940	1250	pF
Output Capacitance		C_{oss}	—	500	750	
Reverse Transfer Capacitance		C_{rss}	—	180	270	
Total Gate Charge	(V_{DS} = 25 V, V_{GS} = 5.0 Vdc, I_D = 23 A)	Q_g	—	21	—	nC
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 30 V, I_D = 3.0 A, V_{GS} = 10 V, R_{GS} = 50 ohms)	$t_{d(on)}$	—	25	40	ns
Rise Time		t_r	—	60	90	
Turn-Off Delay Time		$t_{d(off)}$	—	100	130	
Fall Time		t_f	—	75	95	
SOURCE DRAIN DIODE CHARACTERISTICS*						
Forward On-Voltage	(I_S = 46 A, V_{GS} = 0)	V_{SD}	—	1.3	1.8	Vdc
Forward Turn-On Time	(I_S = 23 A, dI_S/dt = 100 A/μs, V_R = 30 V)	t_{on}	Limited by Stray Inductance			
Reverse Recovery Time		t_{rr}	—	150	—	ns
		Q_{rr}	—	1.0	—	μC

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

OUTLINE DIMENSIONS

CASE 221A-04
TO-220AB



STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIM Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	14.48	15.75	0.570	0.620
B	9.66	10.28	0.380	0.405
C	4.07	4.82	0.160	0.190
D	0.64	0.88	0.025	0.035
F	3.61	3.73	0.142	0.147
G	2.42	2.66	0.095	0.105
H	2.80	3.93	0.110	0.155
J	0.36	0.55	0.014	0.022
K	12.70	14.27	0.500	0.562
L	1.15	1.39	0.045	0.055
N	4.83	5.33	0.190	0.210
Q	2.54	3.04	0.100	0.120
R	2.04	2.79	0.080	0.110
S	1.15	1.39	0.045	0.055
T	5.97	6.47	0.235	0.255
U	0.00	1.27	0.000	0.050
V	1.15	—	0.045	—
Z	—	2.04	—	0.080

Figure 1. On-Region Characteristics

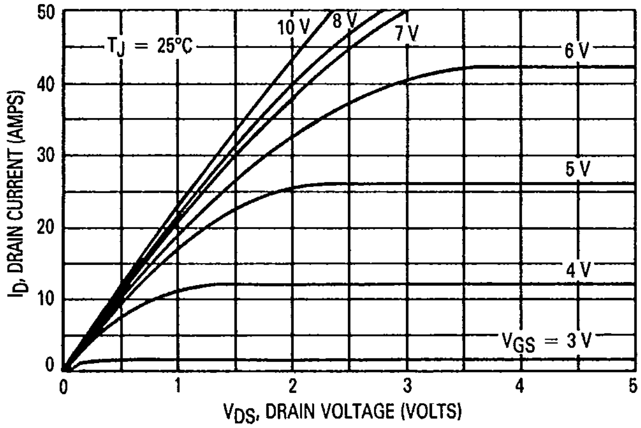


Figure 2. Gate-Threshold Voltage Variation With Temperature

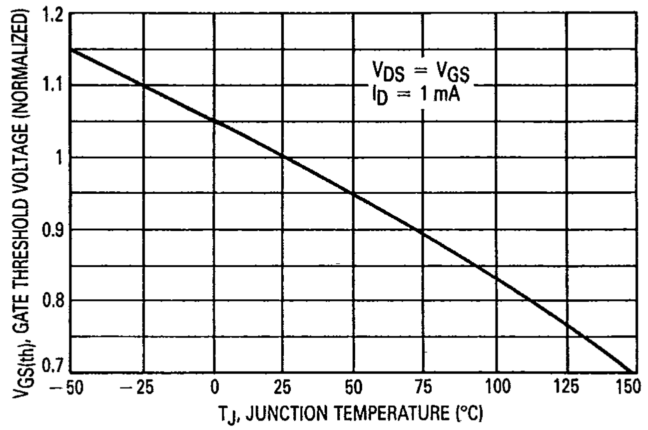


Figure 3. On-Resistance Variation versus Junction Temperature

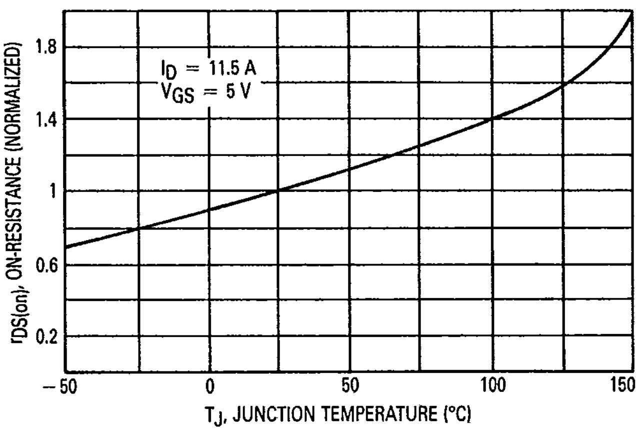


Figure 4. Breakdown Voltage Variation With Temperature

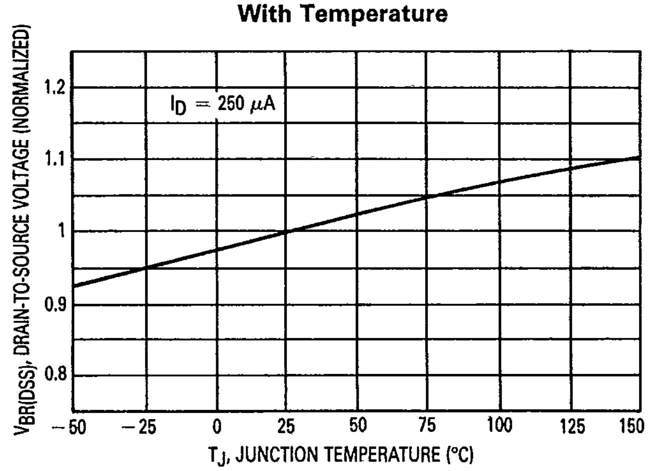


Figure 5. Gate Charge versus Gate-To-Source Voltage

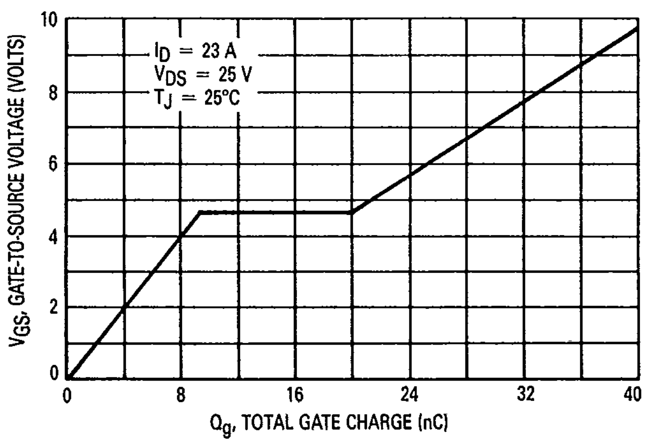
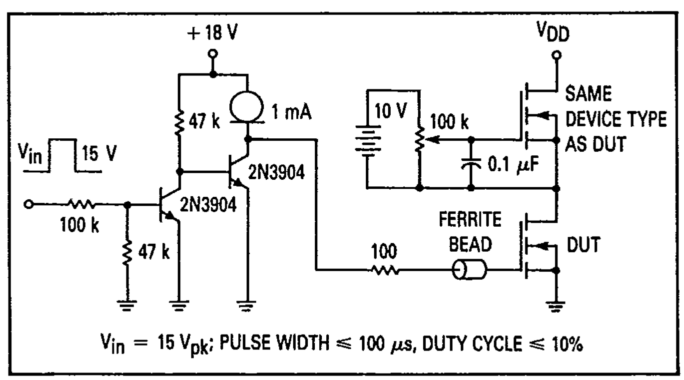


Figure 6. Gate Charge Test Circuit



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

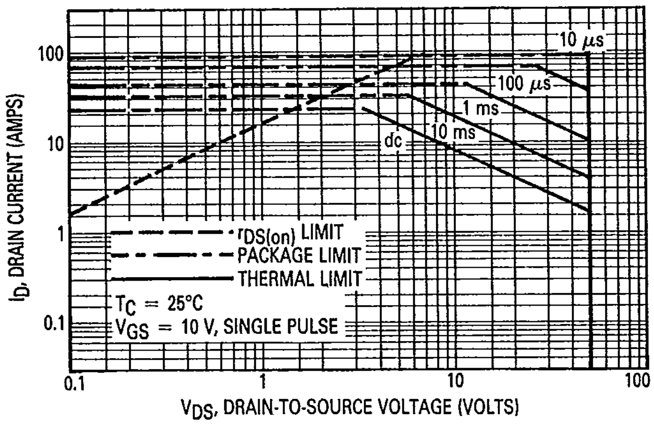
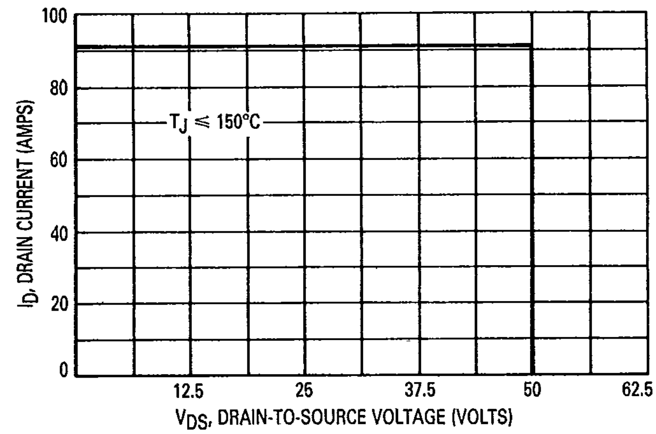


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and its Use" provides detailed instructions.

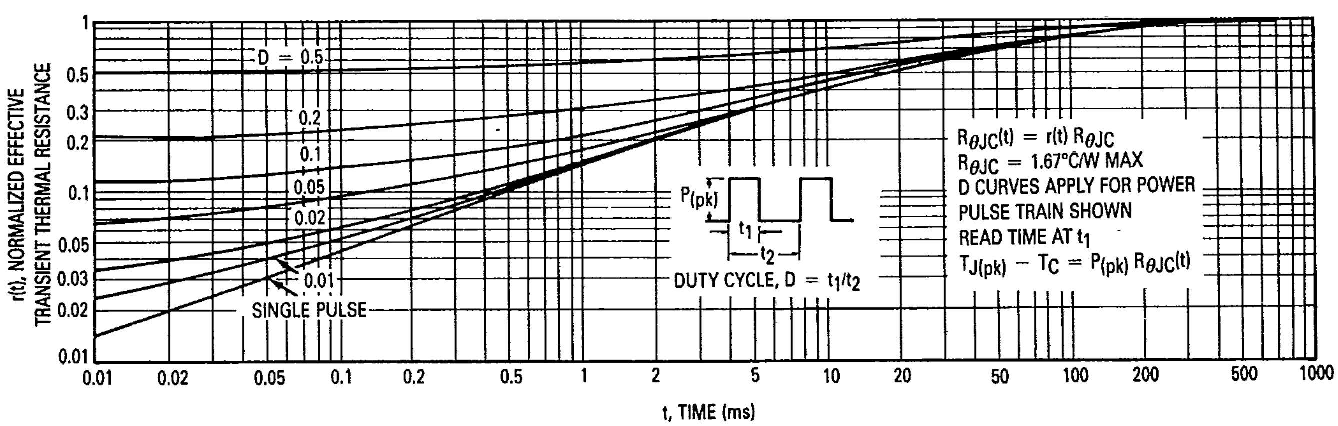
SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Thermal Response



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