# HM5164165A Series
# HM5165165A Series

4194304-word × 16-bit Dynamic RAM

HITACHI

ADE-203-453 (Z)
Preliminary - Rev. 0.4
Apr. 28, 1997

## Description

The Hitachi HM5164165A Series, HM5165165A Series are CMOS dynamic RAMs organized as 4,194,304-word × 16-bit. They employ the most advanced CMOS technology for high performance and low power. HM5164165A Series, HM5165165A Series offer Extended Data Out (EDO) Page Mode as a high speed access mode. They have the package variations of standard 400 mil 50-pin plastic SOJ and standard 400 mil 50-pin plastic TSOPII

## Features

- Single 3.3 V (±0.3 V)
- Access time: 50 ns/60 ns/70 ns (max)
- Power dissipation
  - — Active mode : TBD/450 mW/378 mW (max) (HM5164165A Series)
    : TBD/648 mW/558 mW (max) (HM5165165A Series)
  - — Standby mode : 7.2 mW (max)
    : 0.72 mW (max) (L-version)
- EDO page mode capability
- Refresh cycles
  - — $\overline{\text{RAS}}$-only refresh
    8192 cycles/64 ms (HM5164165A)
    4096 cycles/64 ms (HM5165165A)
    /128 ms (HM5165165AL) (L-version)
  - — CBR/Hidden refresh
    4096 cycles/64 ms (HM5164165A, HM5165165A)
    /128 ms (HM5165165AL) (L-version)
- 4 variations of refresh
  - — $\overline{\text{RAS}}$-only refresh
  - — $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - — Hidden refresh
  - — Self refresh (L-version)

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- 2$\overline{CAS}$-byte control
- Battery backup operation (L-version)

## Ordering Information

| Type No. | Access time | Package |
|---|---|---|
| HM5164165AJ-5 | 50 ns | 400-mil 50-pin plastic SOJ (CP-50DA) |
| HM5164165AJ-6 | 60 ns | |
| HM5164165AJ-7 | 70 ns | |
| HM5164165ALJ-5 | 50 ns | |
| HM5164165ALJ-6 | 60 ns | |
| HM5164165ALJ-7 | 70 ns | |
| HM5165165AJ-5 | 50 ns | |
| HM5165165AJ-6 | 60 ns | |
| HM5165165AJ-7 | 70 ns | |
| HM5165165ALJ-5 | 50 ns | |
| HM5165165ALJ-6 | 60 ns | |
| HM5165165ALJ-7 | 70 ns | |
| HM5164165ATT-5 | 50 ns | 400-mil 50-pin plastic TSOP II (TTP-50DB) |
| HM5164165ATT-6 | 60 ns | |
| HM5164165ATT-7 | 70 ns | |
| HM5164165ALTT-5 | 50 ns | |
| HM5164165ALTT-6 | 60 ns | |
| HM5164165ALTT-7 | 70 ns | |
| HM5165165ATT-5 | 50 ns | |
| HM5165165ATT-6 | 60 ns | |
| HM5165165ATT-7 | 70 ns | |
| HM5165165ALTT-5 | 50 ns | |
| HM5165165ALTT-6 | 60 ns | |
| HM5165165ALTT-7 | 70 ns | |



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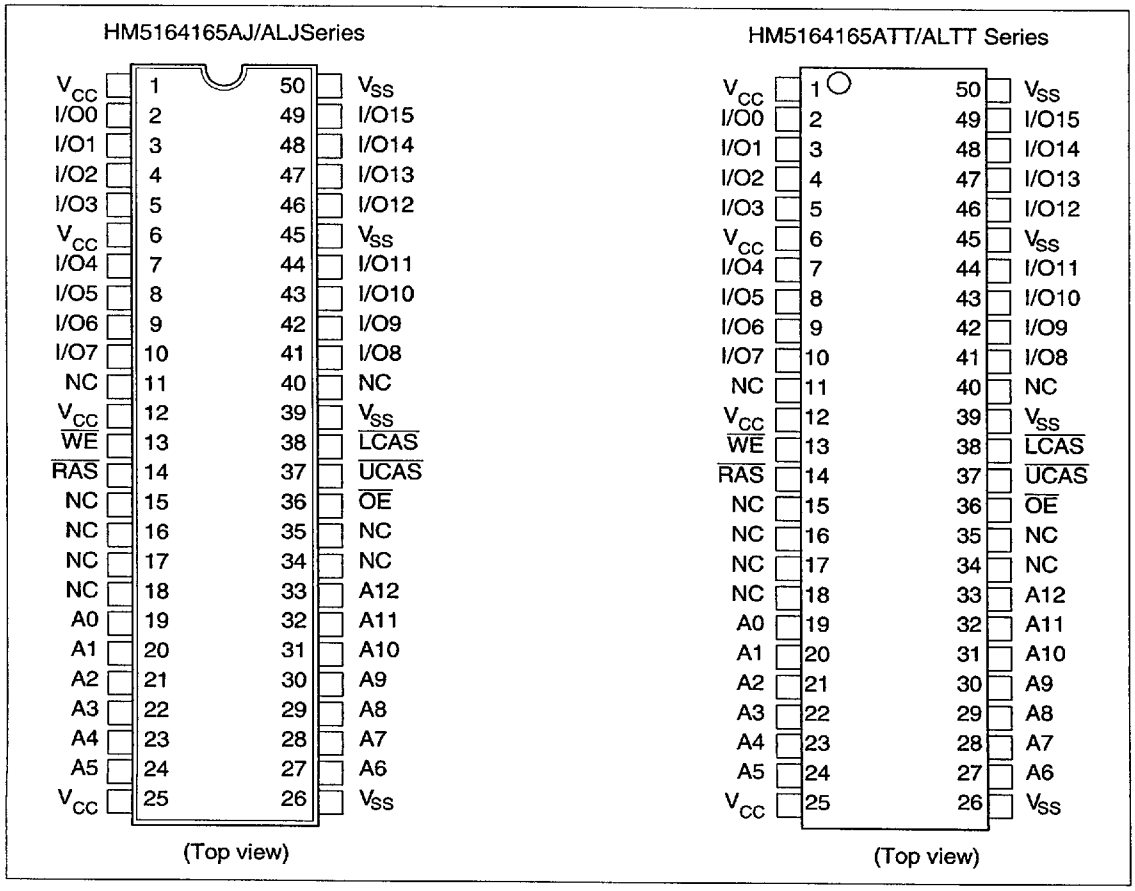
## Pin Arrangement




## Pin Description

| Pin name | Function |
|---|---|
| A0 to A12 | Address input<br>• Row/Refresh address: A0 to A12<br>• Column address: A0 to A8 |
| I/O0 to I/O15 | Data input/Data output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{UCAS}$, $\overline{LCAS}$ | Column address strobe |
| $\overline{WE}$ | Read/Write enable |
| $\overline{OE}$ | Output enable |
| $V_{cc}$ | Power supply |
| $V_{ss}$ | Ground |



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| Pin name | Function |
|---|---|
| NC | No connection |



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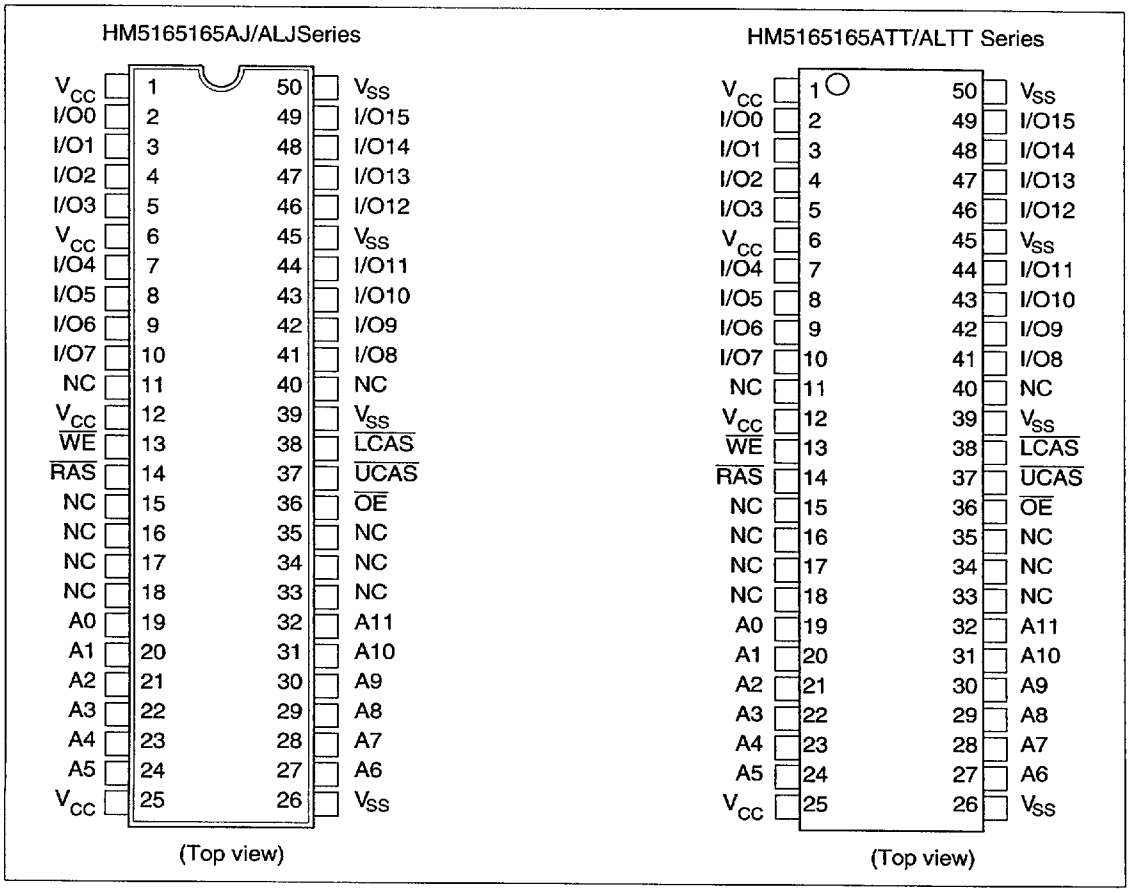
## Pin Arrangement




## Pin Description

| Pin name | Function |
|---|---|
| A0 to A11 | Address input<br>• Row/Refresh address: A0 to A11<br>• Column address: A0 to A9 |
| I/O0 to I/O15 | Data input/Data output |
| $\overline{RAS}$ | Row address strobe |
| $\overline{UCAS}$, $\overline{LCAS}$ | Column address strobe |
| $\overline{WE}$ | Read/Write enable |
| $\overline{OE}$ | Output enable |
| $V_{cc}$ | Power supply |
| $V_{ss}$ | Ground |



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| Pin name | Function |
|---|---|
| NC | No connection |



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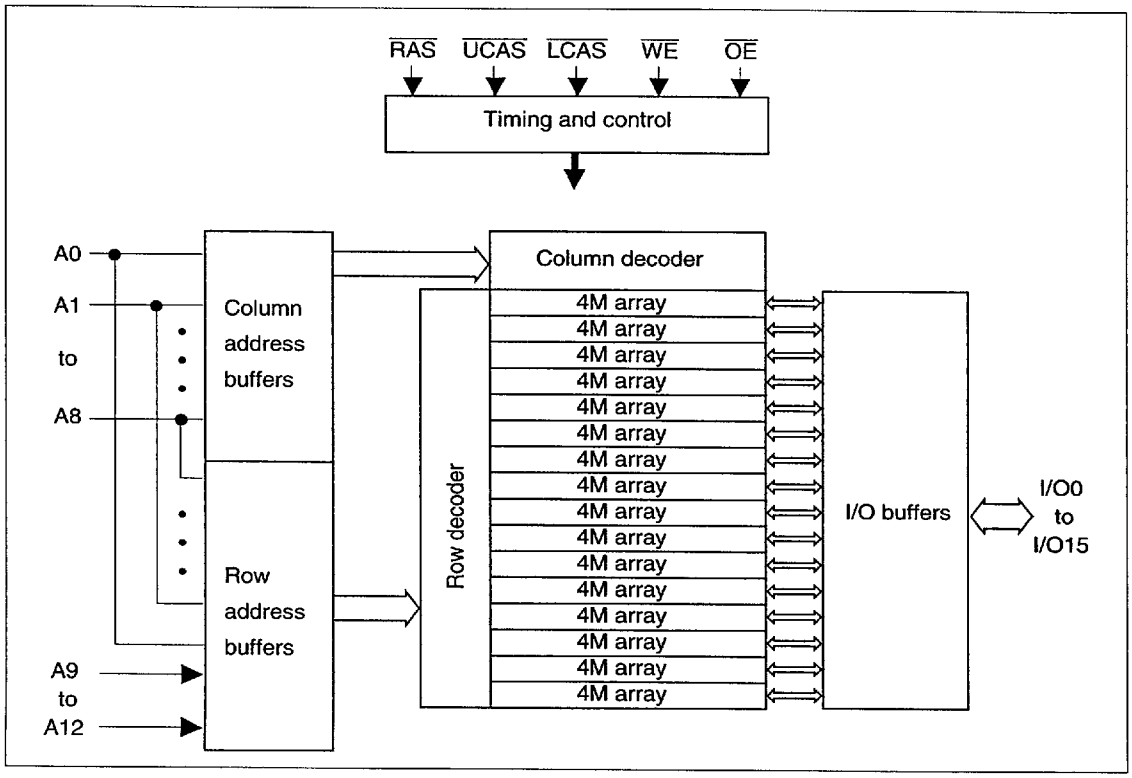
**Block Diagram** (HM5164165A Series)





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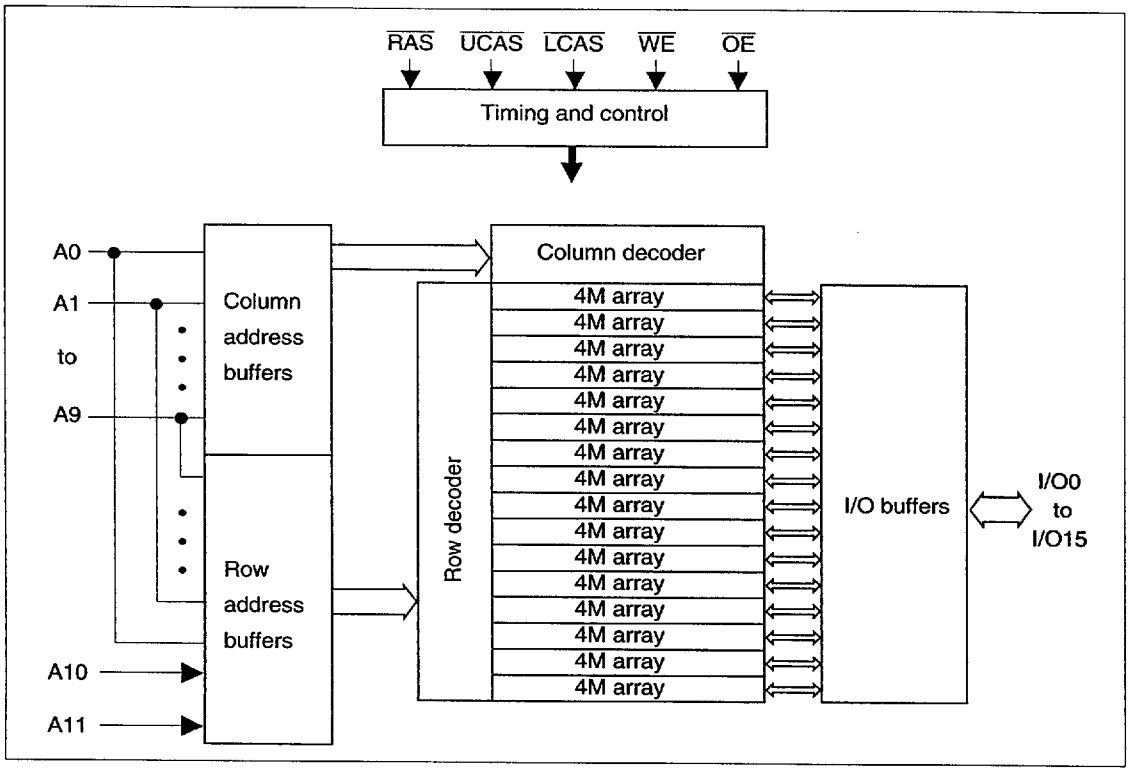
**Block Diagram** (HM5165165A Series)





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## Truth Table

| $\overline{RAS}$ | $\overline{LCAS}$ | $\overline{UCAS}$ | $\overline{WE}$ | $\overline{OE}$ | Output | | Operation |
|---|---|---|---|---|---|---|---|
| H | D | D | D | D | Open | | Standby |
| L | L | H | H | L | Valid | Lower byte | Read cycle |
| L | H | L | H | L | Valid | Upper byte | |
| L | L | L | H | L | Valid | Word | |
| L | L | H | L*2 | D | Open | Lower byte | Early write cycle |
| L | H | L | L*2 | D | Open | Upper byte | |
| L | L | L | L*2 | D | Open | Word | |
| L | L | H | L*2 | H | Undefined | Lower byte | Delayed write cycle |
| L | H | L | L*2 | H | Undefined | Upper byte | |
| L | L | L | L*2 | H | Undefined | Word | |
| L | L | H | H to L | L to H | Valid | Lower byte | Read-modify-write cycle |
| L | H | L | H to L | L to H | Valid | Upper byte | |
| L | L | L | H to L | L to H | Valid | Word | |
| L | H | H | D | D | Open | Word | $\overline{RAS}$-only refresh cycle |
| H to L | H | L | H | D | Open | Word | $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle or |
| H to L | L | H | H | D | Open | Word | Self refresh cycle (L-version) |
| H to L | L | L | H | D | Open | Word | |
| L | L | L | H | H | Open | | Read cycle (Output disabled) |

Notes: 1. H: High (inactive) L: Low (active) D: H or L

2. $t_{WCS} \geq 0$ ns Early write cycle
   $t_{WCS} < 0$ ns Delayed write cycle
3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by the earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.) However write OPERATION and output HIZ control are done independently by each $\overline{UCAS}$, $\overline{LCAS}$.
   ex. if $\overline{RAS}$ = H to L, $\overline{UCAS}$ = H, $\overline{LCAS}$ = L, then $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is selected.



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## Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Voltage on any pin relative to $V_{SS}$ | $V_T$ | −0.5 to $V_{CC}$ + 0.5 (≤ 4.6 V (max)) | V |
| Supply voltage relative to $V_{SS}$ | $V_{CC}$ | −0.5 to +4.6 | V |
| Short circuit output current | Iout | 50 | mA |
| Power dissipation | $P_T$ | 1.0 | W |
| Operating temperature | Topr | 0 to +70 | °C |
| Storage temperature | Tstg | −55 to +125 | °C |

## Recommended DC Operating Conditions (Ta = 0 to +70°C)

| Parameter | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V | 1, 2 |
| Input high voltage | $V_{IH}$ | 2.0 | — | $V_{CC}$ + 0.3 | V | 1 |
| Input low voltage | $V_{IL}$ | −0.3 | — | 0.8 | V | 1 |

Notes: 1. All voltage referred to $V_{SS}$.
2. The supply voltage with all $V_{CC}$ pins must be on the same level. The supply voltage with all $V_{SS}$ pins must be on the same level.



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## DC Characteristics

(Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V) (HM5164165A Series)

| | | HM5164165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test conditions |
| Operating current*1, *2 | $I_{CC1}$ | — | TBD | — | 125 | — | 105 | mA | $t_{RC}$ = min |
| Standby current | $I_{CC2}$ | — | TBD | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = VIH<br>Dout = High-Z |
| | | — | TBD | — | 1 | — | 1 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| Standby current (L-version) | $I_{CC2}$ | — | TBD | — | TBD | — | TBD | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| $\overline{RAS}$-only refresh current*2 | $I_{CC3}$ | — | TBD | — | 125 | — | 105 | mA | $t_{RC}$ = min |
| Standby current*1 | $I_{CC5}$ | — | TBD | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{UCAS}$, $\overline{LCAS}$ = $V_{IL}$<br>Dout = enable |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | TBD | — | 140 | — | 120 | mA | $t_{RC}$ = min |
| EDO page mode current*1, *3 | $I_{CC7}$ | — | TBD | — | 120 | — | 105 | mA | $t_{HPC}$ = min |
| Battery backup current*4 (Standby with CBR refresh) (L-version) | $I_{CC10}$ | — | TBD | — | TBD | — | TBD | µA | CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC}$ = 31.3 µs<br>$t_{RAS}$ ≤ 0.3 µs |
| Self refresh mode current (L-version) | $I_{CC11}$ | — | TBD | — | TBD | — | TBD | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≤ 0.2 V<br>Dout = High-Z |
| Input leakage current | $I_{LI}$ | TBD | TBD | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ $V_{CC}$ + 0.3 V |
| Output leakage current | $I_{LO}$ | TBD | TBD | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vout ≤ $V_{CC}$<br>Dout = disable |
| Output high voltage | $V_{OH}$ | TBD | TBD | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA |
| Output low voltage | $V_{OL}$ | TBD | TBD | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less within one page mode cycle $t_{HPC}$.
4. $V_{IH}$ ≥ $V_{CC}$ – 0.2 V, 0 V ≤ $V_{IL}$ ≤ 0.2 V.



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## DC Characteristics

(Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V) (HM5165165A Series)

| | | HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Test conditions |
| Operating current*1, *2 | $I_{CC1}$ | — | TBD | — | 180 | — | 155 | mA | $t_{RC}$ = min |
| Standby current | $I_{CC2}$ | — | TBD | — | 2 | — | 2 | mA | TTL interface<br>$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = $V_{IH}$<br>Dout = High-Z |
| | | — | TBD | — | 1 | — | 1 | mA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| Standby current (L-version) | $I_{CC2}$ | — | TBD | — | 200 | — | 200 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≥ $V_{CC}$ – 0.2 V<br>Dout = High-Z |
| $\overline{RAS}$-only refresh current*2 | $I_{CC3}$ | — | TBD | — | 180 | — | 155 | mA | $t_{RC}$ = min |
| Standby current*1 | $I_{CC5}$ | — | TBD | — | 5 | — | 5 | mA | $\overline{RAS}$ = $V_{IH}$<br>$\overline{UCAS}$, $\overline{LCAS}$ = $V_{IL}$<br>Dout = enable |
| $\overline{CAS}$-before-$\overline{RAS}$ refresh current | $I_{CC6}$ | — | TBD | — | 140 | — | 120 | mA | $t_{RC}$ = min |
| EDO page mode current*1, *3 | $I_{CC7}$ | — | TBD | — | 150 | — | 135 | mA | $t_{HPC}$ = min |
| Battery backup current*4 (Standby with CBR refresh) (L-version) | $I_{CC10}$ | — | TBD | — | 650 | — | 650 | µA | CMOS interface<br>Dout = High-Z<br>CBR refresh: $t_{RC}$ = 31.3 µs<br>$t_{RAS}$ ≤ 0.3 µs |
| Self refresh mode current (L-version) | $I_{CC11}$ | — | TBD | — | 500 | — | 500 | µA | CMOS interface<br>$\overline{RAS}$, $\overline{UCAS}$,<br>$\overline{LCAS}$ ≤ 0.2 V<br>Dout = High-Z |
| Input leakage current | $I_{LI}$ | TBD | TBD | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vin ≤ $V_{CC}$ + 0.3 V |
| Output leakage current | $I_{LO}$ | TBD | TBD | –10 | 10 | –10 | 10 | µA | 0 V ≤ Vout ≤ $V_{CC}$<br>Dout = disable |
| Output high voltage | $V_{OH}$ | TBD | TBD | 2.4 | $V_{CC}$ | 2.4 | $V_{CC}$ | V | High Iout = –2 mA |
| Output low voltage | $V_{OL}$ | TBD | TBD | 0 | 0.4 | 0 | 0.4 | V | Low Iout = 2 mA |

Notes: 1. $I_{CC}$ depends on output load condition when the device is selected. $I_{CC}$ max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$.
3. Address can be changed once or less within one page mode cycle $t_{HPC}$.
4. $V_{IH}$ ≥ $V_{CC}$ – 0.2 V, 0 V ≤ $V_{IL}$ ≤ 0.2 V.



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**Capacitance** (Ta = 25°C, $V_{CC}$ = 3.3 V ± 0.3 V)

| Parameter | Symbol | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input capacitance (Address) | $C_{I1}$ | — | 5 | pF | 1 |
| Input capacitance (Clocks) | $C_{I2}$ | — | 7 | pF | 1 |
| Output capacitance (Data-in, Data-out) | $C_{I/O}$ | — | 7 | pF | 1, 2 |

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{RAS}$, $\overline{UCAS}$ and $\overline{LCAS}$ = $V_{IH}$ to disable Dout.



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## AC Characteristics (Ta = 0 to +70°C, $V_{CC}$ = 3.3 V ± 0.3 V, $V_{SS}$ = 0 V)*1, *2, *18, *19, *20

### Test Conditions

- Input rise and fall time: 2 ns
- Input levels: 0 V, 3.0 V
- Input timing reference levels: 0.8 V, 2.0 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output load: 1 TTL gate + $C_L$ (100 pF) (Including scope and jig)

### Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

| | | HM5164165A/HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Random read or write cycle time | $t_{RC}$ | TBD | — | 104 | — | 124 | — | ns | |
| $\overline{RAS}$ precharge time | $t_{RP}$ | TBD | — | 40 | — | 50 | — | ns | |
| $\overline{CAS}$ precharge time | $t_{CP}$ | TBD | — | 10 | — | 13 | — | ns | |
| $\overline{RAS}$ pulse width | $t_{RAS}$ | TBD | TBD | 60 | 10000 | 70 | 10000 | ns | |
| $\overline{CAS}$ pulse width | $t_{CAS}$ | TBD | TBD | 10 | 10000 | 13 | 10000 | ns | |
| Row address setup time | $t_{ASR}$ | TBD | — | 0 | — | 0 | — | ns | |
| Row address hold time | $t_{RAH}$ | TBD | — | 10 | — | 10 | — | ns | |
| Column address setup time | $t_{ASC}$ | TBD | — | 0 | — | 0 | — | ns | 21 |
| Column address hold time | $t_{CAH}$ | TBD | — | 10 | — | 13 | – | ns | 21 |
| $\overline{RAS}$ to $\overline{CAS}$ delay time | $t_{RCD}$ | TBD | TBD | 20 | 45 | 20 | 52 | ns | 3 |
| $\overline{RAS}$ to column address delay time | $t_{RAD}$ | TBD | TBD | 15 | 30 | 15 | 35 | ns | 4 |
| $\overline{RAS}$ hold time | $t_{RSH}$ | TBD | — | 15 | — | 18 | — | ns | |
| $\overline{CAS}$ hold time | $t_{CSH}$ | TBD | — | 48 | — | 58 | — | ns | 23 |
| $\overline{CAS}$ to $\overline{RAS}$ precharge time | $t_{CRP}$ | TBD | — | 5 | — | 5 | — | ns | 22 |
| $\overline{OE}$ to Din delay time | $t_{OED}$ | TBD | — | 15 | — | 18 | — | ns | 5 |
| $\overline{OE}$ delay time from Din | $t_{DZO}$ | TBD | — | 0 | — | 0 | — | ns | 6 |
| $\overline{CAS}$ delay time from Din | $t_{DZC}$ | TBD | — | 0 | — | 0 | — | ns | 6 |
| Transition time (rise and fall) | $t_T$ | TBD | TBD | 2 | 50 | 2 | 50 | ns | 7 |



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**Read Cycle**

| | | HM5164165A/HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| **Parameter** | **Symbol** | **Min** | **Max** | **Min** | **Max** | **Min** | **Max** | **Unit** | **Notes** |
| Access time from $\overline{RAS}$ | $t_{RAC}$ | — | TBD | — | 60 | — | 70 | ns | 8, 9 |
| Access time from $\overline{CAS}$ | $t_{CAC}$ | — | TBD | — | 15 | — | 18 | ns | 9, 10, 17 |
| Access time from address | $t_{AA}$ | — | TBD | — | 30 | — | 35 | ns | 9, 11, 17 |
| Access time from $\overline{OE}$ | $t_{OEA}$ | — | TBD | — | 15 | — | 18 | ns | 9 |
| Read command setup time | $t_{RCS}$ | TBD | — | 0 | — | 0 | — | ns | 21 |
| Read command hold time to $\overline{CAS}$ | $t_{RCH}$ | TBD | — | 0 | — | 0 | — | ns | 12, 22 |
| Read command hold time from $\overline{RAS}$ | $t_{RCHR}$ | TBD | — | 60 | — | 70 | — | ns | |
| Read command hold time to $\overline{RAS}$ | $t_{RRH}$ | TBD | — | 0 | — | 0 | — | ns | 12 |
| Column address to $\overline{RAS}$ lead time | $t_{RAL}$ | TBD | — | 30 | — | 35 | — | ns | |
| Column address to $\overline{CAS}$ lead time | $t_{CAL}$ | TBD | — | 18 | — | 23 | — | ns | |
| $\overline{CAS}$ to output in low-Z | $t_{CLZ}$ | TBD | — | 0 | — | 0 | — | ns | |
| Output data hold time | $t_{OH}$ | TBD | — | 3 | — | 3 | — | ns | 27 |
| Output data hold time from $\overline{OE}$ | $t_{OHO}$ | TBD | — | 3 | — | 3 | — | ns | |
| Output buffer turn-off time | $t_{OFF}$ | — | TBD | — | 15 | — | 15 | ns | 13, 27 |
| Output buffer turn-off to $\overline{OE}$ | $t_{OEZ}$ | — | TBD | — | 15 | — | 15 | ns | 13 |
| $\overline{CAS}$ to Din delay time | $t_{CDD}$ | TBD | — | 15 | — | 18 | — | ns | 5 |
| Output data hold time from $\overline{RAS}$ | $t_{OHR}$ | TBD | — | 3 | — | 3 | — | ns | 27 |
| Output buffer turn-off to $\overline{RAS}$ | $t_{OFR}$ | — | TBD | — | 15 | — | 15 | ns | 27 |
| Output buffer turn-off to $\overline{WE}$ | $t_{WEZ}$ | — | TBD | — | 15 | — | 15 | ns | |
| $\overline{WE}$ to Din delay time | $t_{WED}$ | TBD | — | 15 | — | 18 | — | ns | |
| $\overline{RAS}$ to Din delay time | $t_{RDD}$ | TBD | — | 15 | — | 18 | — | ns | |



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### Write Cycle

| | | HM5164165A/HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Write command setup time | $t_{WCS}$ | TBD | — | 0 | — | 0 | — | ns | 14, 21 |
| Write command hold time | $t_{WCH}$ | TBD | — | 10 | — | 13 | — | ns | 21 |
| Write command pulse width | $t_{WP}$ | TBD | — | 10 | — | 10 | — | ns | |
| Write command to $\overline{RAS}$ lead time | $t_{RWL}$ | TBD | — | 10 | — | 13 | — | ns | |
| Write command to $\overline{CAS}$ lead time | $t_{CWL}$ | TBD | — | 10 | — | 13 | — | ns | 23 |
| Data-in setup time | $t_{DS}$ | TBD | — | 0 | — | 0 | — | ns | 15, 23 |
| Data-in hold time | $t_{DH}$ | TBD | — | 10 | — | 13 | — | ns | 15, 23 |

### Read-Modify-Write Cycle

| | | HM5164165A/HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| Read-modify-write cycle time | $t_{RWC}$ | TBD | — | 149 | — | 175 | — | ns | |
| $\overline{RAS}$ to $\overline{WE}$ delay time | $t_{RWD}$ | TBD | — | 78 | — | 91 | — | ns | 14 |
| $\overline{CAS}$ to $\overline{WE}$ delay time | $t_{CWD}$ | TBD | — | 33 | — | 39 | — | ns | 14 |
| Column address to $\overline{WE}$ delay time | $t_{AWD}$ | TBD | — | 48 | — | 56 | — | ns | 14 |
| $\overline{OE}$ hold time from $\overline{WE}$ | $t_{OEH}$ | TBD | — | 15 | — | 18 | — | ns | |

### Refresh Cycle

| | | HM5164165A/HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| $\overline{CAS}$ setup time (CBR refresh cycle) | $t_{CSR}$ | TBD | — | 5 | — | 5 | — | ns | 21 |
| $\overline{CAS}$ hold time (CBR refresh cycle) | $t_{CHR}$ | TBD | — | 10 | — | 10 | — | ns | 22 |
| $\overline{WE}$ setup time (CBR refresh cycle) | $t_{WRP}$ | TBD | — | 0 | — | 0 | — | ns | |
| $\overline{WE}$ hold time (CBR refresh cycle) | $t_{WRH}$ | TBD | — | 10 | — | 10 | — | ns | |
| $\overline{RAS}$ precharge to $\overline{CAS}$ hold time | $t_{RPC}$ | TBD | — | 0 | — | 0 | — | ns | 21 |



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### EDO Page Mode Cycle

| | | HM5164165A/HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| EDO page mode cycle time | $t_{HPC}$ | TBD | — | 25 | — | 30 | — | ns | 25 |
| EDO page mode $\overline{RAS}$ pulse width | $t_{RASP}$ | — | TBD | — | 100000 | — | 100000 | ns | 16 |
| Access time from $\overline{CAS}$ precharge | $t_{CPA}$ | — | TBD | — | 35 | — | 40 | ns | 9, 17 |
| $\overline{RAS}$ hold time from $\overline{CAS}$ precharge | $t_{CPRH}$ | TBD | — | 35 | — | 40 | — | ns | |
| Output data hold time from $\overline{CAS}$ low | $t_{DOH}$ | TBD | — | 3 | — | 3 | — | ns | 9, 17 |
| $\overline{CAS}$ hold time referred $\overline{OE}$ | $t_{COL}$ | TBD | — | 10 | — | 13 | — | ns | |
| $\overline{CAS}$ to $\overline{OE}$ setup time | $t_{COP}$ | TBD | — | 10 | — | 10 | — | ns | |
| Read command hold time from $\overline{CAS}$ precharge | $t_{RCHC}$ | TBD | — | 35 | — | 40 | — | ns | |
| Write pulse width during $\overline{CAS}$ precharge | $t_{WPE}$ | TBD | — | 10 | — | 10 | — | ns | |
| $\overline{OE}$ precharge time | $t_{OEP}$ | TBD | — | 10 | — | 10 | — | ns | |

### EDO Page Mode Read-Modify-Write Cycle

| | | HM5164165A/HM5165165A | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | -5 | | -6 | | -7 | | | |
| Parameter | Symbol | Min | Max | Min | Max | Min | Max | Unit | Notes |
| EDO page mode read-modify-write cycle time | $t_{HPRWC}$ | TBD | — | 68 | — | 79 | — | ns | |
| $\overline{WE}$ delay time from $\overline{CAS}$ precharge | $t_{CPW}$ | TBD | — | 54 | — | 62 | — | ns | 14 |

### Refresh (HM5164165A Series)

| Parameter | Symbol | Max | Unit | Note |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 64 | ms | 8192 cycles |
| Refresh period (L-version) | $t_{REF}$ | TBD | ms | 8192 cycles |



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**Refresh** (HM5165165A Series)

| Parameter | Symbol | Max | Unit | Note |
|---|---|---|---|---|
| Refresh period | $t_{REF}$ | 64 | ms | 4096 cycles |
| Refresh period (L-version) | $t_{REF}$ | 128 | ms | 4096 cycles |



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**Self Refresh Mode** (L-version)

| Parameter | Symbol | HM5165165AL -5 Min | -5 Max | -6 Min | -6 Max | -7 Min | -7 Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| $\overline{RAS}$ pulse width (self refresh) | $t_{RASS}$ | TBD | — | 100 | — | 100 | — | µs | |
| $\overline{RAS}$ precharge time (self refresh) | $t_{RPS}$ | TBD | — | 110 | — | 130 | — | ns | |
| $\overline{CAS}$ hold time (self refresh) | $t_{CHS}$ | TBD | — | –50 | — | –50 | — | ns | |

Notes:
1. AC measurements assume $t_T$ = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Operation with the $t_{RCD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RCD}$ (max) is specified as a reference point only; if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, than the access time is controlled exclusively by $t_{CAC}$.
4. Operation with the $t_{RAD}$ (max) limit insures that $t_{RAC}$ (max) can be met, $t_{RAD}$ (max) is specified as a reference point only; if $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled exclusively by $t_{AA}$.
5. Either $t_{OED}$ or $t_{CDD}$ must be satisfied.
6. Either $t_{DZO}$ or $t_{DZC}$ must be satisfied.
7. $V_{IH}$ (min) and $V_{IL}$ (max) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).
8. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If $t_{RCD}$ or $t_{RAD}$ is greater than the maximum recommended value shown in this table, $t_{RAC}$ exceeds the value shown.
9. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
10. Assumes that $t_{RCD} \geq t_{RCD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\geq t_{RAD} + t_{AA}$ (max).
11. Assumes that $t_{RAD} \geq t_{RAD}$ (max) and $t_{RCD} + t_{CAC}$ (max) $\leq t_{RAD} + t_{AA}$ (max).
12. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycles.
13. $t_{OFF}$ (max), $t_{OEZ}$ (max), $t_{WEZ}$ (max) and $t_{OFR}$ (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
14. $t_{WCS}$, $t_{RWD}$, $t_{CWD}$, $t_{AWD}$ and $t_{CPW}$ are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
15. These parameters are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
16. $t_{RASP}$ defines $\overline{RAS}$ pulse width in EDO page mode cycles.
17. Access time is determined by the longest among $t_{AA}$, $t_{CAC}$ and $t_{CPA}$.
18. When both $\overline{UCAS}$ and $\overline{LCAS}$ go low at the same time, all 16-bit data are written into the device. $\overline{UCAS}$ and $\overline{LCAS}$ cannot be staggered within the same write/read cycles.
19 All the $V_{CC}$ and $V_{SS}$ pins shall be supplied with the same voltages.
20. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
21. $t_{ASC}$, $t_{CAH}$, $t_{RCS}$, $t_{WCS}$, $t_{WCH}$, $t_{CSR}$ and $t_{RPC}$ are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
22. $t_{CRP}$, $t_{CHR}$, $t_{RCH}$, $t_{CPA}$ and $t_{CPW}$ are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
23. $t_{CWL}$, $t_{DH}$, $t_{DS}$ and $t_{CSH}$ should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.



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24. $t_{CP}$ is determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
25. $t_{HPC}$ (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle ($t_{CAS} + t_{CP} + 2\ t_T$) becomes greater than the specified $t_{HPC}$ (min) value. The value of $\overline{CAS}$ cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
26. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large $V_{CC}/V_{SS}$ line noise, which causes to degrade $V_{IH}$ min/$V_{IL}$ max level.
27. Data output turns off and becomes high impedance from later rising edge of $\overline{RAS}$ and $\overline{CAS}$. Hold time and turn off time are specified by the timing specifications of later rising edge of $\overline{RAS}$ and $\overline{CAS}$ between $t_{OHR}$ and $t_{OH}$, and between $t_{OFR}$ and $t_{OFF}$.
28. Please do not use $t_{RASS}$ timing, 10 µs ≤ $t_{RASS}$ ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS}$ ≥ 100 µs, then $\overline{RAS}$ precharge time should use $t_{RPS}$ instead of $t_{RP}$.
29. CBR burst refresh or 4096 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 64 ms immediately after exiting from and before entering into the self refresh mode.
30. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.
31. XXX: H or L (H: $V_{IH}$ (min) ≤ $V_{IN}$ ≤ $V_{IH}$ (max), L: $V_{IL}$ (min) ≤ $V_{IN}$ ≤ $V_{IL}$ (max))
    ///////: Invalid Dout
    When the address, clock and input pins are not described on timing waveforms, their pins must be applied $V_{IH}$ or $V_{IL}$.



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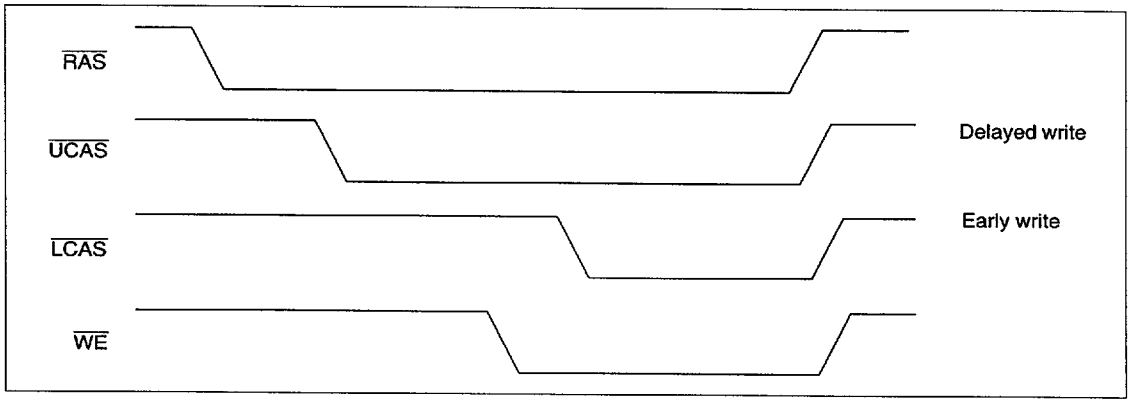
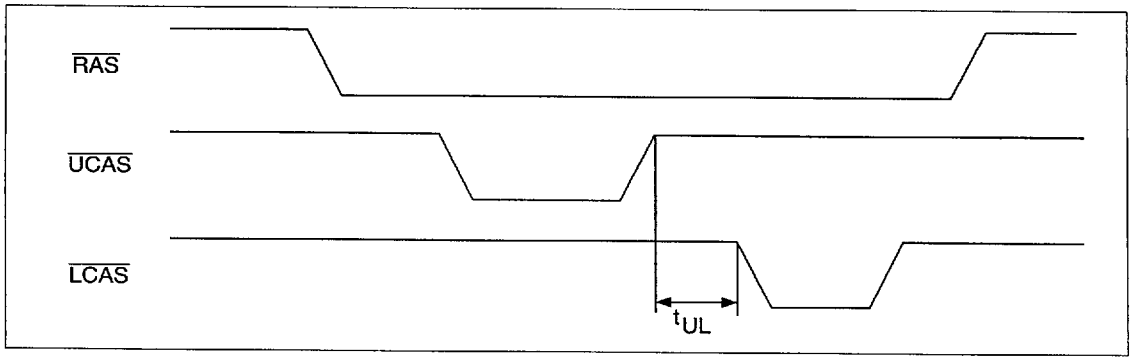
## Notes concerning 2$\overline{CAS}$ control

Please do not separate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$/$\overline{LCAS}$ are allowed under the following conditions.

1. Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.
2. Different operation mode for upper/lower byte is not allowed; such as following.




3. Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, EDO page mode can be performed.




4. Byte control operation by remaining $\overline{UCAS}$ or $\overline{LCAS}$ high is guaranteed.





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## Timing Waveforms*[31]

### Read Cycle



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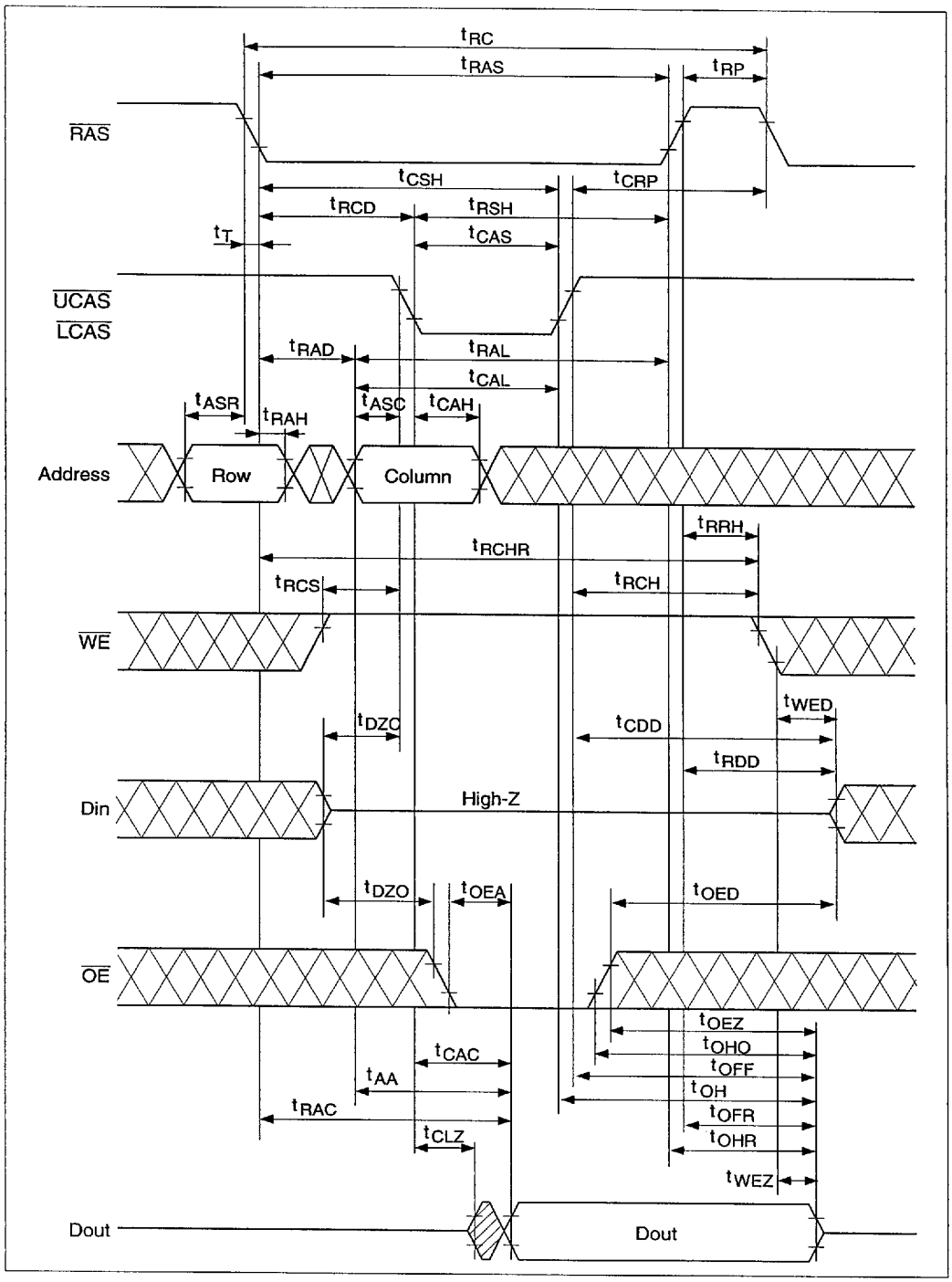






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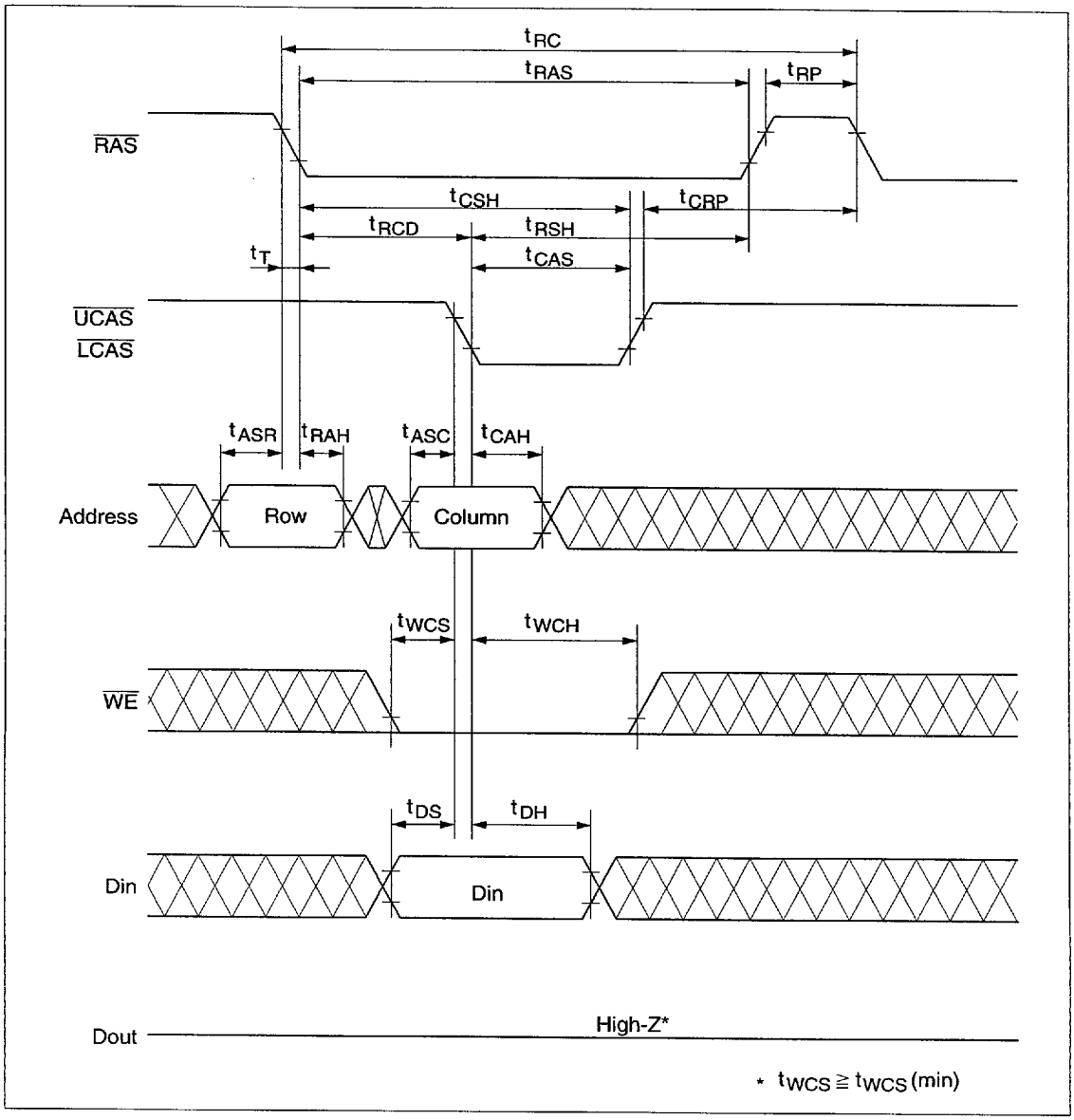
**Early Write Cycle**



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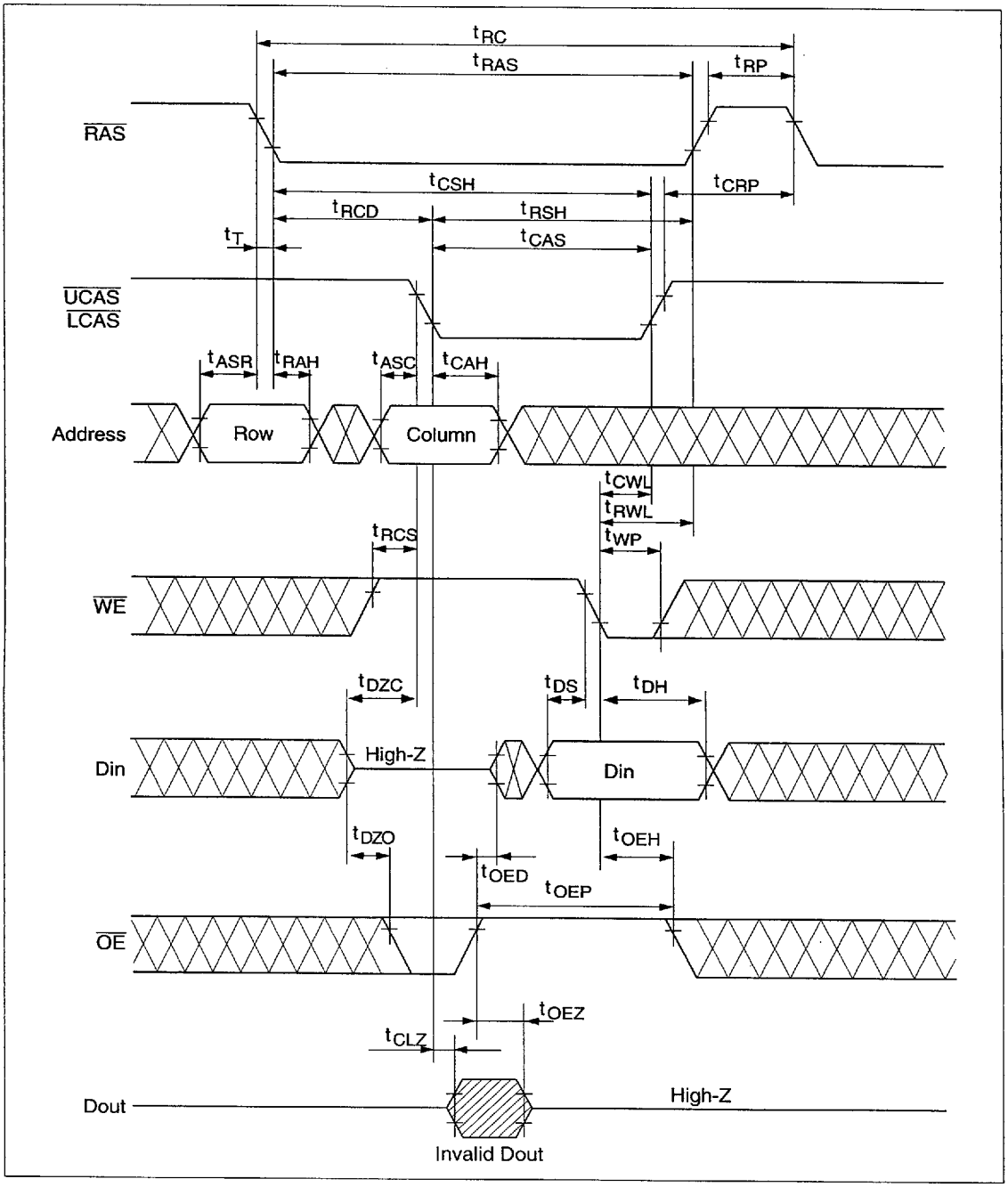
**Delayed Write Cycle*[20]**





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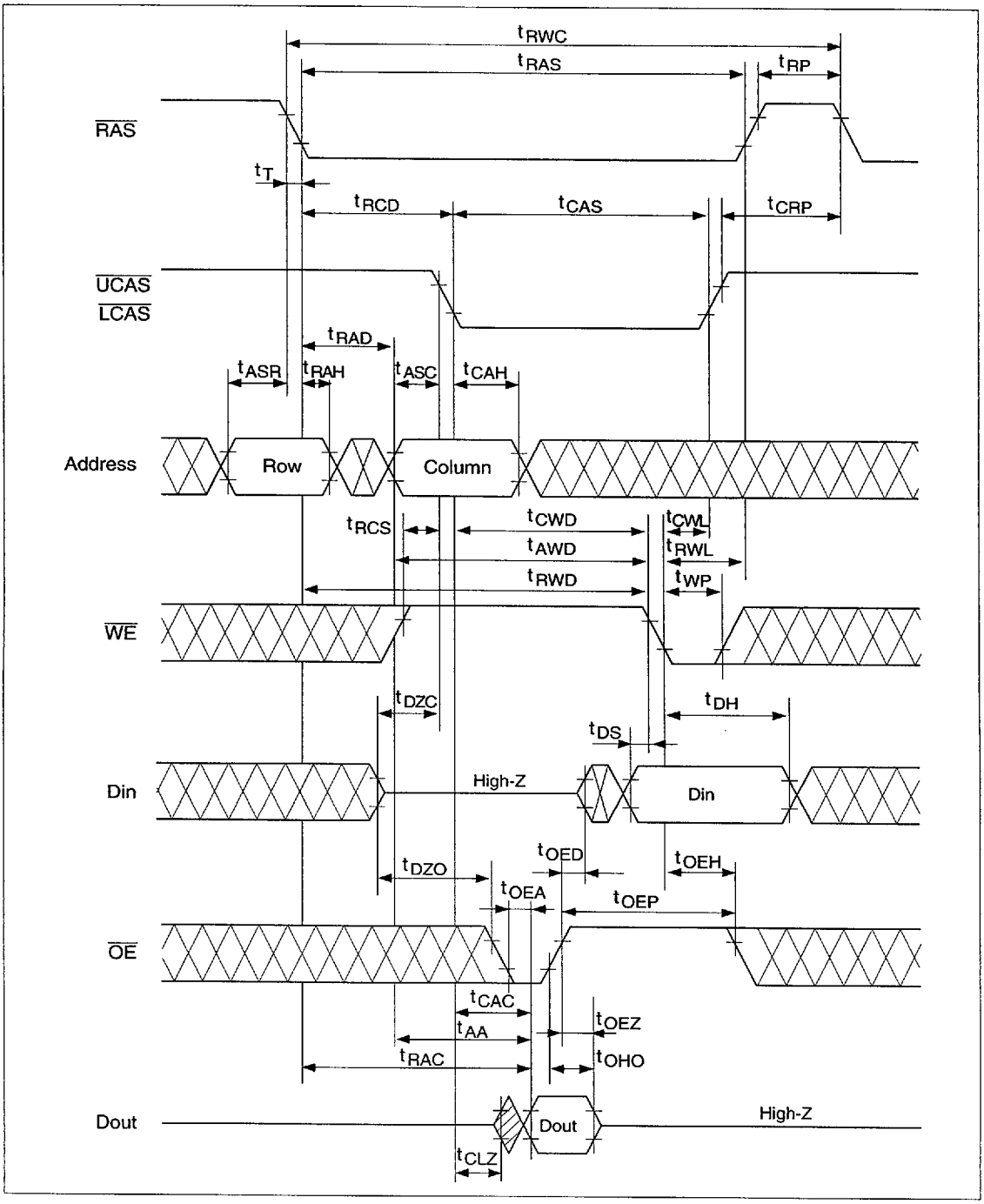
**Read-Modify-Write Cycle*[20]**



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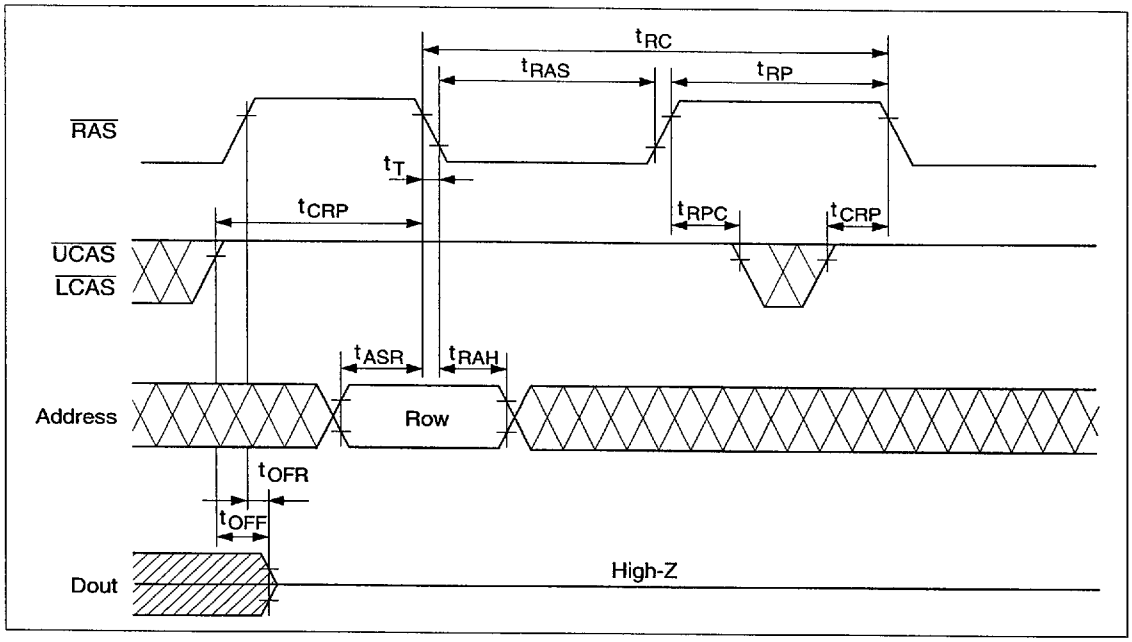
**$\overline{\text{RAS}}$-Only Refresh Cycle**



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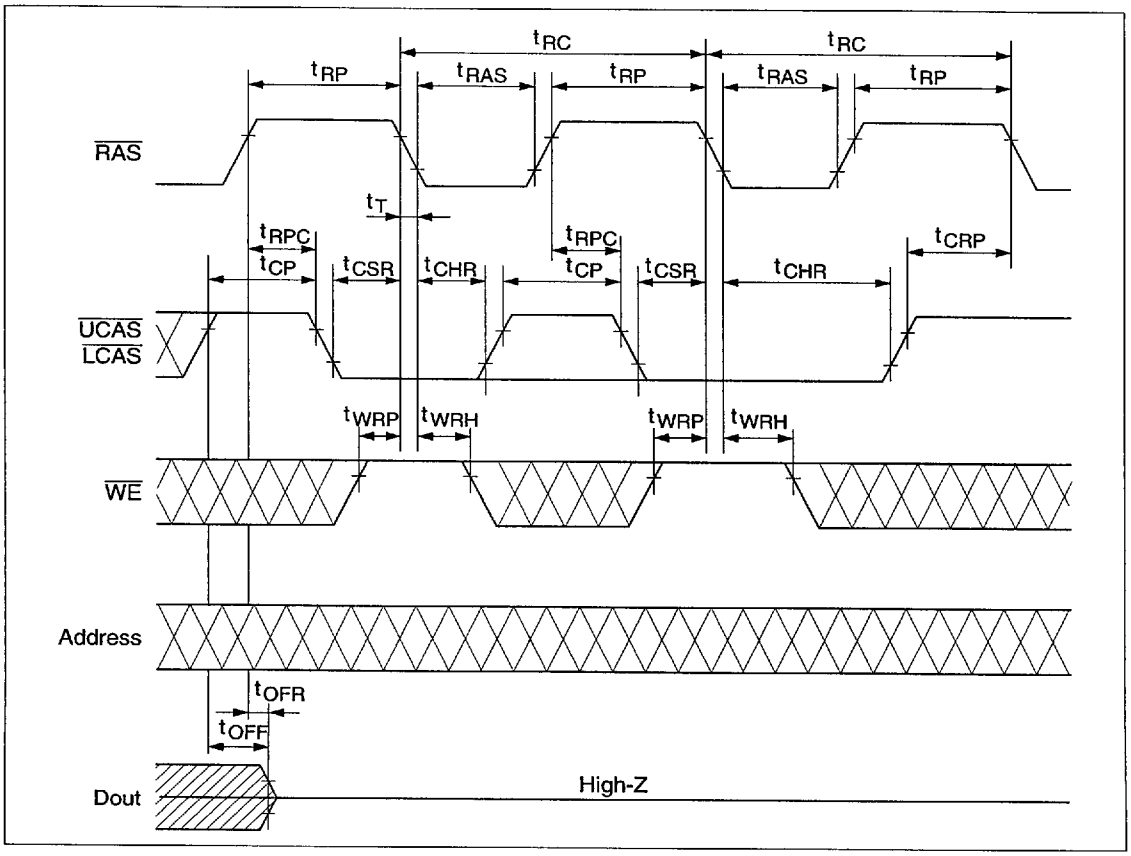
### $\overline{\text{CAS}}$-Before-$\overline{\text{RAS}}$ Refresh Cycle



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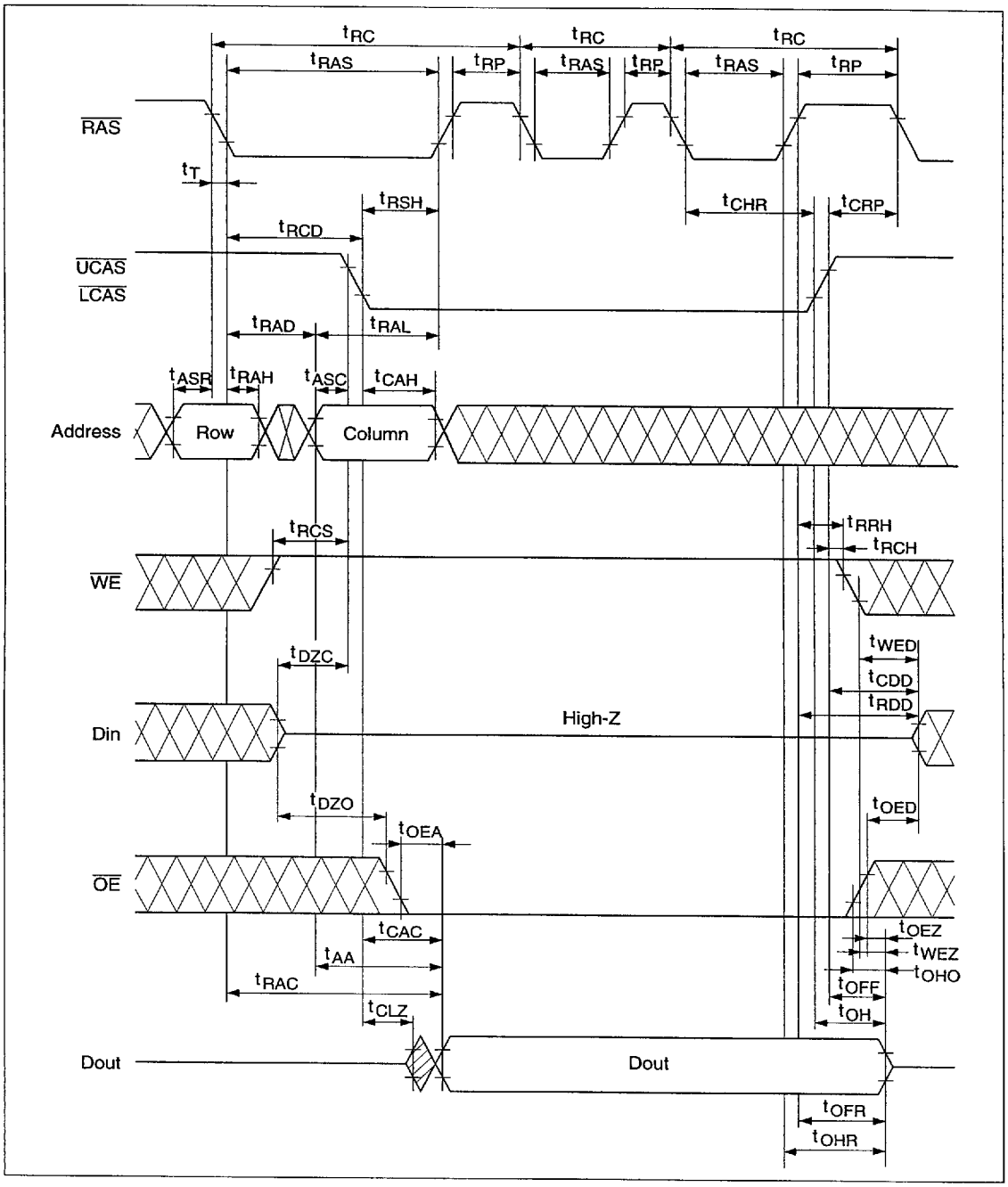
**Hidden Refresh Cycle**



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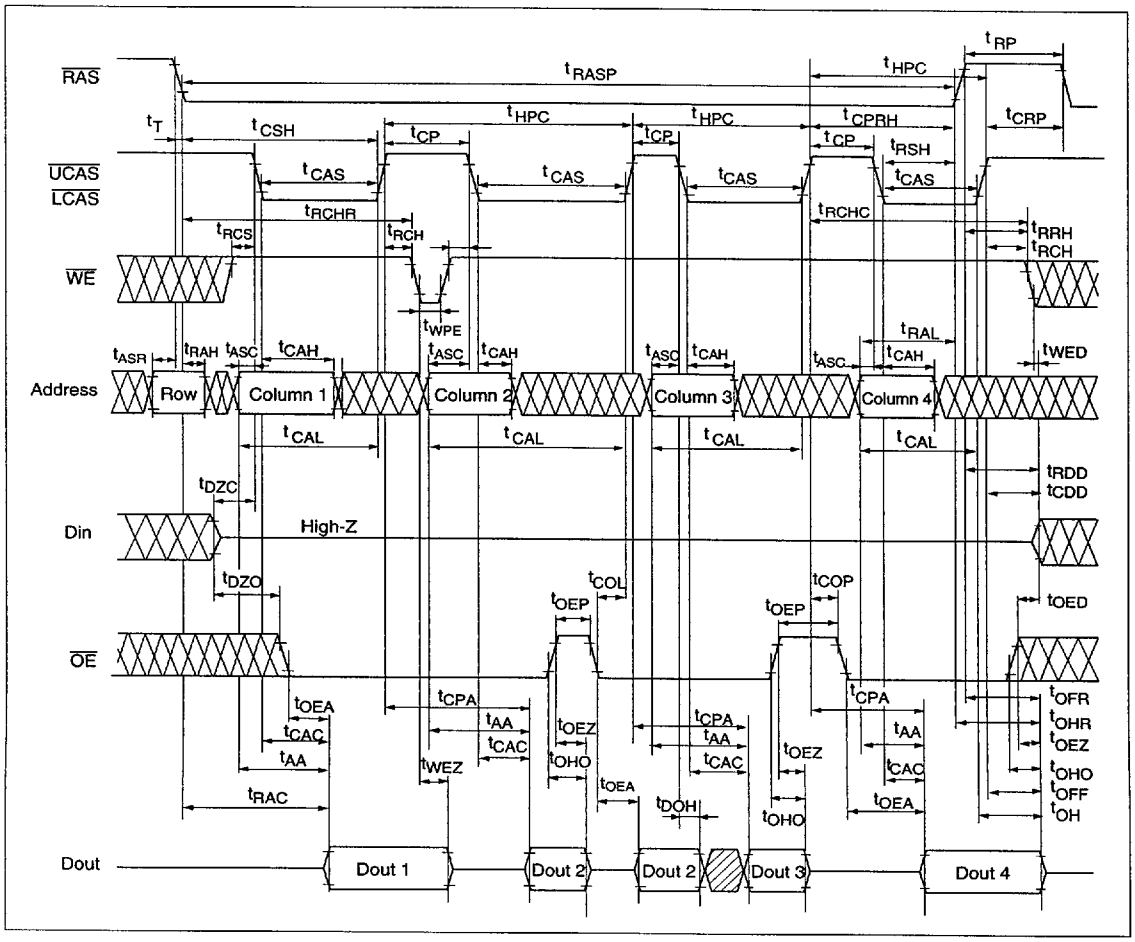
**EDO Page Mode Read Cycle**





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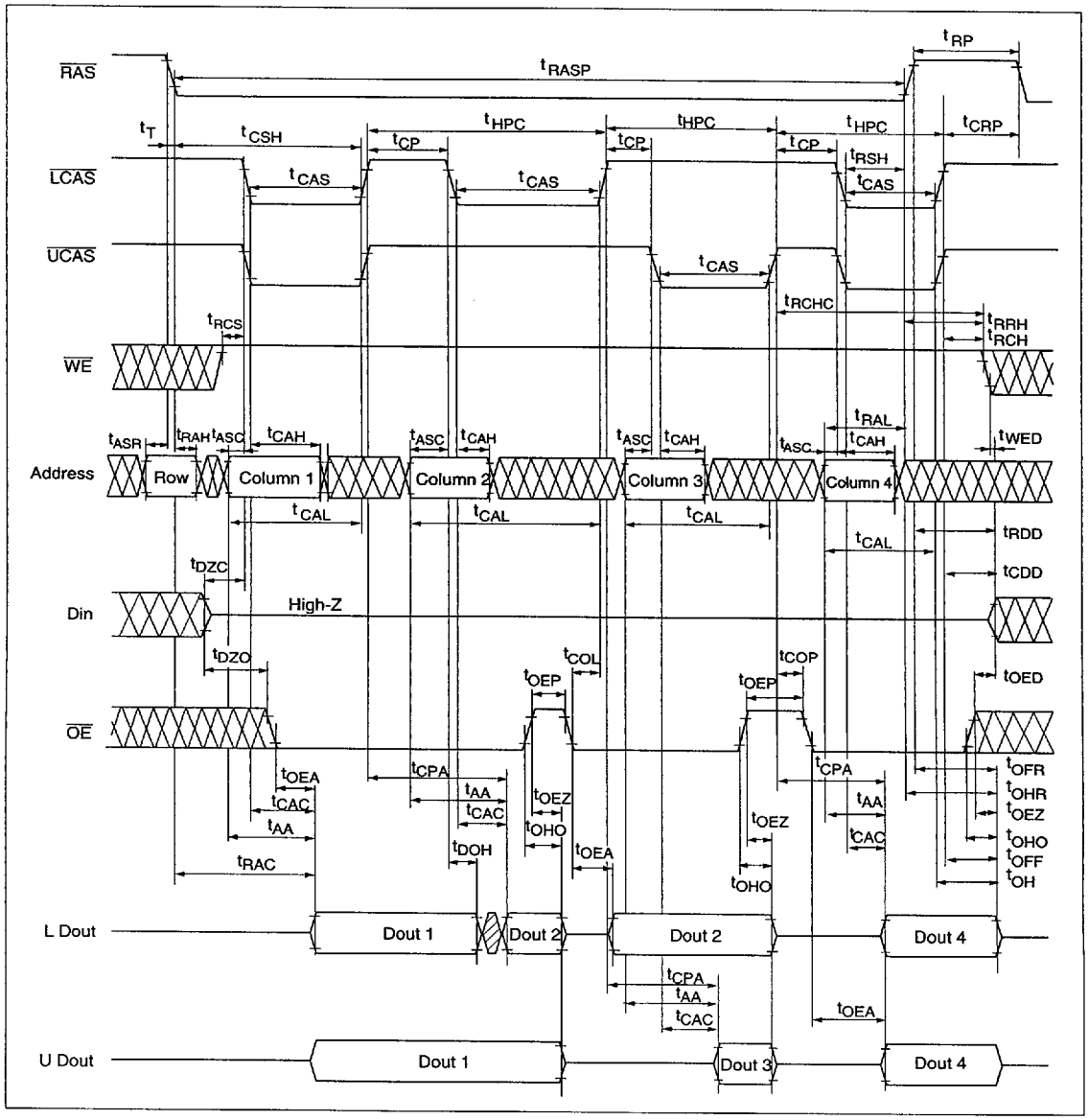
**EDO Page Mode Read Cycle** ($2\overline{CAS}$)





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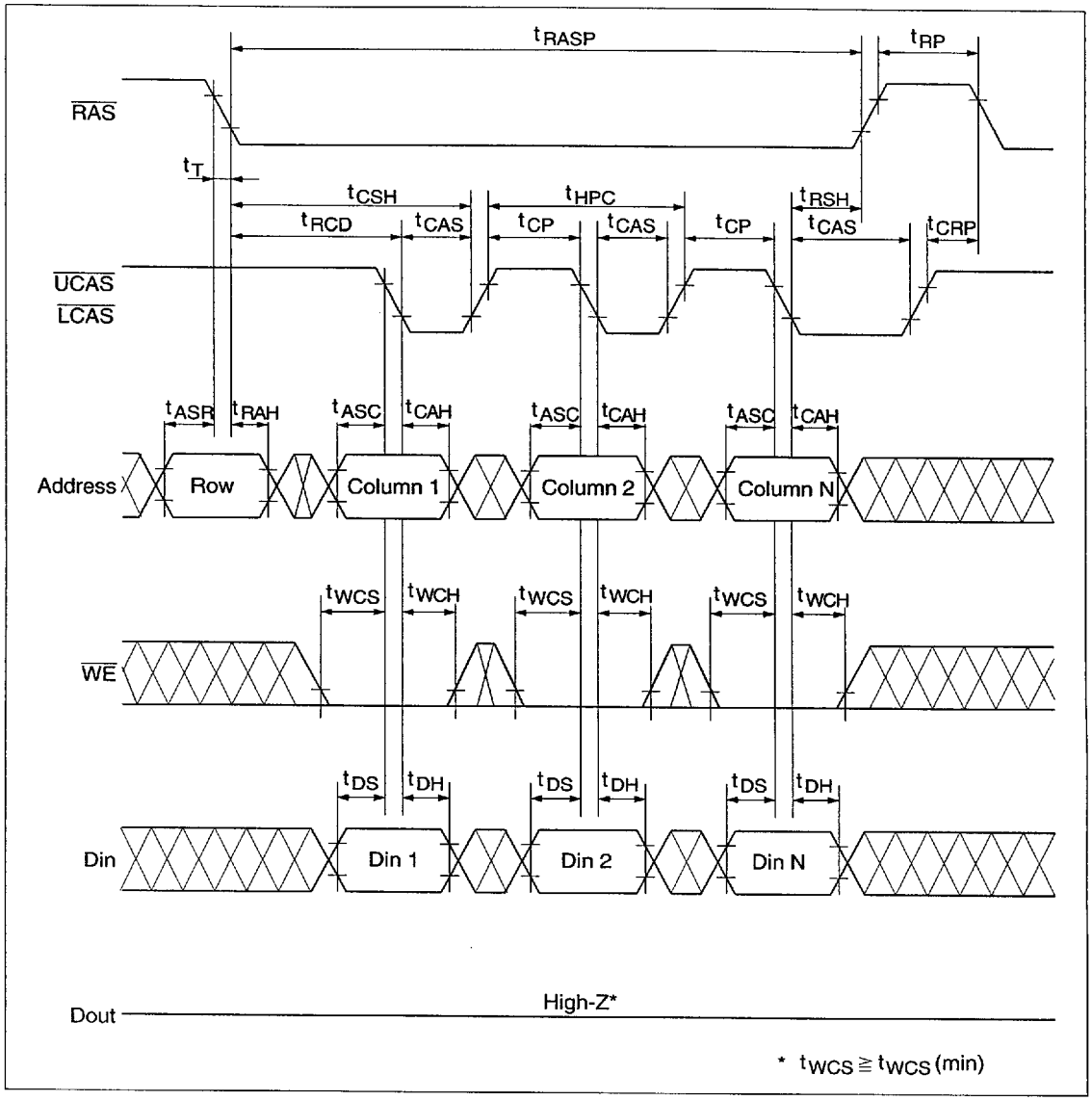
**EDO Page Mode Early Write Cycle**





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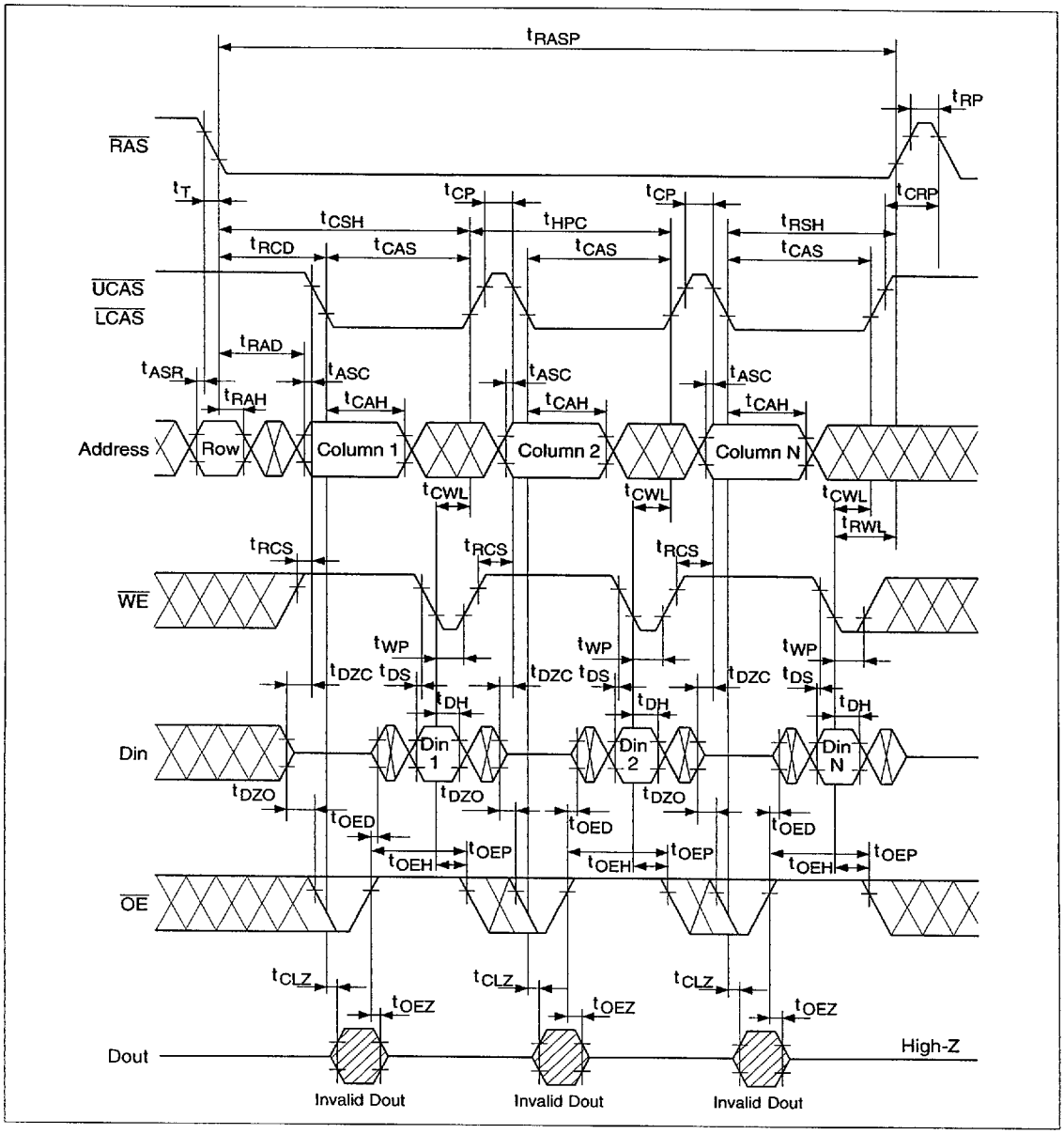
**EDO Page Mode Delayed Write Cycle*[20]**



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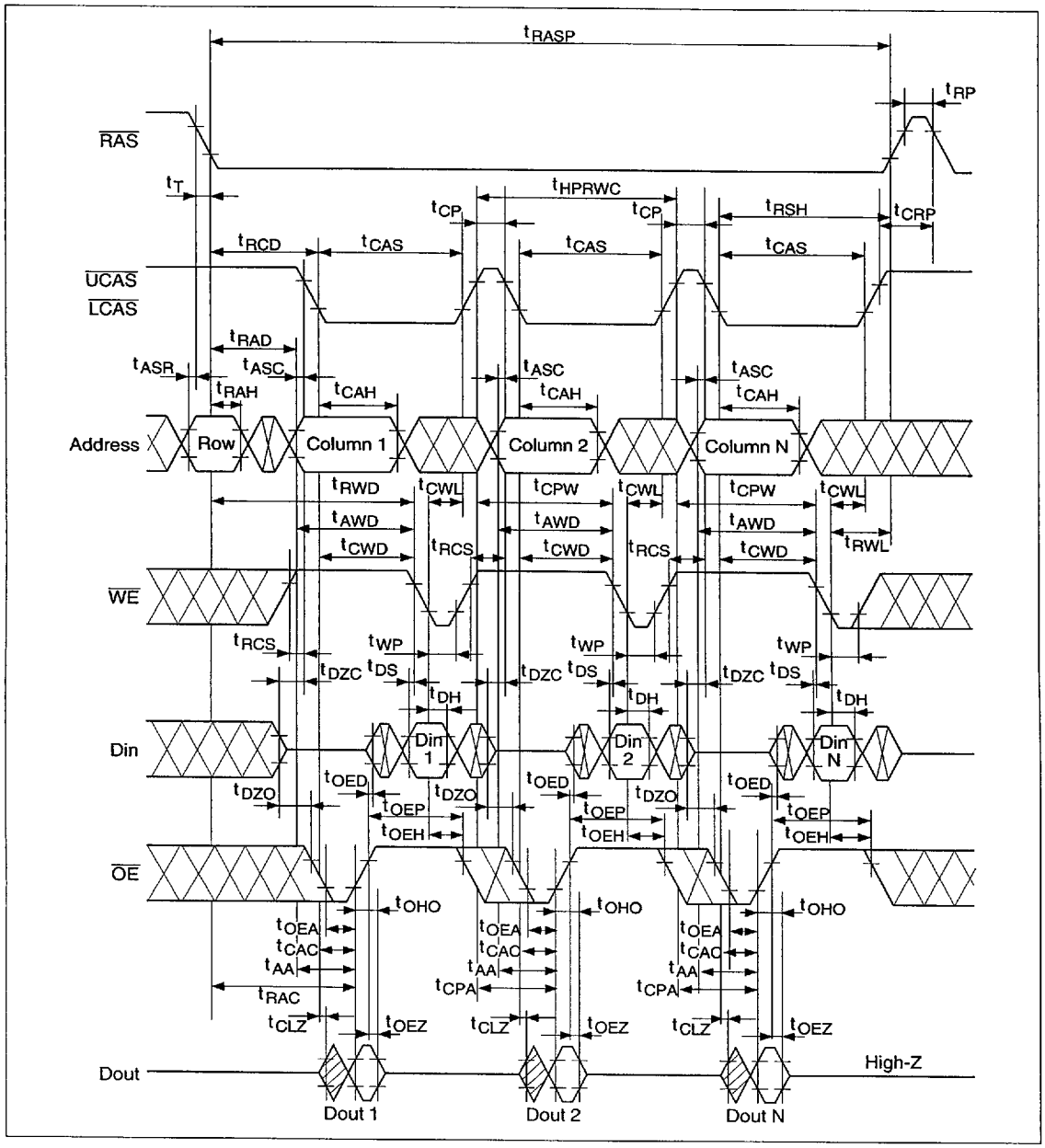
**EDO Page Mode Read-Modify-Write Cycle*[20]**



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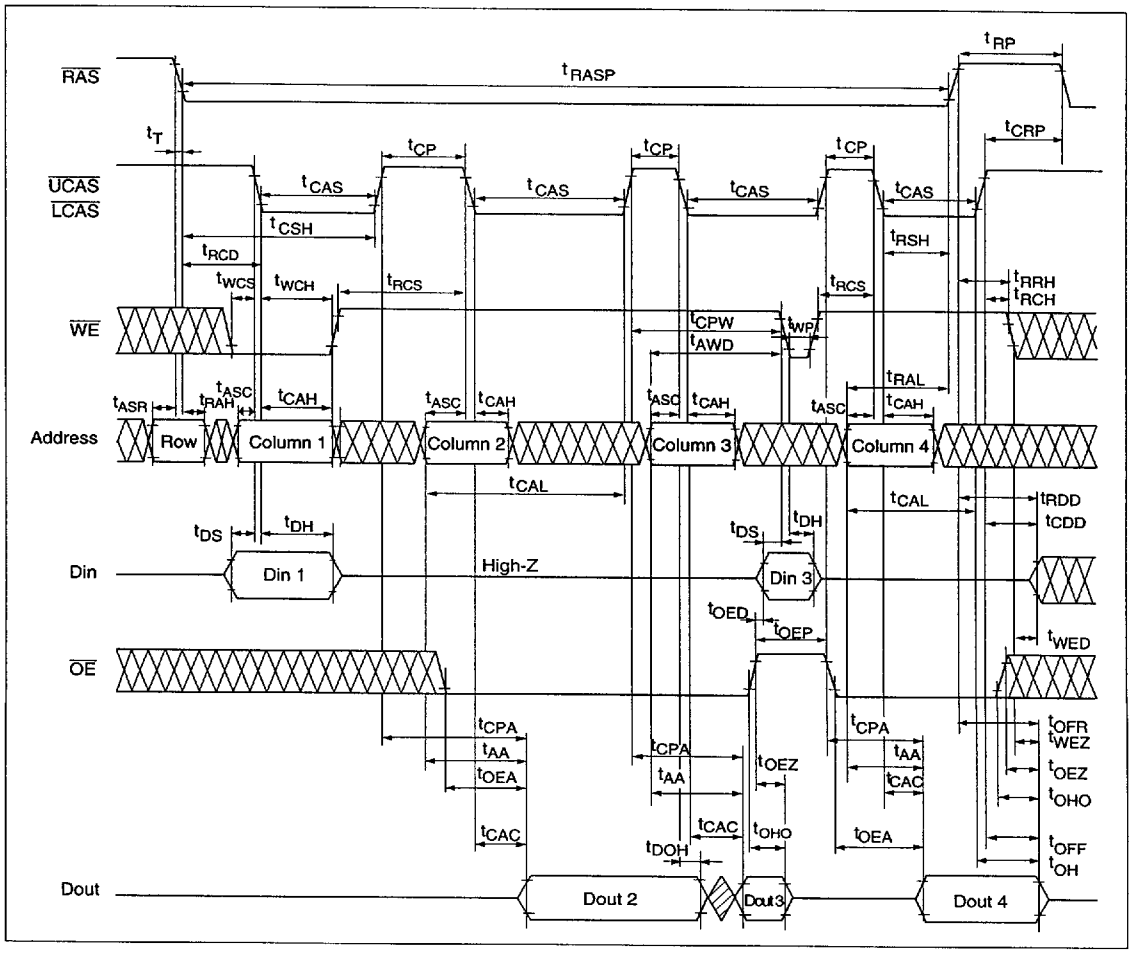
**EDO Page Mode Mix Cycle (1)**





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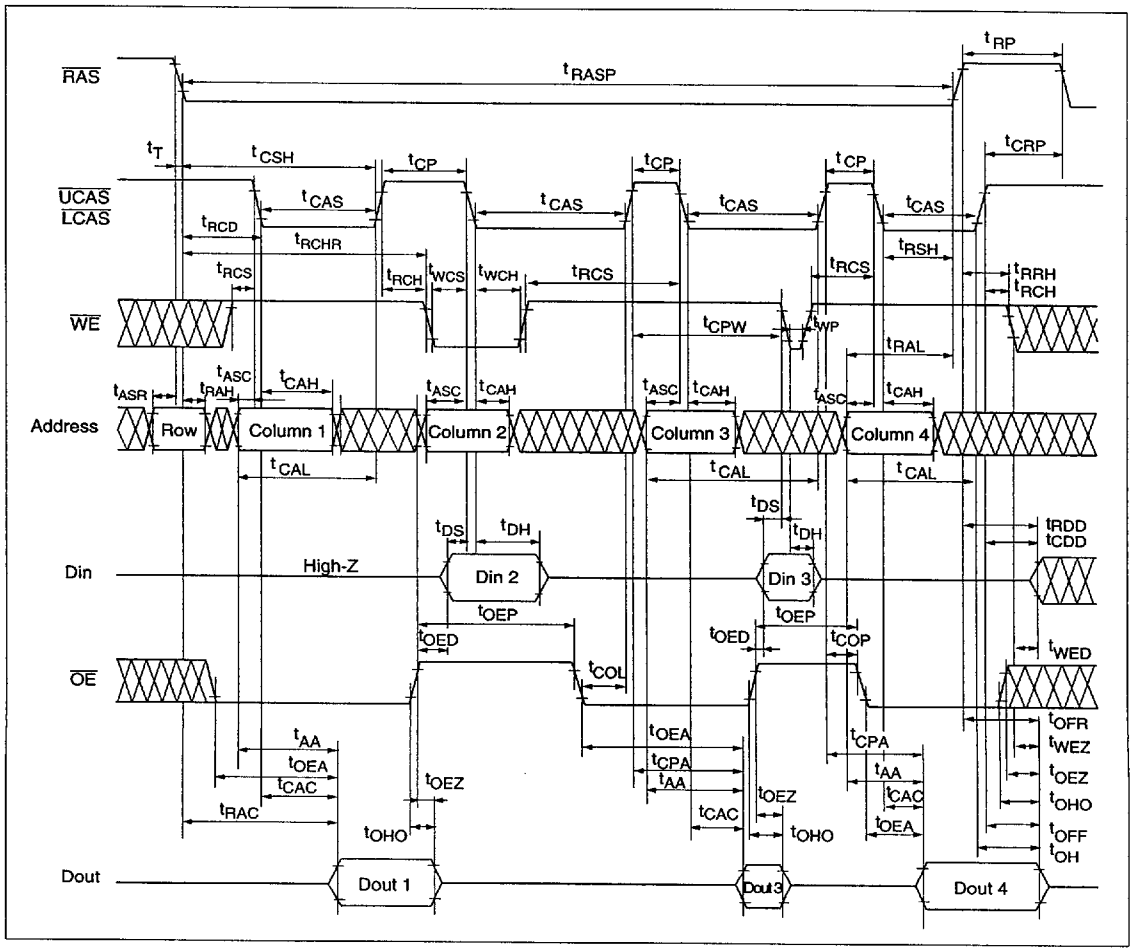
**EDO Page Mode Mix Cycle (2)**





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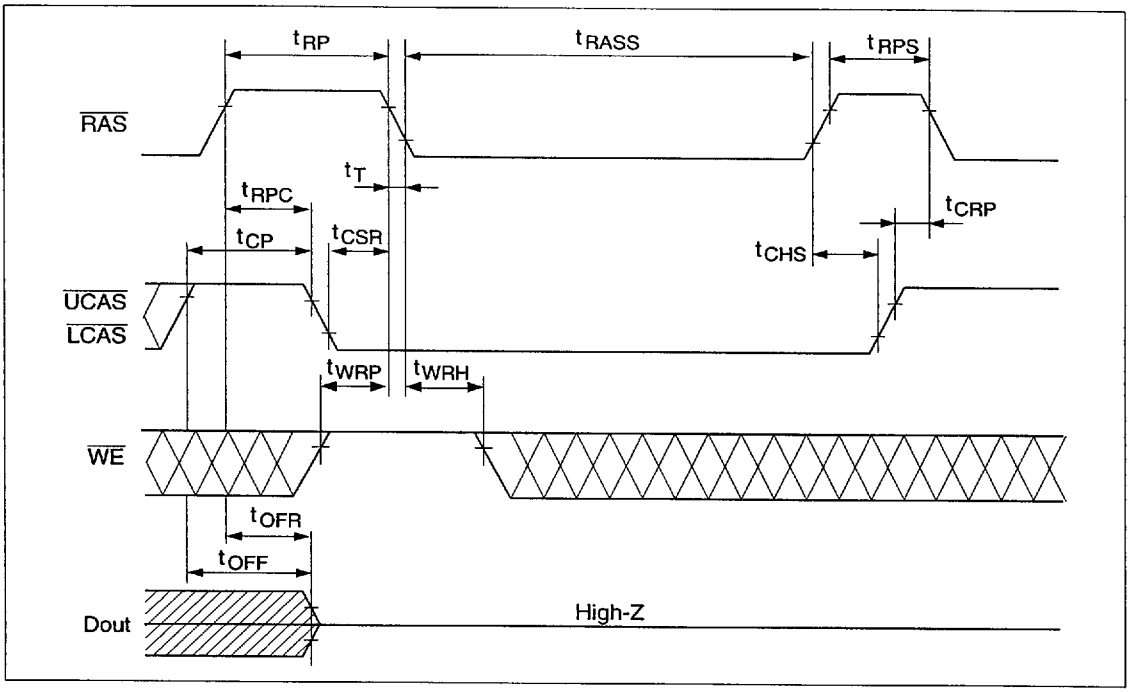
**Self Refresh Cycle** (L-version)*[28, 29, 30]





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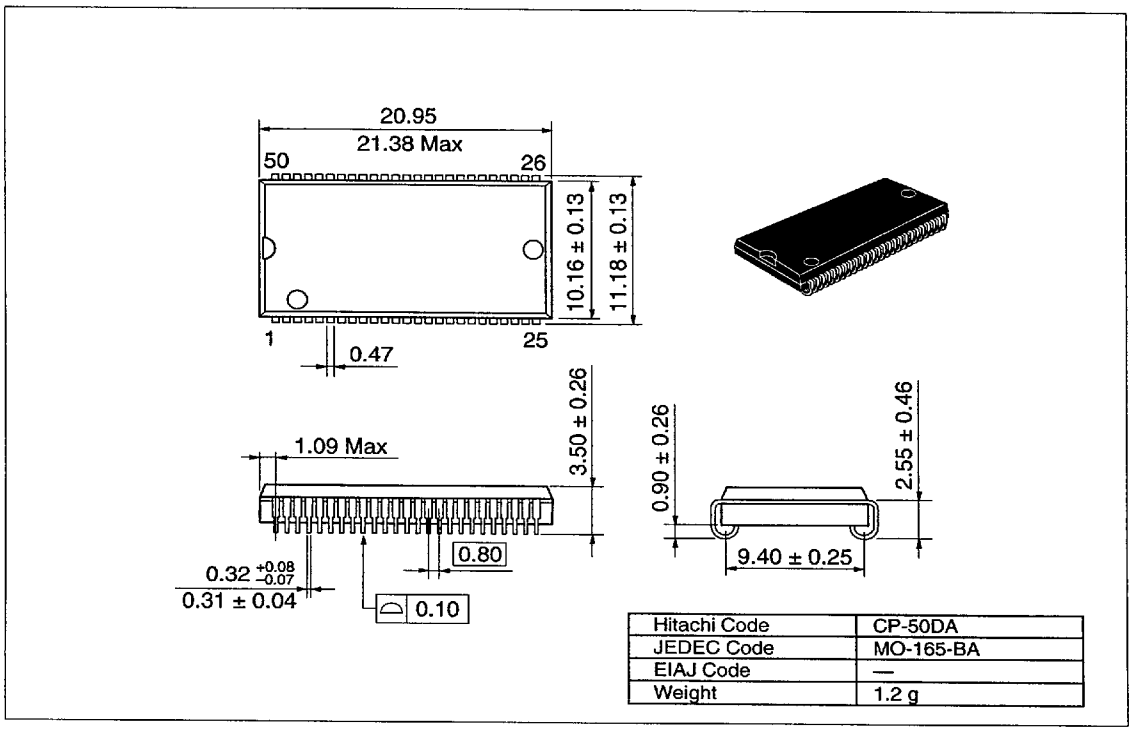
## Package Dimensions

**HM5164165AJ/ALJ Series**
**HM5165165AJ/ALJ Series** (CP-50DA)

Unit: mm




| | |
|---|---|
| Hitachi Code | CP-50DA |
| JEDEC Code | MO-165-BA |
| EIAJ Code | — |
| Weight | 1.2 g |





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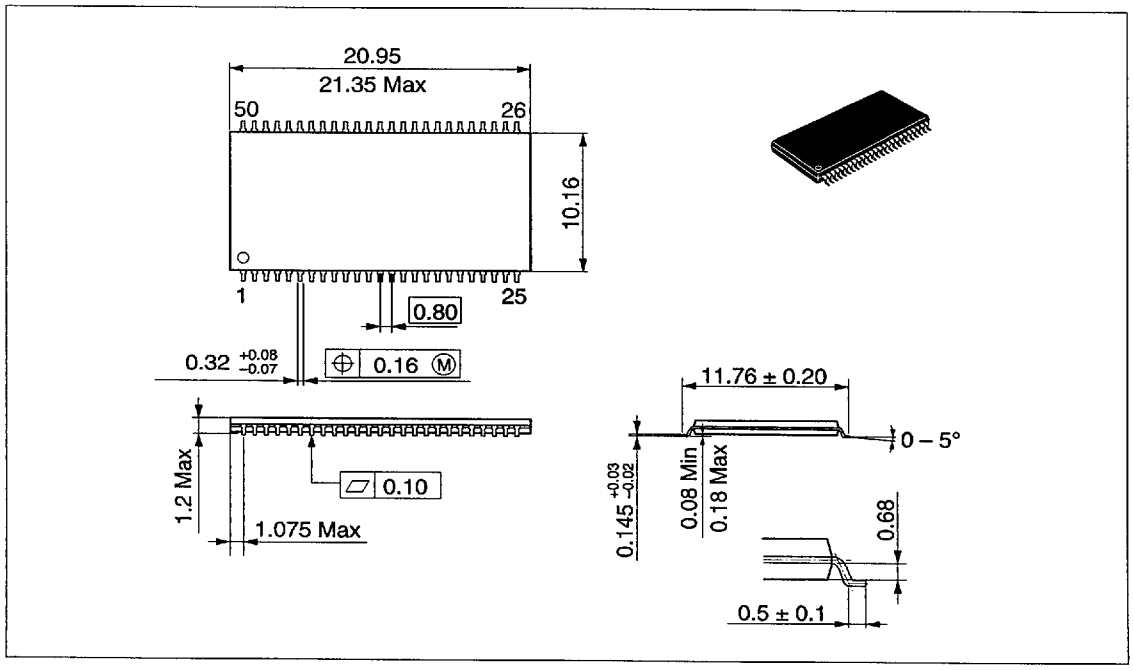
**HM5164165ATT/ALTT Series**
**HM5165165ATT/ALTT Series** (TTP-50DB)

Unit: mm



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