

HM514260A/AL-6R Series

HM51S4260A/AL-6R Series

Preliminary

262,144-word x 16-bit Dynamic Random Access Memory

HITACHI

Rev. 0.1
May. 31, 1994

The Hitachi HM514260A/AL are CMOS dynamic RAM organized as 262,144-word x 16-bit. HM514260A/AL have realized higher density, higher performance and various functions by employing 0.8 μm CMOS process technology and some new CMOS circuit design technologies. The HM514260A/AL offer fast page mode as a high speed access mode.

Multiplexed address input permits the HM514260A/AL to be packaged in standard 400-mil 40-pin plastic SOJ, standard 475-mil 40-pin plastic ZIP and standard 400-mil 40-pin plastic TSOPII.

Internal refresh timer enables HM51S4260A/AL self refresh operation.

Ordering Information

Type No.	Access time	Package
HM514260AJ/ALJ-6R	60 ns	400-mil 40-pin plastic SOJ
HM51S4260AJ/ALJ-6R	60 ns	(CP-40DA)
HM514260AZ/ALZ-6R	60 ns	475-mil 40-pin plastic ZIP
HM51S4260AZ/ALZ-6R	60 ns	(ZP-40)
HM514260ATT/ALTT-6R	60 ns	400-mil 40-pin plastic TSOPII
HM51S4260ATT/ALTT-6R	60 ns	(TTP-40DB)

Features

- Single 5 V ($\pm 5\%$)
- High speed
 - Access time: 60 ns (max)
- Low power dissipation
 - Active mode: 788 mW (max)
 - Standby mode: 11 mW (max)
1.1 mW (max) (L-version)
- Fast page mode capability
- 512 refresh cycles: 8 ms
128 ms (L-version)
- 2 $\overline{\text{CAS}}$ byte control
- 2 variations of refresh
 - $\overline{\text{RAS}}$ -only refresh
 - $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh
- Battery back up operation (L-version)
- Self-refresh operation (HM51S4260A/AL-6R)

Preliminary : This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

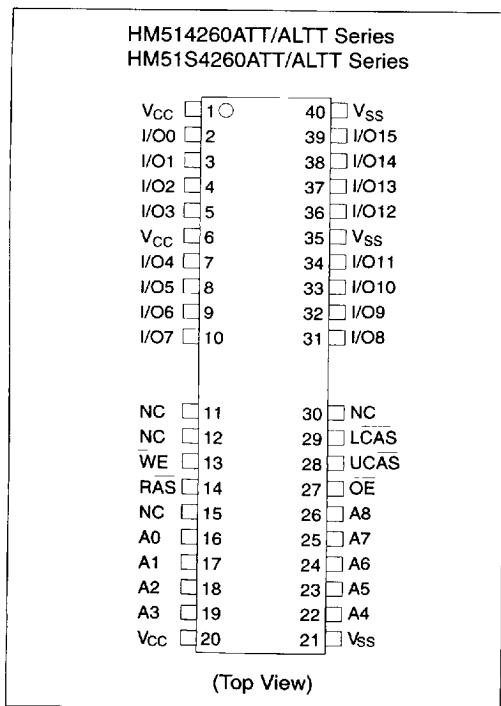
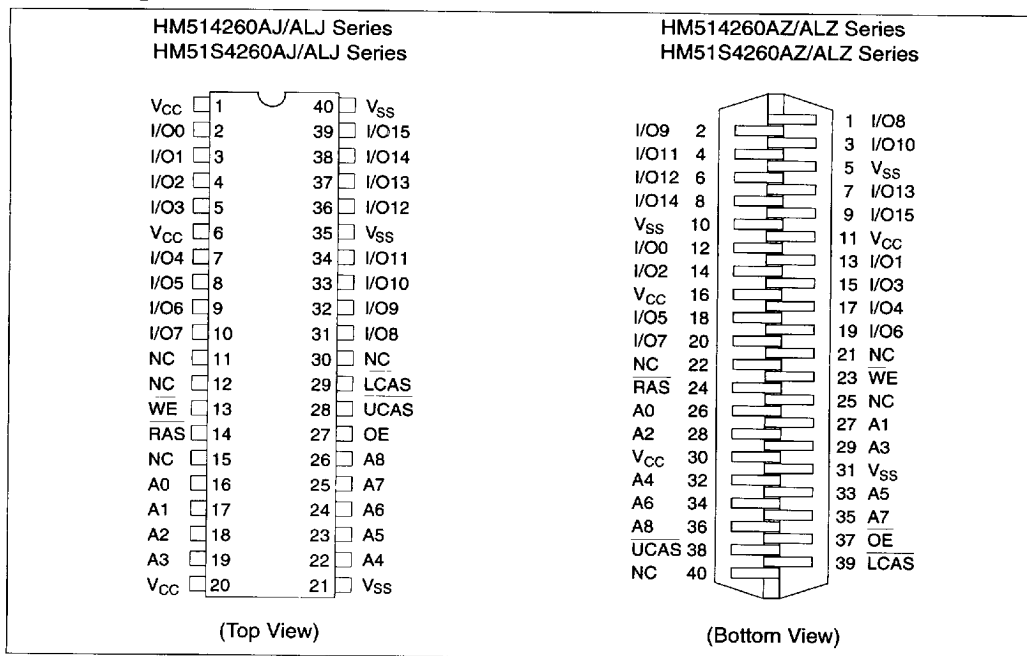
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Pin Arrangement



Pin Description

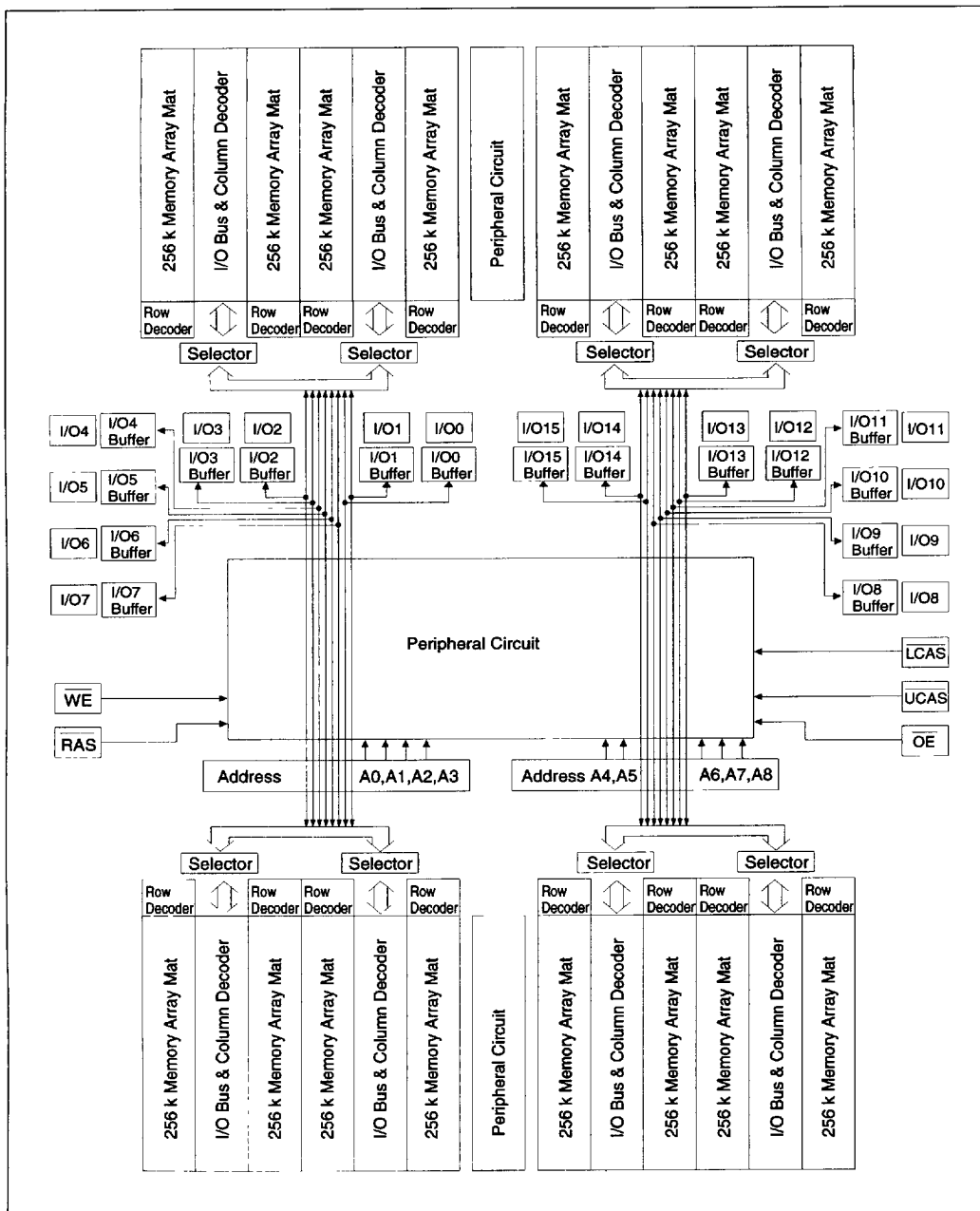
Pin name	Function
A0 – A8	Address input – Row address A0 – A8 – Column address A0 – A8 – Refresh address A0 – A8
I/O0 – I/O15	Data-in/data-out
$\overline{\text{RAS}}$	Row address strobe
$\overline{\text{UCAS}}, \overline{\text{LCAS}}$	Column address strobe
$\overline{\text{WE}}$	Read/write enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power (+5 V)
V _{SS}	Ground

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Block Diagram



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Operation Mode

The HM514260A series has the following 11 operation modes.

- | | |
|---------------------------------|---|
| 1. Read cycle | 7. Self refresh cycle(HM51S4260A) |
| 2. Early write cycle | 8. Fast page mode read cycle |
| 3. Delayed write cycle | 9. Fast page mode early write cycle |
| 4. Read-modify-write cycle | 10. Fast page mode delayed write cycle |
| 5. RAS-only refresh cycle | 11. Fast page mode read- modify-write cycle |
| 6. CAS-before-RAS refresh cycle | |

Inputs

RAS	LCAS	UCAS	WE	OE	Output	Operation
H	H	H	D	D	Open	Standby
H	L	L	H	L	Valid	Standby
L	L	L	H	L	Valid	Read cycle
L	L	L	L*2	D	Open	Early write cycle
L	L	L	L*2	H	Undefined	Delayed write cycle
L	L	L	H to L	L to H	Valid	Read-modify-write cycle
L	H	H	D	D	Open	RAS-only refresh cycle
H to L	H	L	D	D	Open	CAS-before-RAS refresh cycle Self refresh cycle(HM51S4260A)
	L	H				
	L	L				
L	H to L	H to L	H	L	Valid	Fast page mode read cycle
L	H to L	H to L	L*2	D	Open	Fast page mode early write cycle
L	H to L	H to L	L*2	H	Undefined	Fast page mode delayed write cycle
L	H to L	H to L	H to L	L to H	Valid	Fast page mode read-modify-write cycle
L	L	L	H	H	Open	Read cycle (Output disabled)

- Notes:
1. H: High(inactive) L: Low(active) D: Don't care
 2. $t_{WCS} \geq 0$ ns Early write cycle
 $t_{WCS} < 0$ ns Delayed write cycle
 3. Mode is determined by the OR function of the \overline{UCAS} and \overline{LCAS} . (Mode is set by the earliest of \overline{UCAS} and \overline{LCAS} active edge and reset by the latest of \overline{UCAS} and \overline{LCAS} inactive edge.)
 However write OPERATION and output HIZ control are done independently by each \overline{UCAS} , \overline{LCAS} .
 ex. if $\overline{RAS} = H$ to L, $\overline{LCAS} = L$, $\overline{UCAS} = H$, then CAS-before-RAS refresh cycle is selected.

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

Recommended DC Operating Conditions ($T_a = 0$ to +70°C) *2

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{SS}	0	0	0	V	2
	V_{CC}	4.75	5.0	5.25	V	1, 2
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	(I/O pin) V_{IL}	-1.0	—	0.8	V	1
	(Others) V_{IL}	-2.0	—	0.8	V	1

- Notes: 1. All voltage referred to V_{SS}
2. The supply voltage with all V_{CC} pins must be on the same level.
The supply voltage with all V_{SS} pins must be on the same level.

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DC Characteristics (Ta = 0 to 70°C, V_{CC} = 5 V ± 5%, V_{SS} = 0 V)

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Testconditions	Notes
		Min	Max			
Operating current	I _{CC1}	—	150	mA	$\overline{\text{RAS}}$ cycling LCAS or UCAS cycling t _{RC} = min	1, 2
Standby current	I _{CC2}	—	2	mA	TTL interface RAS, LCAS, UCAS = V _{IH} Dout = High-Z	
		—	1	mA	CMOS interface RAS, LCAS, UCAS, $\overline{\text{WE}}$ OE ≥ V _{CC} - 0.2 V Dout = High-Z	
Standby current (L-version)		—	200	μA	CMOS interface RAS, LCAS, OE, $\overline{\text{WE}}$ UCAS ≥ V _{CC} - 0.2 V Dout = High-Z	
RAS-only refresh current	I _{CC3}	—	140	mA	t _{RC} = min	2
Standby current	I _{CC5}	—	5	mA	$\overline{\text{RAS}} = V_{IH}$ LCAS or UCAS = V _{IL} Dout = enable	1
CAS-before-RAS refresh current	I _{CC6}	—	140	mA	t _{RC} = min	4
Fast page mode current	I _{CC7}	—	150	mA	t _{PC} = min	1, 3
Battery back up current (Standby with CBR refresh) (L-version)	I _{CC10}	—	300	μA	Standby: CMOS interface Dout = High-Z CBR refresh: t _{RC} = 250 μs t _{RAS} ≤ 1 μs, LCAS, UCAS = V _{IL} WE, OE = V _{IH}	4
Self-refresh mode current (HM51S4260A)	I _{CC11}	—	1	mA	CMOS interface RAS, LCAS, UCAS ≤ 0.2 V, Dout = High-Z	
Self-refresh mode current (HM51S4260AL)		—	200	μA	CMOS interface RAS, LCAS, UCAS ≤ 0.2 V, Dout = High-Z	
Input leakage current	I _{LI}	-10	10	μA	0 V ≤ Vin ≤ 6.5 V	

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DC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) (cont)

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Testconditions	Notes
		Min	Max			
Output leakage current	I_{LO}	-10	10	μA	$0\text{ V} \leq V_{out} \leq 6.5\text{ V}$ Dout = disable	
Output high voltage	V_{OH}	2.4	V_{CC}	V	High Iout = -5.0 mA	
Output low voltage	V_{OL}	0	0.4	V	Low Iout = 4.2 mA	

- Notes:
1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
 2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 3. Address can be changed once or less while \overline{LCAS} and $\overline{UCAS} = V_{IH}$.
 4. $V_{IH} \geq V_{CC} - 0.2\text{ V}$, $0 \leq V_{IL} \leq 0.2\text{ V}$, Address can be changed once or less while $\overline{RAS} = V_{IL}$.
 5. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

Capacitance ($T_a = 25^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 5\%$)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	10	pF	1, 2

- Notes:
1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. \overline{LCAS} and $\overline{UCAS} = V_{IH}$ to disable Dout

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AC Characteristics ($T_a = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 5\%$, $V_{SS} = 0\text{ V}$) *1, *14, *15, *17, *18

Test Conditions

- Input rise and fall times: 5 ns
- Input timing reference levels: 0.8 V, 2.4 V
- Output load: 2 TTL gate + C_L (50 pF)
(Including scope and jig)

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Notes
		Min	Max		
Random read or write cycle time	t_{RC}	110	—	ns	
$\overline{\text{RAS}}$ precharge time	t_{RP}	40	—	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	60	10000	ns	
$\overline{\text{CAS}}$ pulse width	t_{CAS}	15	10000	ns	23
Row address setup time	t_{ASR}	0	—	ns	
Row address hold time	t_{RAH}	10	—	ns	
Column address setup time	t_{ASC}	0	—	ns	19
Column address hold time	t_{CAH}	15	—	ns	19
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ delay time	t_{RCD}	20	45	ns	8
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	15	30	ns	9
$\overline{\text{RAS}}$ hold time	t_{RSH}	15	—	ns	
$\overline{\text{CAS}}$ hold time	t_{CSH}	60	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	15	—	ns	20, 24
$\overline{\text{OE}}$ to Din delay time	t_{ODD}	15	—	ns	
$\overline{\text{OE}}$ delay time from Din	t_{DZO}	0	—	ns	
$\overline{\text{CAS}}$ setup time from Din	t_{DZC}	0	—	ns	
Transition time (rise and fall)	t_T	3	50	ns	7
Refresh period	t_{REF}	—	8	ms	
Refresh period (L-version)	t_{REF}	—	128	ms	

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Read Cycle

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Notes
		Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	—	60	ns	2, 3
Access time from $\overline{\text{CAS}}$	t_{CAC}	—	15	ns	3, 4, 13
Access time from address	t_{AA}	—	30	ns	3, 5, 13
Access time from $\overline{\text{OE}}$	t_{OAC}	—	15	ns	23
Read command setup time	t_{RCS}	0	—	ns	19
Read command hold time to $\overline{\text{CAS}}$	t_{RCH}	0	—	ns	16, 19
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	—	ns	16
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	ns	
Output buffer turn-off time	t_{OFF1}	0	15	ns	6
Output buffer turn-off to $\overline{\text{OE}}$	t_{OFF2}	0	15	ns	6
$\overline{\text{CAS}}$ to Din delay time	t_{CDD}	15	—	ns	
$\overline{\text{OE}}$ pulse width	t_{OEP}	15	—	ns	23

Write Cycle

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Notes
		Min	Max		
Write command setup time	t_{WCS}	0	—	ns	10, 19
Write command hold time	t_{WCH}	15	—	ns	19
Write command pulse width	t_{WCP}	10	—	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	15	—	ns	
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	15	—	ns	21
Data-in setup time	t_{DS}	0	—	ns	11
Data-in hold time	t_{DH}	15	—	ns	11
$\overline{\text{CAS}}$ to $\overline{\text{OE}}$ delay time	t_{COD}	—	0	ns	23

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Read-Modify-Write Cycle

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Notes
		Min	Max		
Read-modify-write cycle time	t_{RWC}	150	—	ns	
\overline{RAS} to \overline{WE} delay time	t_{RWD}	80	—	ns	10
\overline{CAS} to \overline{WE} delay time	t_{CWD}	35	—	ns	10
Column address to \overline{WE} delay time	t_{AWD}	50	—	ns	10, 13
\overline{OE} hold time from \overline{WE}	t_{OEH}	15	—	ns	

Refresh Cycle

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Notes
		Min	Max		
\overline{CAS} setup time (\overline{CAS} -before- \overline{RAS} refresh cycle)	t_{CSR}	10	—	ns	19
\overline{CAS} hold time (\overline{CAS} -before- \overline{RAS} refresh cycle)	t_{CHR}	10	—	ns	20
\overline{RAS} precharge to \overline{CAS} hold time	t_{RPC}	10	—	ns	19
\overline{CAS} precharge time in normal mode	t_{CPN}	10	—	ns	22

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Fast Page Mode Cycle

Parameter	Symbol	HM514260A/AL-6R HM51S4260A/AL-6R		Unit	Notes
		Min	Max		
Fast page mode cycle time	t_{PC}	40	—	ns	
Fast page mode \overline{CAS} precharge time	t_{CP}	10	—	ns	22
Fast page mode \overline{RAS} pulse width	t_{RASC}	—	100000	ns	12
Access time from \overline{CAS} precharge	t_{ACP}	—	35	ns	3, 13, 20
\overline{RAS} hold time from \overline{CAS} precharge	t_{RHCP}	35	—	ns	
Fast page mode read-modify-write cycle \overline{CAS} precharge to WE delay time	t_{CPW}	55	—	ns	
Fast page mode read-modify-write cycle time	t_{PCM}	80	—	ns	

Self-refresh Mode

Parameter	Symbol	HM51S4260A/AL-6R		Unit	Notes
		Min	Max		
\overline{RAS} pulse width (self-refresh)	t_{RASS}	100	—	μs	
\overline{RAS} precharge time (self-refresh)	t_{RPS}	110	—	ns	
\overline{CAS} hold time (self-refresh)	t_{CHS}	-50	—	ns	21

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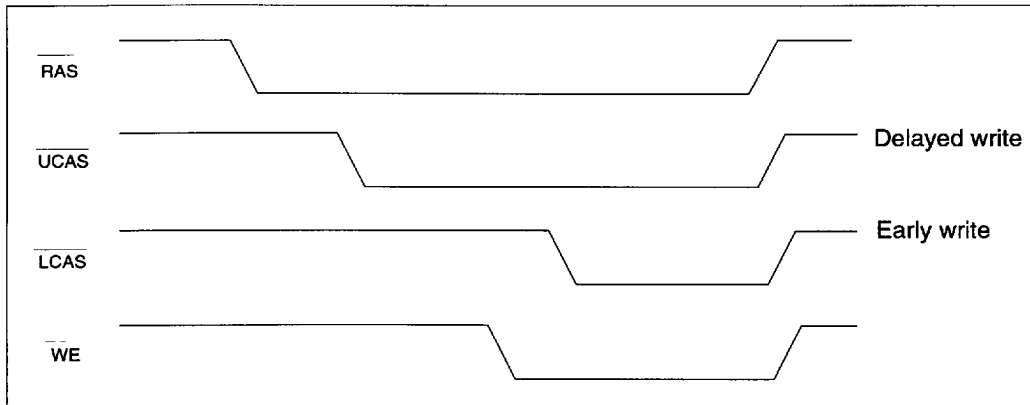
- Notes:
1. AC measurements assume $t_T = 5$ ns.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2 TTL loads and 50 pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referred to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWD} \geq t_{AWD}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referred to $\overline{\text{CAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ leading edge in a delayed write or a read-modify-write cycle.
 12. t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 13. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 14. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles is required.
 15. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
 16. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
 17. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be staggered within the same write/read cycles.
 18. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
 19. t_{ASC} , t_{CAH} , t_{RCS} , t_{RCH} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 20. t_{CRP} , t_{CHR} , t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
 21. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$.
 22. t_{CPN} and t_{CP} are determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
 23. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH}(\text{min})/V_{IL}(\text{max})$ level.
 24. t_{CRP} is planned to be improved to match the standard DRAM specifications.
 25. If you use distributed CBR refresh mode with 15.6 μs interval in normal read/write cycle, CBR refresh should be executed within 15.6 μs immediately after exiting from and before entering into self refresh mode.
 26. If you use $\overline{\text{RAS}}$ only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with 15.6 μs interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
 27. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

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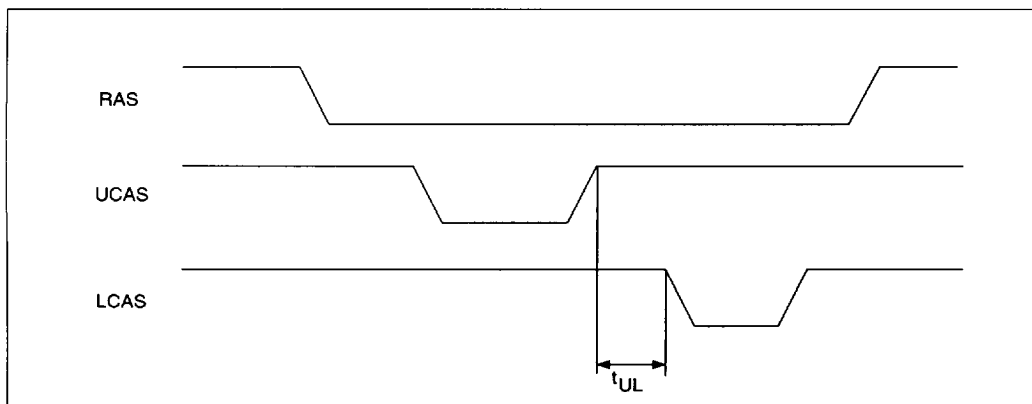
Notes concerning $\overline{2CAS}$ control

Please do not separate the $\overline{UCAS/LCAS}$ operation timing intentionally. However skew between $\overline{UCAS/LCAS}$ are allowed under the following conditions.

- (1) Each of the $\overline{UCAS/LCAS}$ should satisfy the timing specifications individually.
- (2) Different operation mode for upper/lower byte is not allowed; such as following.

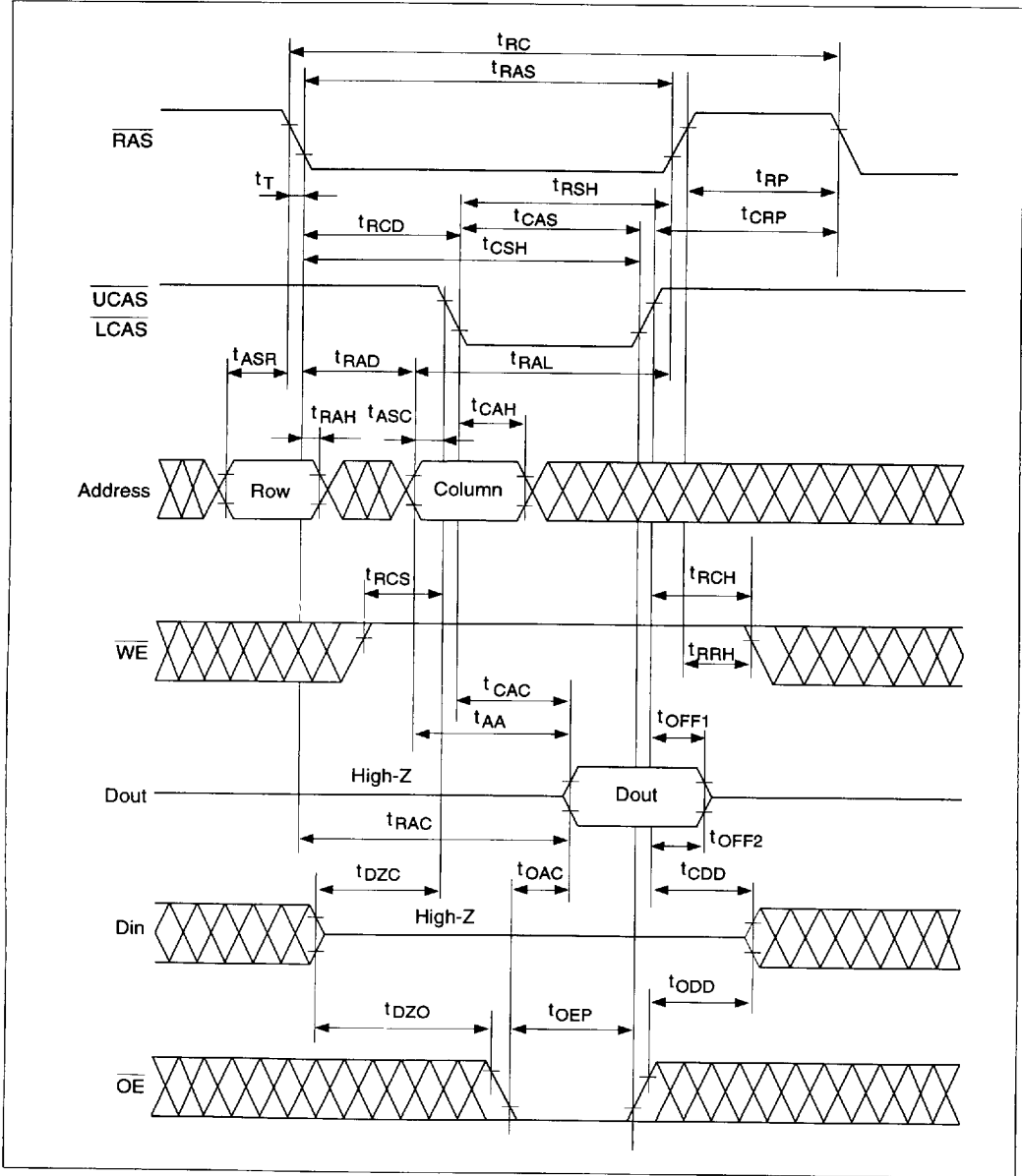




- (3) Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.



Timing Waveforms*28

Read Cycle



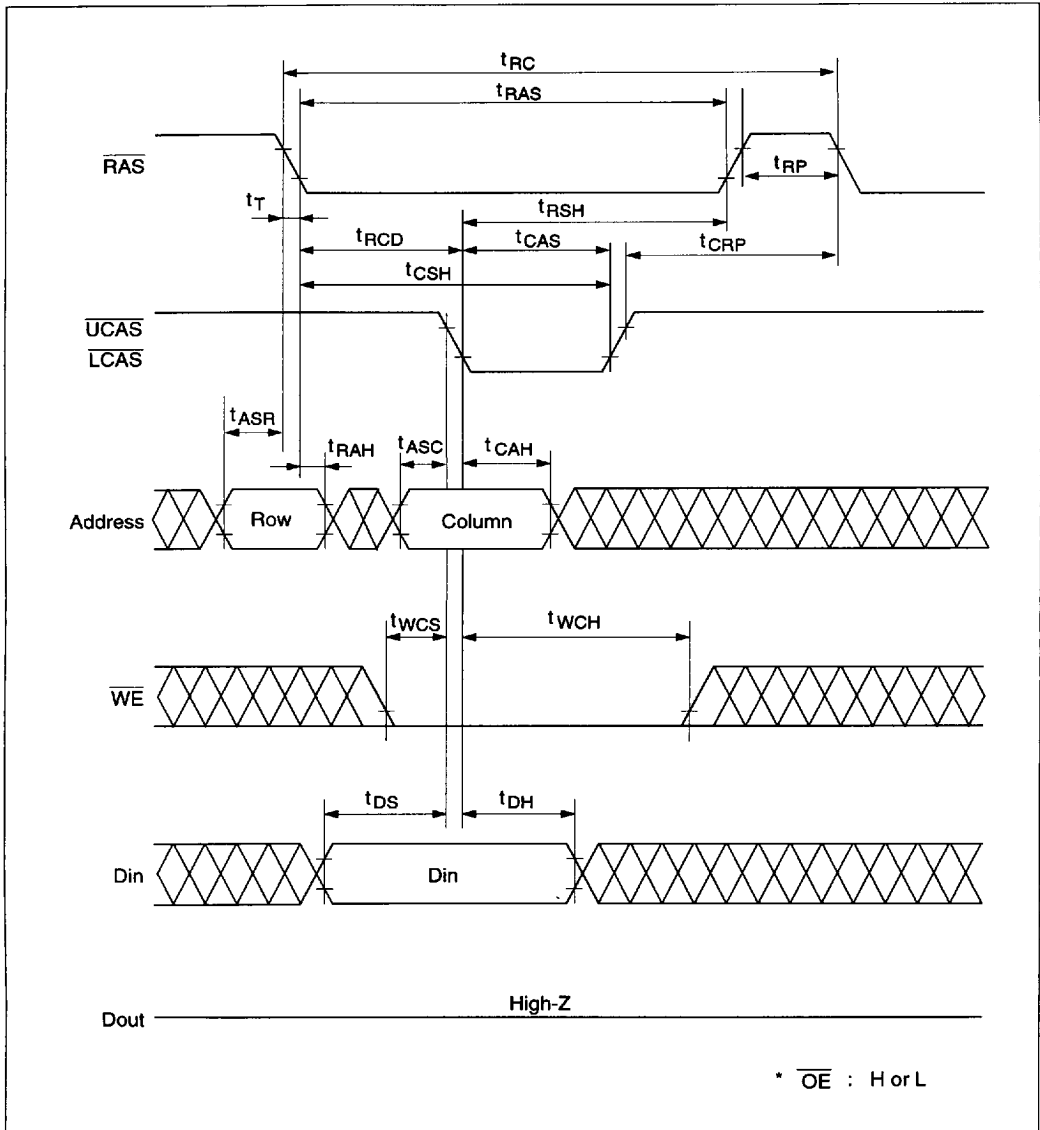
Note: 28  H or L (H: $V_{IH}(\min) \leq V_{IN} \leq V_{IH}(\max)$, L: $V_{IL}(\min) \leq V_{IN} \leq V_{IL}(\max)$)
 Invalid Dout

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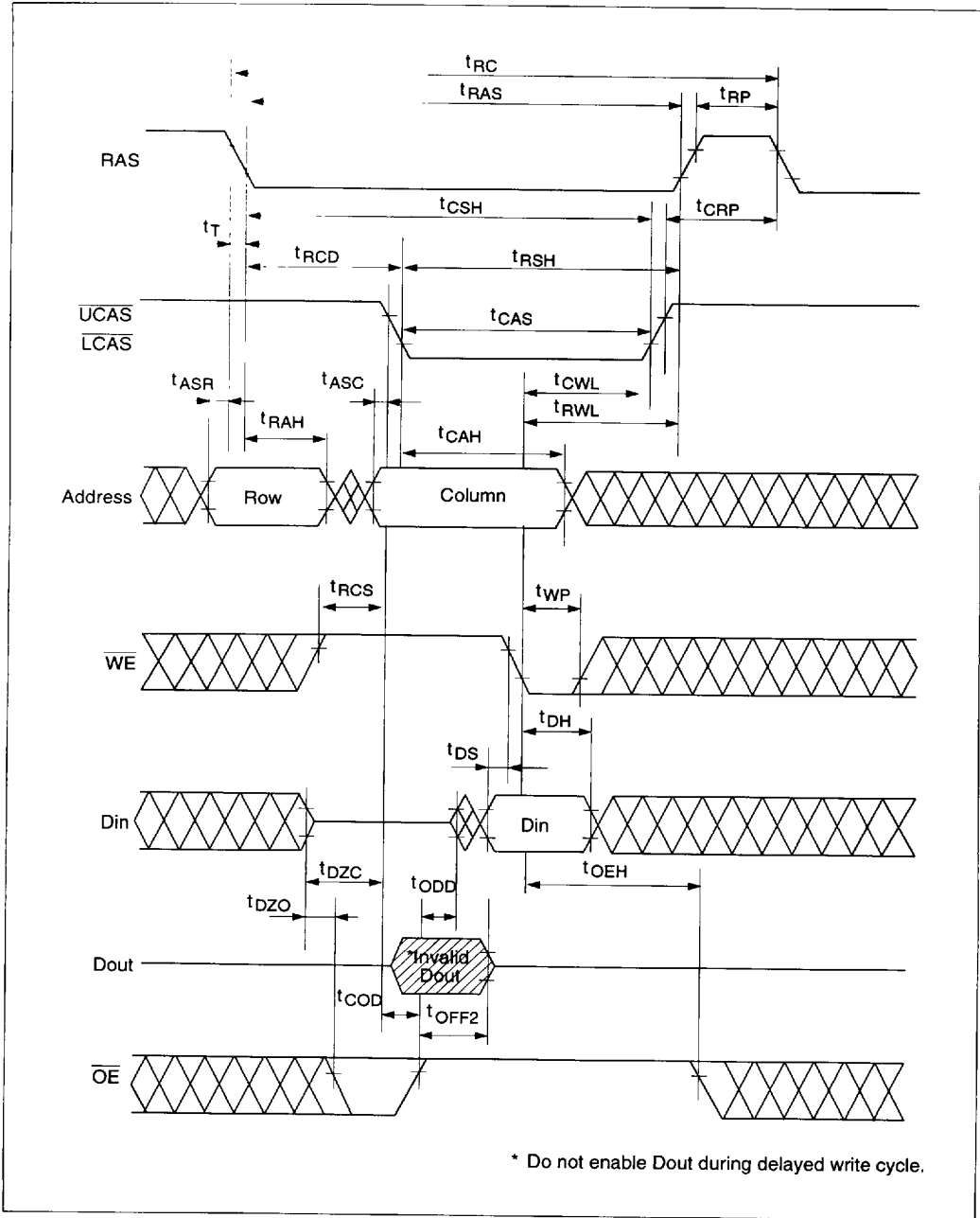
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Early Write Cycle

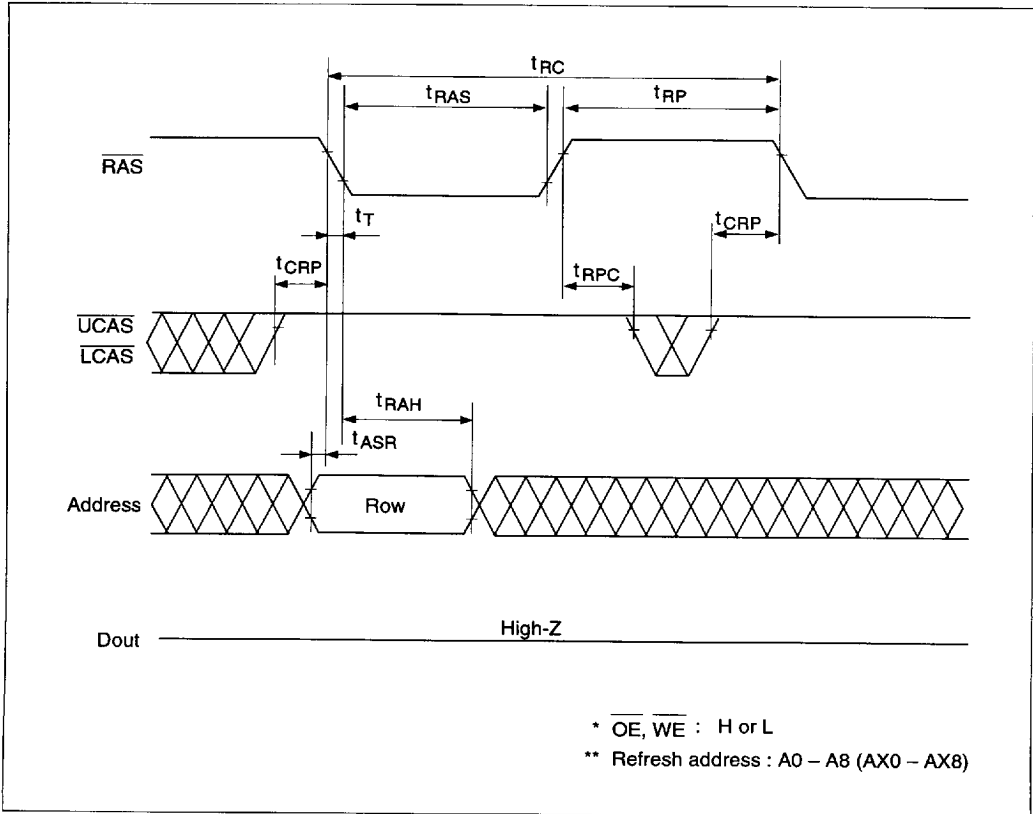


Delayed Write Cycle



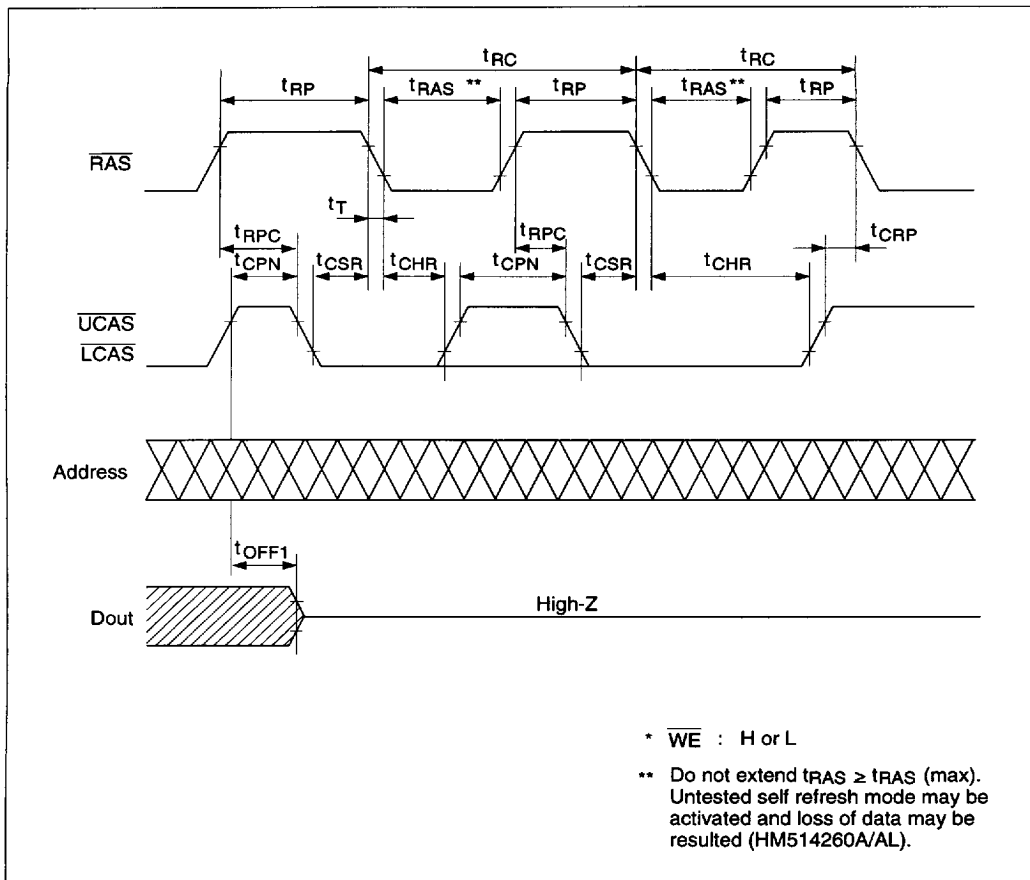
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RAS-Only Refresh Cycle

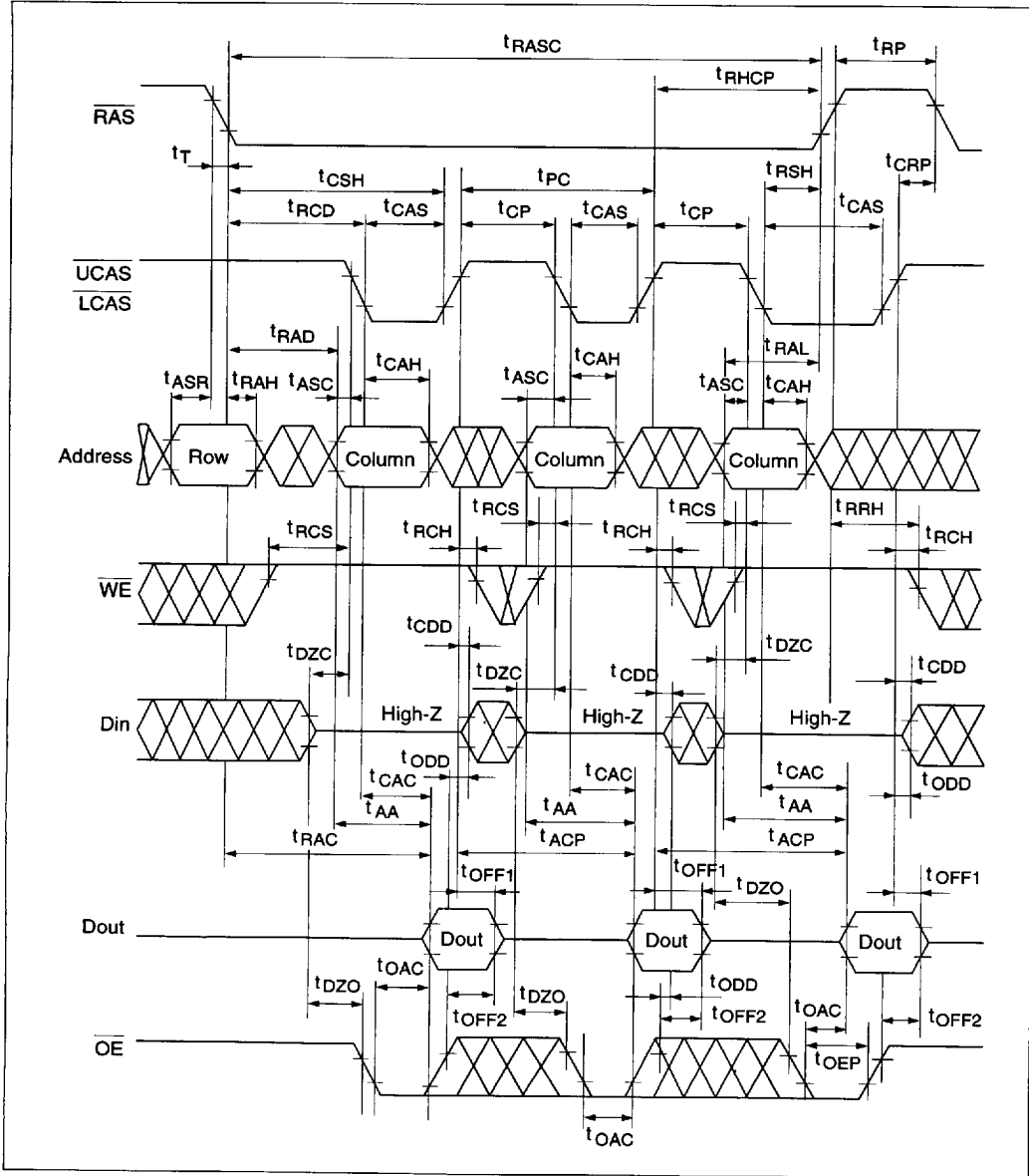


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$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh Cycle

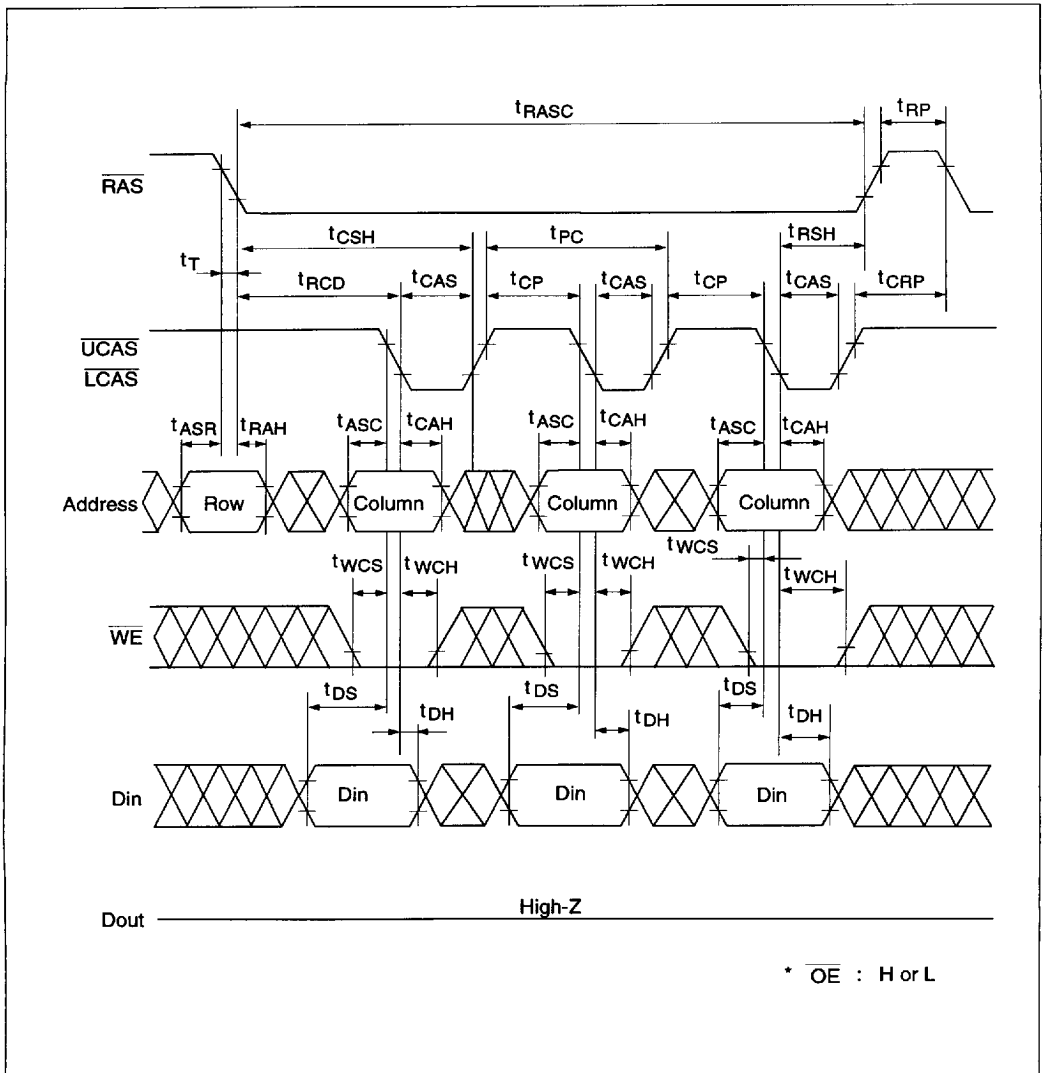


Fast Page Mode Read Cycle

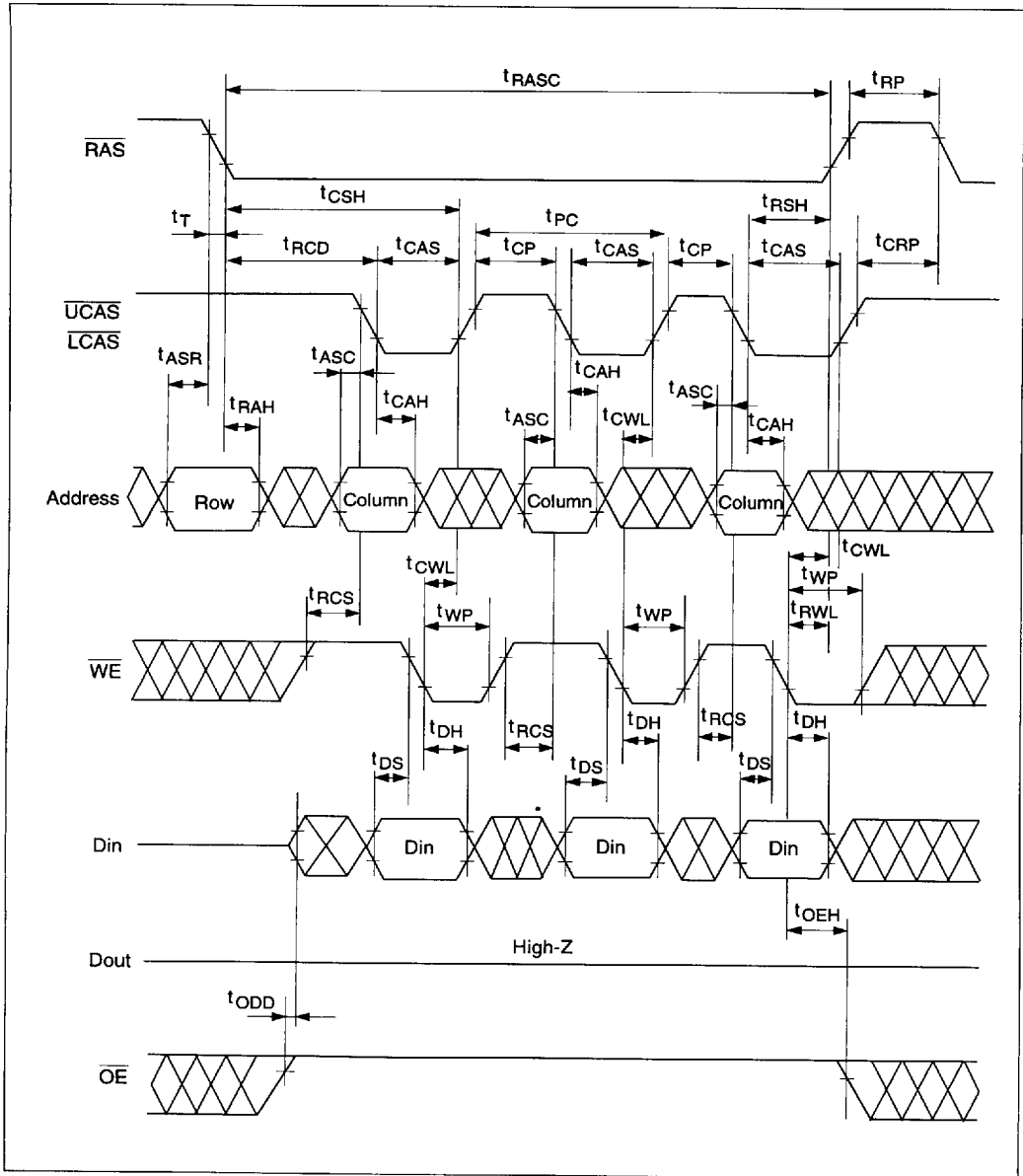


HM514260A/AL-6R, HM51S4260A/AL-6R Series

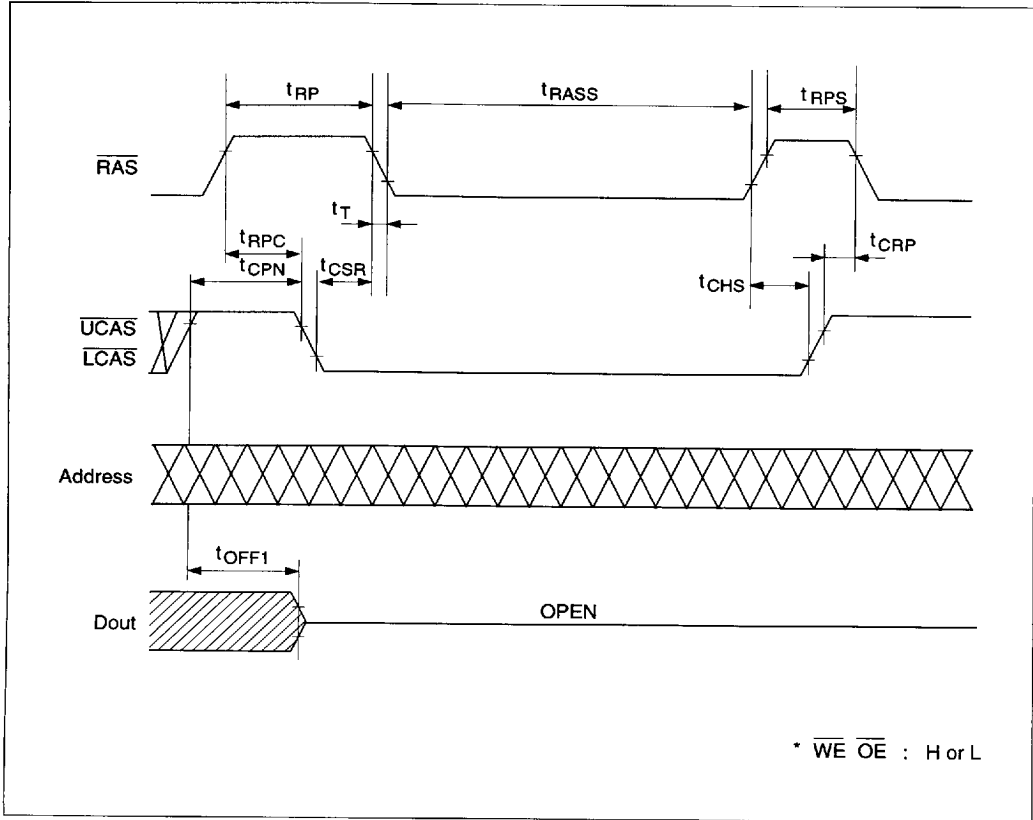
Fast Page Mode Early Write Cycle



Fast Page Mode Delayed Write Cycle



Self Refresh Cycle



The low self refresh current is achieved by introducing extremely long internal refresh cycle. Therefore some care needs to be taken on the refresh.

1. Please do not use t_{RASS} timing, $10 \mu s \leq t_{RASS} \leq 100 \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100 \mu s$, then RAS precharge time should use t_{RPS} instead of t_{RP} .
2. If you use \overline{RAS} only refresh or CBR burst refresh mode in normal read/write cycle, 512 cycles of distributed CBR refresh with $15.6 \mu s$ interval should be executed within 8 ms immediately after exiting from and before entering into the self refresh mode.
3. If you use distributed CBR refresh mode with $15.6 \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6 \mu s$ immediately after exiting from and before entering into self refresh mode.
4. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.