MHS

MATRA M H S

September 1990

T-46-23-05

DATA SHEET

HM 65262

16 k x 1
VERY LOW POWER CMOS SRAM

FEATURES

- ACCESS TIME
  MILITARY/INDUSTRIAL : 70/85 ns (max)
  COMMERCIAL : 55/70 ns (max)
- VERY LOW POWER CONSUMPTION
  ACTIVE : 110 mW (typ)
  STANDBY : 2.0 µW (typ)
  DATA RETENTION : 0.8 µW (typ)
- WIDE TEMPERATURE RANGE : – 55 TO + 125°C
- 300 MILS WIDTH PACKAGE
- TTL COMPATIBLE INPUTS AND OUTPUTS
- ASYNCHRONOUS
- SINGLE 5 VOLT SUPPLY
- EQUAL CYCLE AND ACCESS TIME
- GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED

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DESCRIPTION

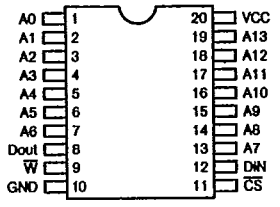
The HM 65262 is a very low power CMOS static RAM organized as 16384 x 1 bit. It is manufactured using the MHS high performance CMOS technology.
The HM 65262 is a "Pure CMOS SRAM" utilising an array of six transistor (6T) memory cells permitting the lowest possible standby supply current (typical value = 0.1 µA) over the full temperature range. The high stability of the 6T cell provides excellent protection against soft errors due to noise.

Easy memory expansion is provided by an active low chip select ($\overline{CS}$), an active low output enable ($\overline{OE}$) and three state drivers.
All inputs and outputs of the HM 65262 are TTL compatible and operate from single 5 V supply thus simplifying system design.
The HM 65262 is processed following the test methods of MIL STD 883C.

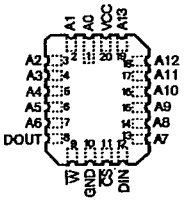
PACKAGES

Plastic 300 mils, 20 pins, DIL.
Ceramic 300 mils, 20 pins, DIL.
LCC, 20 pins.

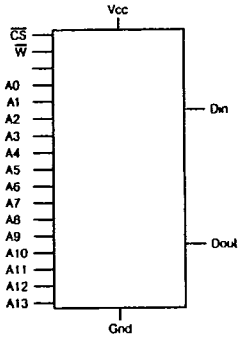
Pinout DIL 20 pins (top view)



Pinout LCC 20 pins (top view)



LOGIC SYMBOL



BLOCK DIAGRAM

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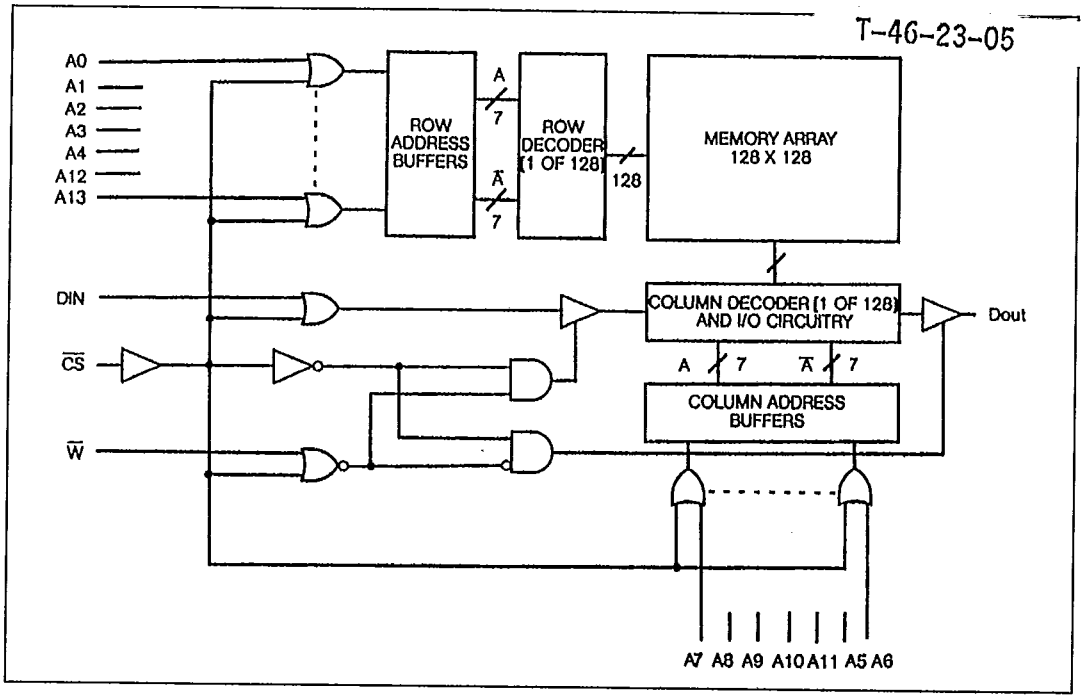

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PIN NAMES

A0-A13	: Address inputs	$\overline{W}$	: Write enable
Din	: Input	VCC	: Power
Dout	: Output	GND	: Ground
$\overline{CS}$	: Chip Select		

TRUTH TABLE

$\overline{CS}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	Z	Z	Deselect
L	H	Z	Valid	Read
L	L	Valid	Z	Write

L = low, H = high, X = H or L, Z = high impedance.

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : – 0.3 V to + 7.0 V
Input or Output voltage applied : (Gnd – 0.3 V) to (Vcc + 0.3 V)
Storage temperature : – 65°C to + 150°C

OPERATING RANGE

		OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	(– 2)	Vcc ± 10 %	– 55°C to + 125°C
Industrial	(– 9)	Vcc ± 10 %	– 40°C to + 85°C
Commercial	(– 5)	Vcc ± 10 %	– 0°C to + 70°C

RECOMMENDED DC OPERATING CONDITIONS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc	Supply voltage	4.5	5.0	5.5	V
Gnd	Ground	0.0	0.0	0.0	V
VIL (1)	Input low voltage	– 0.3	0.0	0.8	V
VIH	Input high voltage	2.2	–	Vcc + 0.3 V	V

Note : 1. VIL min = – 0.3 V or - 1.0 V pulse width 50 ns.

CAPACITANCE

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin (2)	Input capacitance	–	–	8	pF
Cout (2)	Output capacitance	–	–	8	pF

Note : 2. TA = 25°C, f = 1 MHz, Vcc = 5.0 V, these parameters are not 100 % tested.

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ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(3)	Input leakage current	– 1.0	–	1.0	µA
IOZ	(3)	Output leakage current	– 1.0	–	1.0	µA
VOL	(4)	Output low voltage	–	–	0.4	V
VOH	(4)	Output high voltage	2.4	–	–	V

Notes : 3. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
4. Vcc min, IOL = 8.0 mA, IOH = – 4.0 mA.

Consumption for Commercial specification (– 5) :

SYMBOL		PARAMETER	65262 B-5	65262 -5	65262 C-5	UNIT	VALUE
ICCSB	(5)	Standby supply current	2.0	2.0	2.0	mA	max
ICCSB1	(6)	Standby supply current	1.0	1.0	100.0	µA	max
ICC	(7)	Operating supply current	50.0	50.0	50.0	mA	max
ICCOP	(8)	Operating supply current	50.0	50.0	50.0	mA	max

Consumption for Industrial specification (– 9) :

SYMBOL		PARAMETER	65262 B-9	65262 -9	65262 C-9	UNIT	VALUE
ICCSB	(5)	Standby supply current	3.0	3.0	3.0	mA	max
ICCSB1	(6)	Standby supply current	5.0	5.0	100.0	µA	max
ICC	(7)	Operating supply current	50.0	50.0	50.0	mA	max
ICCOP	(8)	Operating supply current	50.0	50.0	50.0	mA	max

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Consumption for Military specification (– 2) :

SYMBOL		PARAMETER	65262 B-2	65262 -2	65262 C-2	UNIT	VALUE
ICCSB	(5)	Standby supply current	5.0	5.0	5.0	mA	max
ICCSB1	(6)	Standby supply current	50.0	50.0	500.0	µA	max
ICC	(7)	Operating supply current	50.0	50.0	50.0	mA	max
ICCOP	(8)	Operating supply current	50.0	50.0	50.0	mA	max

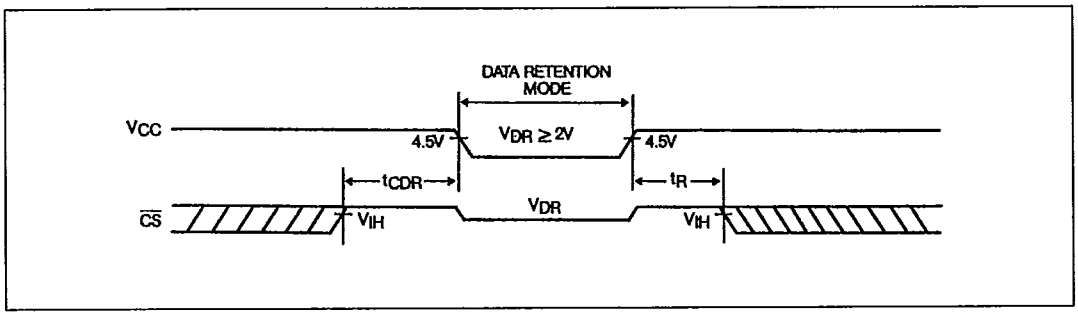
Notes : 5. $\overline{CS} \geq$ VIH.
6. $\overline{CS} \geq$ Vcc - 0.3V, Iout = 0 mA.
7. $\overline{CS} \leq$ VIL, Iout = 0 mA, Vin = Gnd/Vcc.
8. Vcc max, Iout = 0 mA, f = 1 MHz and 5 mA/MHz, Vin = Gnd/Vcc.

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc + 0.3 V.
2. $\overline{CS}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
3. The RAM can begin operation > 55 ns after Vcc reaches the minimum operating voltage (4.5 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (9)	MAXIMUM	UNIT
VCCDR	Vcc for data retention	2.0	–	–	V
TCDR	Chip deselect to data retention time	0.0	–	–	ns
TR	Operation recovery time	TAVAV (10)	–	–	ns
ICCDR1 (11)	Data retention current @ 2.0 V : HM-65262(B)-5	–	0.1	1.0	µA
	HM-65262(B)-9	–	0.1	2.0	µA
	HM-65262(B)-2	–	0.1	20.0	µA
	HM-65262C-5	–	0.1	30.0	µA
	HM-65262C-9	–	0.1	30.0	µA
	HM-65262C-2	–	0.1	200.0	µA
ICCDR2 (11)	Data retention current @ 3.0 V : HM-65262(B)-5	–	0.3	1.0	µA
	HM-65262(B)-9	–	0.3	3.0	µA
	HM-65262(B)-2	–	0.3	30.0	µA
	HM-65262C-5	–	0.3	50.0	µA
	HM-65262C-9	–	0.3	50.0	µA
	HM-65262C-2	–	0.3	300.0	µA

Notes : 9. TA = 25°C.
10. TAVAV = Read cycle time.
11. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc, this parameter is only tested to Vcc = 2 V.

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ELECTRICAL CHARACTERISTICS AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.5 V
Output load : 1 TTL gate + 100 pF

WRITE CYCLE : Commercial specification

SYMBOL	PARAMETER	65262 B-5	65262 -5	65262 C-5	UNIT	VALUE
TAVAV	Write cycle time	55	70	70	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	50	55	55	ns	min
TDVWH	Data set-up time	35	40	40	ns	min
TELWH	$\overline{CS}$ low to write end	50	55	55	ns	min
TWLQZ (12)	Write low to high Z	35	40	40	ns	max
TWLWH	Write pulse width	50	55	55	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

WRITE CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65262 B-9/2	65262 -9/2	65262 C-9/2	UNIT	VALUE
TAVAV	Write cycle time	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	ns	min
TAVWH	Address valid to end of write	55	65	65	ns	min
TDVWH	Data set-up time	40	45	45	ns	min
TELWH	$\overline{CS}$ low to write end	55	65	65	ns	min
TWLQZ (12)	Write low to high Z	50	50	50	ns	max
TWLWH	Write pulse width	55	65	65	ns	min
TWHAX	Address hold to end of write	0	0	0	ns	min
TWHDX	Data hold time	0	0	0	ns	min
TWHQX (12)	Write high to low Z	0	0	0	ns	min

Note : 12. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.

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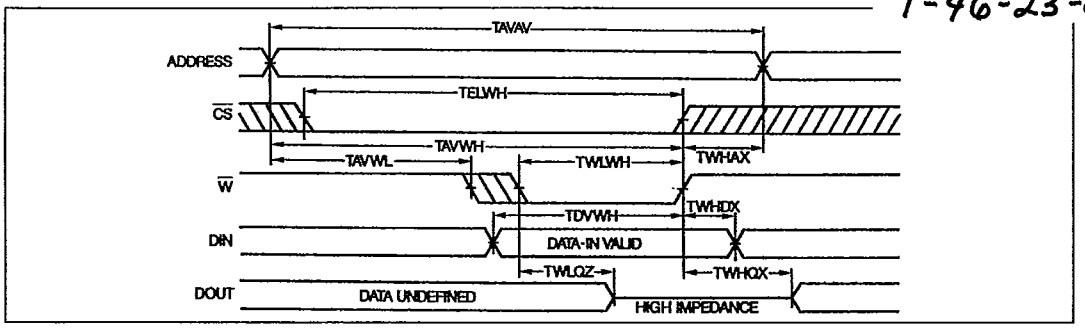
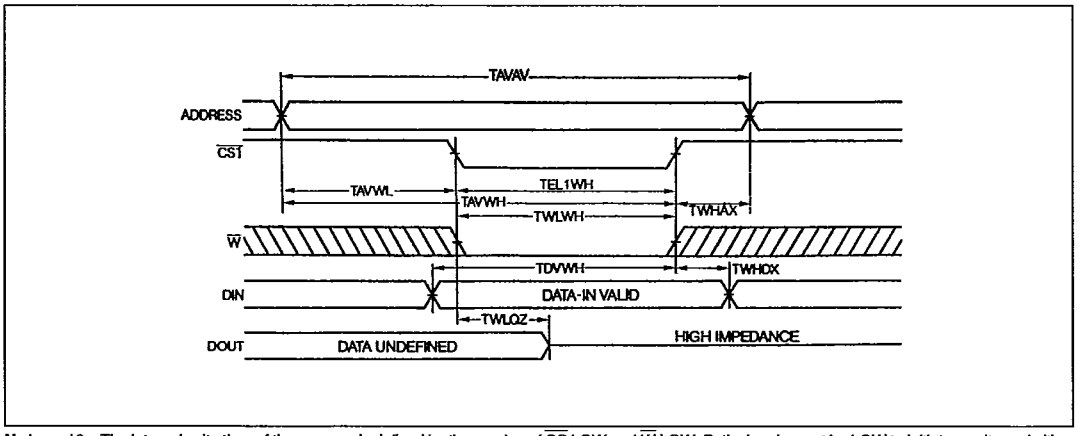
WRITE CYCLE 1 ($\overline{W}$ CONTROLLED) (note 13)



WRITE CYCLE 2 ($\overline{CS}$ CONTROLLED) (note 13)



Note : 13. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

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READ CYCLE : Commercial specification

SYMBOL	PARAMETER	65262 B-5	65262 -5	65262 C-5	UNIT	VALUE
TAVAV	READ cycle time	55	70	70	ns	min
TAVQV	Address access time	55	70	70	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	55	70	70	ns	max
TELQZ	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	40	40	40	ns	max

READ CYCLE : Industrial and Military specification

SYMBOL	PARAMETER	65262 B-9/2	65262 -9/2	65262 C-9/2	UNIT	VALUE
TAVAV	READ cycle time	70	85	85	ns	min
TAVQV	Address access time	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	ns	min
TELQV	Chip-select access time	70	85	85	ns	max
TELQX	$\overline{CS}$ low to low Z	5	5	5	ns	min
TEHQZ	$\overline{CS}$ high to high Z	40	40	40	ns	max

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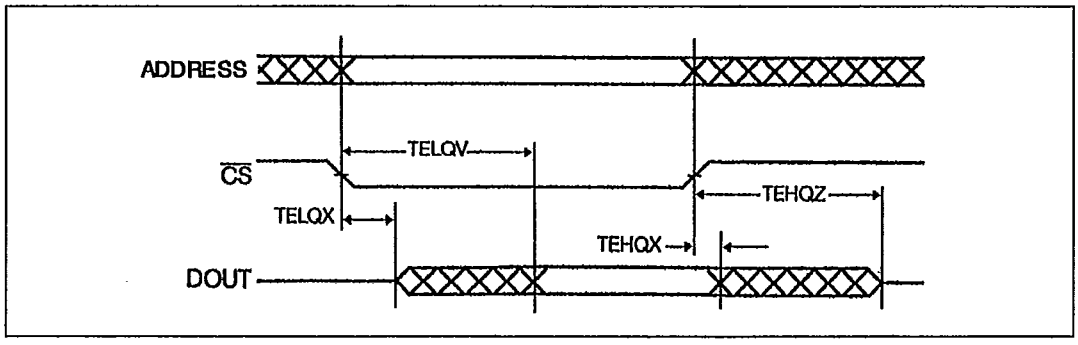
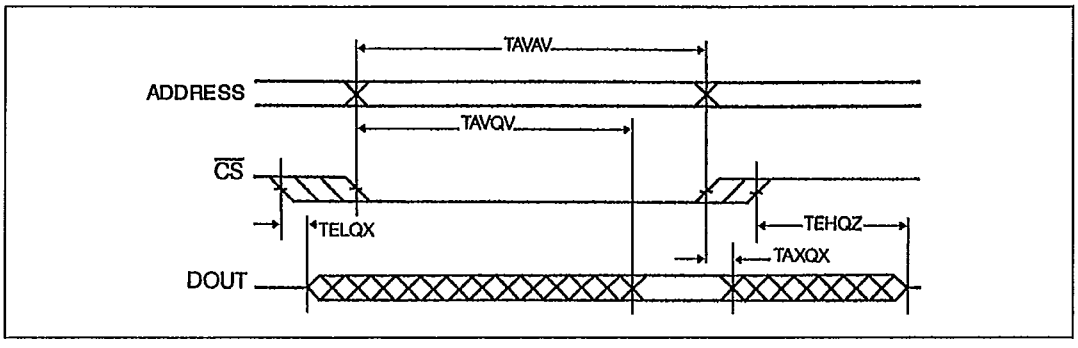
READ CYCLE nb 1



READ CYCLE nb 2



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ORDERING INFORMATION

Package
HM1
- 0 - Chip form
- 1 - Ceramic 20 pins 300 mils
- 3 - Plastic 20 pins 300 mils
- 4 - LCC 20 pins

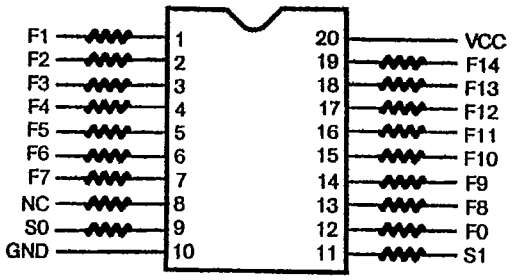
Device Type
65262
- 16 k x 1 very low power static RAM

Grade
B
- B = high speed/low current
- Blank : standard speed/low current
- C : standard

Level
– 5
- – 5 : Commercial
- – 9 : Industrial
- – 2 : Military
- – 8 : Military with B.I.

(B.I. = Burn-in)

BURN-IN SCHEMATICS



R = 1 KΩ
Fo = 50 KHz ± 20 %
Fn = 1/2 F n-1

S0, S1 : programmable signals for write / read cycles

VCC = 5.5 V

NC = Not connected

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