OSR

Applying the DLX3416* Intelligent Display® Device Appnote 17

This application note is intended to serve as a design and application guide for users of the DLX3416 (referred to as 3416 hereafter) alphanumeric Intelligent Displays. This appnote also covers device electrical description and operation, considerations for general circuit design, and interfacing the 3416 to microprocessors. Refer to the specific data sheet and other Infineon / OSRAM Appnotes for more details.

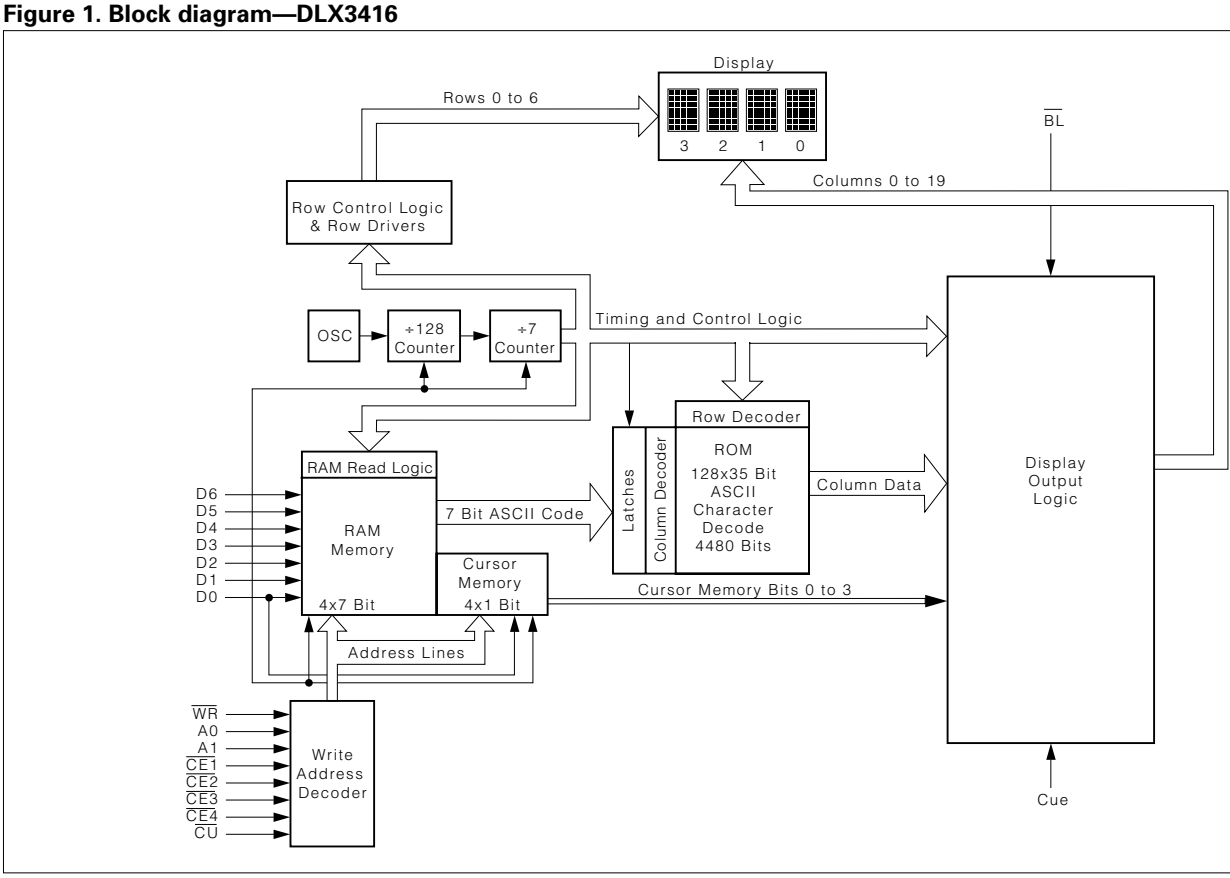
Electrical & Mechanical Description

The internal electronics in these Intelligent Displays eliminates all the traditional difficulties of using multi-digit light emitting displays (segment decoding, drivers, and multiplexing).

An Intelligent Display also provides internal mer four digits. This approach allows the user to asy address one of four digits, and load new data wi the LED multiplex timing.

Figure 1 is a block diagram of the DLX3416. The of four (5x7) LED arrays and a single CMOS inte The IC chip contains the column and row drivers ROM, four word x7 bit Random Access Memor multiplexing, multiplex counter/decoder, cursor address decoder, and miscellaneous control log

Figure 1. Block diagram—DLX3416



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Packaging

Packaging consists of a transfer molded nylon lens which also serves as an "encapsulation shell" since it covers five of the six "faces." The assembled and tested substrate ("PTF" multi-layer), is placed within the shell and the entire assembly is then filled with a water clear IC grade epoxy.

This yields a very rugged part, which is quite impervious to moisture, shock and vibration. Although not "hermetic," the device will easily withstand total immersion in water/detergent solutions.

Figure 2. Top view

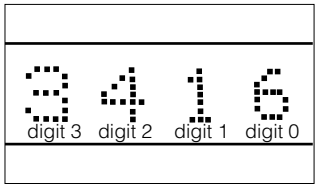


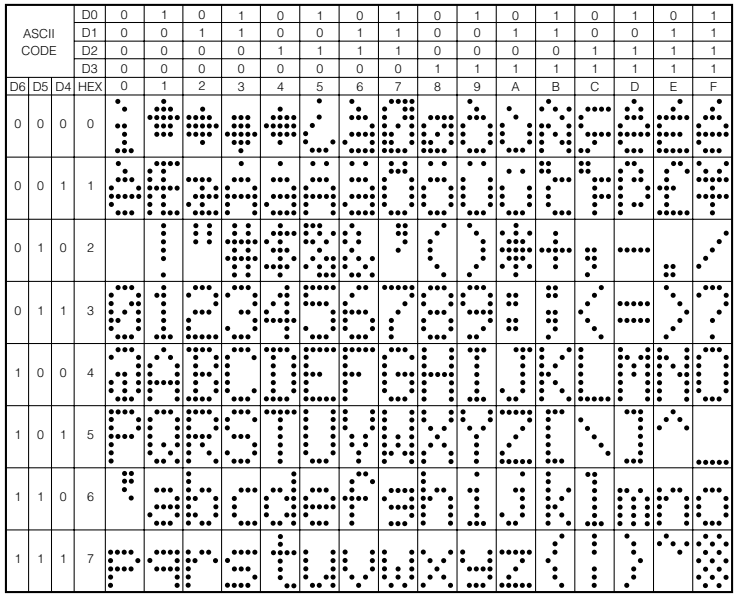
Table 1. Pin outs

Pin	Function	Pin	Function
1	$\overline{CE1}$ Chip Enable	10	GND
2	$\overline{CE2}$ Chip Enable	11	D0 Data Input
3	$\overline{CLR}$ Clear	12	D1 Data Input
4	CUE Cursor Enable	13	D2 Data Input
5	$\overline{CU}$ Cursor Select	14	D3 Data Input
6	$\overline{WR}$ Write	15	D6 Data Input
7	A1 Digit Select	16	D5 Data Input
8	A0 Digit Select	17	D4 Data Input
9	V_{CC}	18	$\overline{BL}$ Display Blank

Table 2. Electrical inputs to the 3416

V_{CC}	Positive supply +5 volts
GND	Ground
D0-D6	Data Lines The seven data input lines are d accept the first 64 ASCII charac ure 3 for DL3416 character set interprets all undefined codes a See Figure 3 for DLX3416 chara
A0, A1	Address Lines The address determines the dig which the data will be written. A is right to left for positive-true lo
$\overline{WR}$	Write (Active Low) Data and address to be loaded r present and stable before and af edge of write. (See DL3416, DL sheets for timing information).
$\overline{CE1}$, $\overline{CE2}$	Chip Enable (Active High)
$\overline{CE3}$, $\overline{CE4}$	Chip Enable (Active Low) Determines which device in an ally accept data. When either or chip enable is in the high state, are inhibited.
$\overline{CLR}$	Clear (Active Low) The data RAM and cursor RAM 3416 will be cleared when held l The minimum for the $\overline{CLR}$ is 1 m DLX3416.
CUE	Cursor Enable Activates Cursor function. Curso displayed regardless of cursor m tents when cue is Low.
$\overline{CU}$	Cursor Select (Active Low) This input must be held high to data memory and low to store d cursor memory.
$\overline{BL}$	Display Blank (Active Low) Blanking the entire display may plished by holding the $\overline{BL}$ input l stored function. When $\overline{BL}$ is rele stored characters are again disp be used for flashing or dimming

Figure 3. Character set—DLX3416



Notes: 1. High = 1 level.
2. Low = 0 level.
3. Upon power up, the device will initialize in a random state.

Clear Memory

Clearing of the entire internal four digit memory may be accomplished by holding the clear line ($\overline{CLR}$) low for one complete internal display multiplex cycle, 15 mS minimum for DL 3416, 1 mS for DLX3416. Less time may leave some data uncleared. $\overline{CLR}$ also clears the cursor memory.

Display Blanking

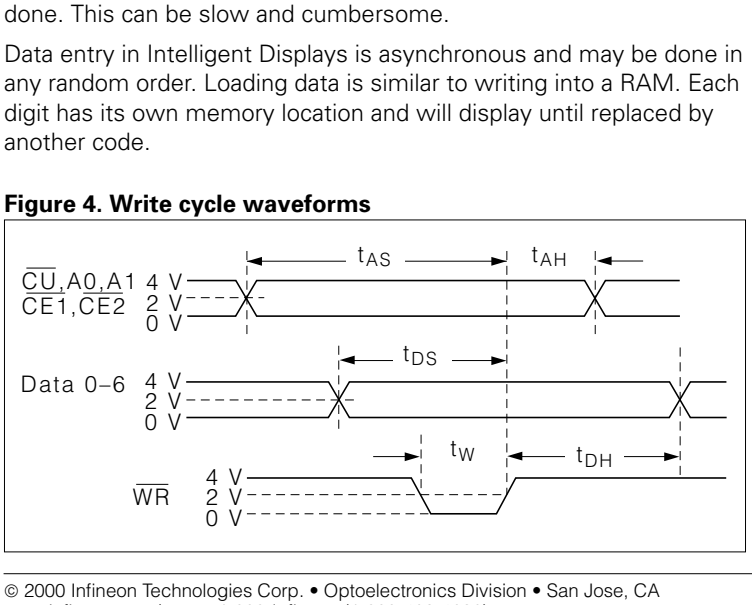
Blanking the display may be accomplished by loading a blank, space or illegal code into each digit of the display or by using the ($\overline{BL}$) display blank input. Setting the ($\overline{BL}$) input low does not affect the contents of either data or cursor memory. A flashing display can be realized by pulsing ($\overline{BL}$).

Operation

Multiplexed display systems sequentially read and display data from a memory device. In synchronous systems, control circuitry must compare the location of data to be read to the location or position of new data to be stored or displayed, i.e., synchronize before a Write can be done. This can be slow and cumbersome.

Data entry in Intelligent Displays is asynchronous and may be done in any random order. Loading data is similar to writing into a RAM. Each digit has its own memory location and will display until replaced by another code.

Figure 4. Write cycle waveforms



The waveforms of Figure 4 demonstrate t
ships of the signals required to generate a
(Check individual data sheet for minimum
be seen from the waveforms, all signals a
from the rising or trailing edge of write.

Cursor

The DLX3416 cursor function causes al
at 50% brightness. The cursor can be us
the position in the display of the next c
entered. The cursor is not a character b
the display of a stored character. Upon
cursor, the display will again show the c
stored in memory.

The cursor can be written into any digit p
ting the cursor enable (CUE) high, setting
address (A1, A0), enabling Chip Enable, (
sor select ($\overline{CU}$), Write ($\overline{WR}$) and Data (D0)
line D0 will place a cursor into the positio
address A0 and A1. Conversely, a low on
the cursor. The cursor will remain display
sor ($\overline{CU}$) and write ($\overline{WR}$) signals have bee
During the cursor-write sequence, data li
D6 are ignored by the 3416.

If the user does not wish to utilize the cur
the cursor enable (CUE) can be tied low to
cursor function. A flashing cursor can be r
ply pulsing the CUE line after cursor data
stored.

General Design Considerations

Using Positive true logic, address order is
left. For left to right address order, use th
plement" or simple inversion of the addr

For systems with only a 6 bit (abbreviated
format, Data Line D6 cannot be left open
be the complement of Data Line D5.

A "display test" or "lamp test" function c
by simply storing a cursor into all digits.

Because of the random state of the curso
power up, if the cursor function is to be u
necessary to clear cursors initially to assu
sor memories contain its zero state. This
accomplished with the $\overline{CLR}$ input.

When using the 3416 on a separate displa
more than 6 inches of cable length, it ma
to buffer all inputs. This is most easily ach
non-inverting buffers such as the 74365.
prevent transient current in the protection
buffers should be located on the display
the displays.

Local power supply bypass capacitors are
many cases. These should be 6 or 10 volt
with 10 µF or greater capacitance. Low in
tance is important due to current steps w
from the internal multiplexing of the disp

If small wire cables are used, it is good en
tice to calculate the wire resistance of the
the +5 volt wires. More than 0.1 volt drop

digit worst cast) should be avoided, since this loss is in addition to any inaccuracies or load regulation limitations of the power supply.

The 5 volt power supply for the displays should be the same one supplying V_{CC} to all logic devices which drive the display devices. If a separate supply must be used, then local buffers using hex non-inverting gates should be used on all inputs and these buffers should be powered from the display power supply. This precaution is to avoid logic inputs higher than display V_{CC} during power up or line transients.

Figure 5.

Loading Data

$\overline{BL}$	$\overline{CE1}$	$\overline{CE2}$	CUE	$\overline{CU}$	$\overline{WR}$	$\overline{CLR}$	A_1	A_0	D6	D5	D4	D3	D2	D1	D0	Digit 3	Digit 2	Digit 1	Digit 0
L	X	X	X	H	X	H	X	X	X	X	X	X	X	X	X	Blank			
H	H	X	L	H	X	H	X	X	X	X	X	X	X	X	X	Previous Characters			
H	X	H	L	H	X	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	X	X	L	H	H	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	NC
H	L	L	L	H	L	H	L	L	H	L	L	L	L	L	H	NC	NC	NC	A
H	L	L	L	H	L	H	L	H	H	L	L	L	L	H	L	NC	NC	B	A
H	L	L	L	H	L	H	H	L	H	L	L	L	L	H	H	NC	C	B	NC
H	L	L	L	H	L	H	H	H	H	L	L	L	H	L	L	D	C	NC	A
H	L	L	L	H	L	H	L	L	H	L	L	L	H	L	H	D	C	B	E
H	L	L	L	H	L	H	H	L	H	L	L	H	L	H	H	D	K	B	E
H	L	L	L	H	L	H	–	–	–	–	–	–	–	–	–	See Character Set			

Loading Cursor

																Normal Data Entry Enable Previous Stored Cursors			
H	L	L	L	H	X	H	X	X	X	X	X	X	X	X	X	NC	NC	NC	■
H	L	L	H	H	H	H	X	X	X	X	X	X	X	X	X	NC	NC	■	■
H	L	L	H	L	L	H	L	L	X	X	X	X	X	X	H	NC	■	■	■
H	L	L	H	L	L	H	L	H	X	X	X	X	X	X	H	■	■	■	■
H	L	L	H	L	L	H	H	L	X	X	X	X	X	X	H	D	K	B	E
H	L	L	H	L	L	H	H	H	X	X	X	X	X	X	H	D	K	B	E
H	L	L	L	H	H	H	X	X	X	X	X	X	X	X	X	■	■	■	■
H	L	L	L	L	L	H	L	L	X	X	X	X	X	X	L				
H	L	L	L	H	H	H	X	X	X	X	X	X	X	X	X				

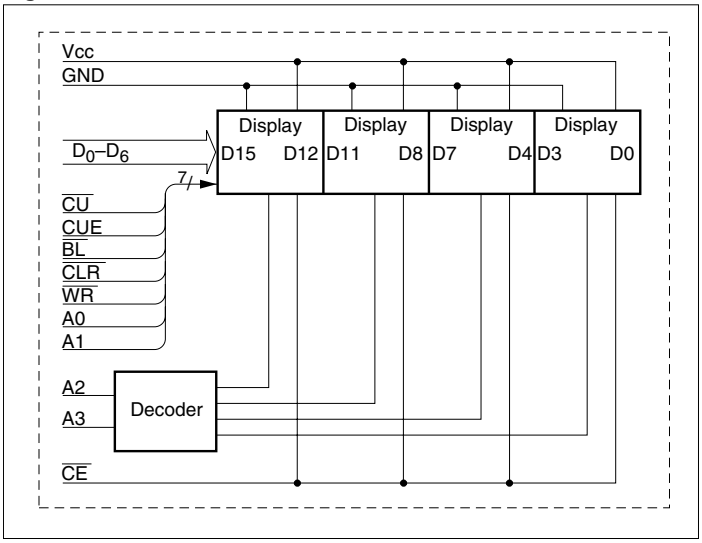
X = Don't care
NC = No change from previously displayed characters

■ = all dots/segments on at half brightness

Interfacing the 3416

A general and straightforward interface circuit is shown in Figure 6. This scheme can easily interface to µP systems or any other systems which can provide the seven data lines, appropriate address, and control lines.

Figure 6. General interface circuit



Parallel I/O

The parallel I/O device of a microprocessor ca
nected to the circuit in Figure 6. One eight bit
provide the seven input data bits and the curs
Another eight bit output port can contain the a
chip enable information and the other control

INIT:	MVI A,80H OUT CONTROL	;CONTROL DAT ;LOAD CONTR
CUSR:	MVI A,00H OUT PORT A MVI B, 0FH	;CLEAR CURSO ;LOAD DATA P ;SET CHARACT
CUSRI	:MOV A, B CALL DSPWT DCR B JNZ CUSRI MOV A, B CALL DSPWT MVI A, FFH OUT PORT B	; ;WRITE SUBRO ;DECREMENT ;DIGIT 0? ; ; ;SET DATA FOR ;LOAD CONTR
DISP:	LXI H, TABLE	;SET TABLE AD

DISP1	MOV A, M
	
	OUT PORT A
	MOV A, B
	CALL DSPWT
	
	INX H
	
	INR B
	MVI A, 10H
	CMP B
	JNZ DISP1
	HALT
		;MOVE TABLE
		ACCUMULATO
		;LOAD DATA P
		;
		;LOAD ADDRES
		CONTROL
		;INCREMENT T
		ADDRESS
		;INCREMENT C
		SET # OF DIGI
		;
		;16 CHARACTE
		;END OF PROG

DSPWT	:ORI F0H OUT PORT C ANI 7FH OUT PORT C ORI F0H OUT PORT C RET	;SET CONTROL ;LOAD CONTR ;SET WRITE BI ;LOAD WRITE ORI F0H ;LOAD CONTR
TABLE:	DB DB DB DB DB DB DB DB DB DB DB DB DB DB DB DB	;0C3H ;0C9H ;0D4H ;0D3H ;0C1H ;0D4H ;0CEH ;0C1H ;0C6H ;0A0H ;0D3H ;0D4H ;0C8H ;0C7H ;0C9H ;0CCH

Figure 7. 16-digit parallel I/O system

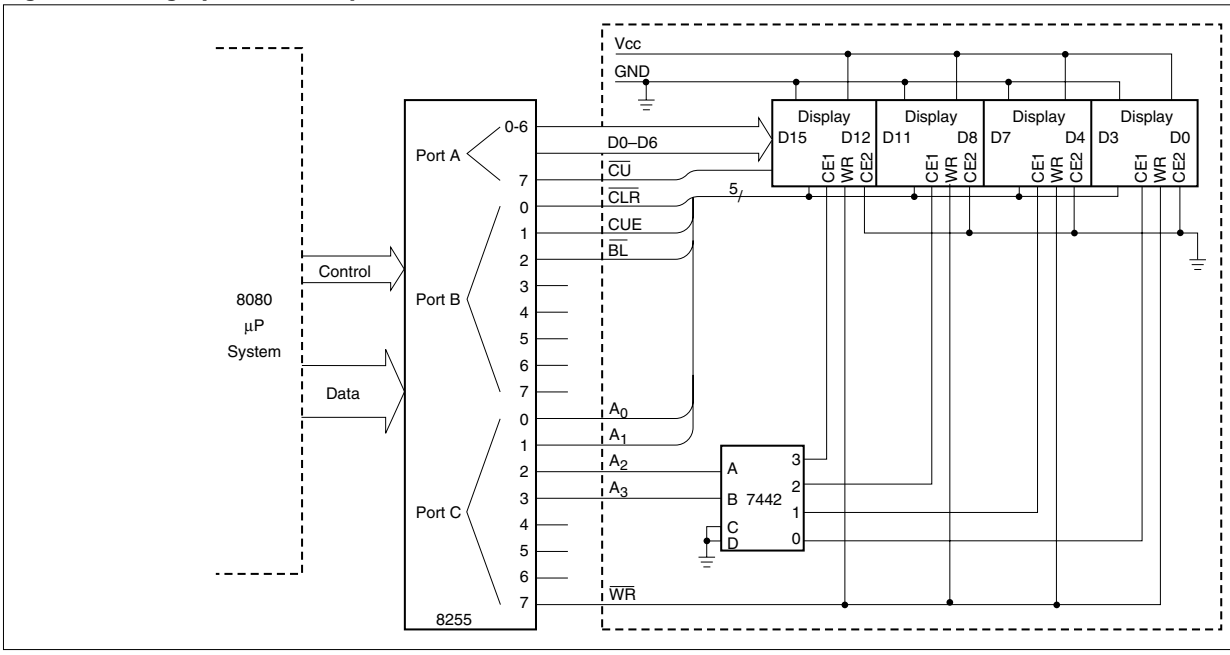


Figure 8. Mapped interface.

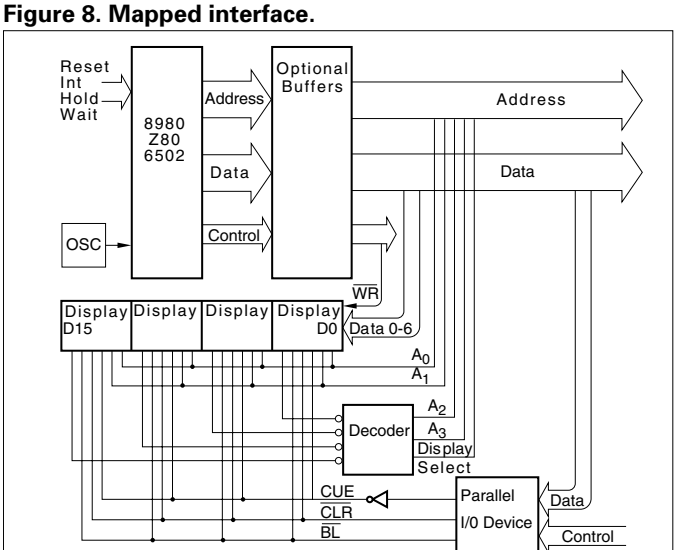


Figure 9. Interface with 6800 microprocessor

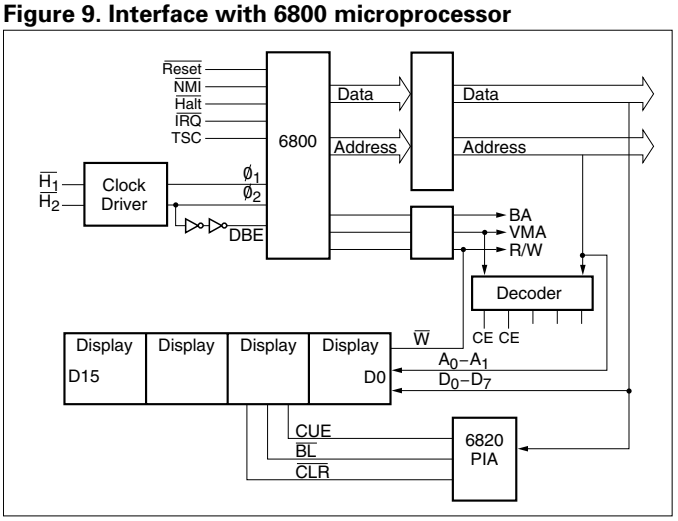


Figure 7 illustrates a 16 character display with a using the 8255 programmable peripheral interfa The following program will display a simple 16 c sage using this interface.

I/O or Memory Mapped Addressing

Some designers may wish to avoid the addition allel I/O in their system. Structuring the addressi for the 3416 to look like a set of peripheral or ou (I/O mapped) or RAM's and ROM's (memory ma easy. Figure 8 shows the simplicity of interfacin cessors, such as 8080, Z80 and 6502 as examp

The interface with the 6800 microprocessor in F trates the need for designers to check the timin of the 3416 and the µP. The typical data output h 30 ns for DBE=Ø2 timing; two inverters in the D added to increase the data output hold time for with the 50 nS minimum specification of the 34

Conclusion

Note that although other manufacturers' produc examples, this application note does not imply s endorsement, or recommendation or warranty o facturer's products by Infineon / OSRAM.

The interface schemes shown demonstrate the using the 3416 with microprocessors. The slight encountered with various microprocessors to int 3416 are similar to those encountered when usi RAMs. The techniques used in the examples w their generality, and any display of this family ar able in these examples. The user will undoubted schemes to optimize his particular system to its