

Logic Diagram

FEATURES:

- 14-bit resolution and accuracy
- Total dose hardness:
 - > 100 krad (Si), depending upon space mission
- Single event effects:
 - SEL > 104 MeV/mg/cm²
 - SEU_{TH} = 1.4 MeV/mg/cm²
 - SEU_{Sat} = 1E-3 cm²/Device
- Package:
 - 16 pin RAD-PAK[®] flat package
 - 16 pin RAD-PAK[®] dual-in-line package
- Fast Conversion Times: 10 μs
- Low 50 mW typical power consumption
- High speed LC²MOS technology
 - Analog input range of ±3V
 - 83 KSPS throughput rate
 - Operates with +5V/-5V power supplies
 - 80 dB SNR at 10 kHz input frequency
 - 2 s complement coding
 - Serial output

DESCRIPTION:

Maxwell Technologies' 7872 high-speed 14-bit ADC microcircuit features a greater than 100 krad (Si) total dose tolerance; depending upon orbit. The 7872 consists of a track/hold amplifier, successive-approximation ADC, 3V buried Zener reference and versatile interface logic. It features a self-contained, laser-trimmed internal clock, so no external clock timing components are required. For minimum noise possible, the on-chip clock may be overridden to synchronize the device operation to the digital system. The 7872 is a serial output device. It is capable of interfacing to all modern microprocessors and digital signal processors. The 7872 operates from ±5V power supplies, accepts bipolar input signals of ±3V and is able to convert full power signals up to 41.5 kHz. It is also fully specified for dynamic performance parameters including distortion and signal-to-noise ratio.

Maxwell Technologies' patented RAD-PAK[®] packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, RAD-PAK provides greater than 100 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

TABLE 1. 7872 PIN DESCRIPTION

PIN	SIGNAL	DESCRIPTION
1	CONTROL	Control Function
2	CONVST	Convert Start
3	CLK	Clock Input
4	SSTRB	Serial Strobe
5	SCLK	Serial Clock
6	SDATA	Serial Data
7	NC	Non Connect
8	DGND	Digital Ground
9	V _{DD}	Positive Supply
10	NC	No Connect
11	C _{REF}	Reference Capacitor
12	AGND	Analog Ground
13	REF _{OUT}	Voltage Reference Output
14	V _{IN}	Analog Input
15	V _{SS}	Negative Supply
16	V _{DD}	Positive Supply

TABLE 2. 7872 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT
Positive Supply Voltage; Relative to GND	V _{DD}	-0.3	7.0	V
Negative Supply Voltage; Relative to GND	V _{SS}	0.3	7.0	V
AGND to DGND; Relative to GND	--	-0.3	V _{DD} +0.3	V
REF _{OUT} , C _{REF} to AGND	--	0	V _{DD}	V
V _{IN} to AGND	--	V _{SS} -0.3	V _{DD} +0.3	V
Digital Input Voltage	V _{IN}	-0.3	V _{DD} +0.3	V
Digital Output Voltage	V _{OUT}	-0.3	V _{DD} +0.3	V
Thermal Impedance	Θ _{JC}	--	2.44	°C/W
Storage Temperature Range	T _S	-65	150	°C
Operating Temperature Range	T _A	-55	125	°C

TABLE 3. 7872 DC ELECTRICAL CHARACTERISTICS FOR DYNAMIC PERFORMANCE ¹

($V_{DD} = 5\text{ V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$, AGND = DGND = 0 V,
 $f_{CLK} = 2\text{ MHz}$ EXTERNAL, $f_{SAMPLE} = 83\text{ kHz}$, -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	TYP	MAX	UNIT
Signal to Noise Ratio $V_{IN} = 10\text{kHz}$ Sine Wave, T_{MIN} to T_{MAX} SNR is typically 82dB for $V_{IN} < 41.5\text{kHz}$ ²	SNR	4, 5, 6	79	--	--	dB
Total Harmonic Distortion $V_{IN} = 10\text{kHz}$ Sine Wave	THD	4, 5, 6	--	-86	--	dB
Peak Harmonic or Spurious Noise	--	4, 5, 6	--	-86	--	dB
Intermodulation Distortion Second Order Terms: $f_a = 9\text{ kHz}$, $f_b = 9.5\text{ kHz}$, $f_{SAMPLE} = 50\text{ kHz}$ Third Order Terms: $f_a = 9\text{ kHz}$, $f_b = 9.5\text{ kHz}$, $f_{SAMPLE} = 50\text{ kHz}$	IMD	4, 5, 6	-- --	-86 -86	-- --	dB
Track/Hold Acquisition Time	--	4, 5, 6	--	--	2	μs

1. $V_{IN} = \pm 3\text{ V}$. Guaranteed by design.
2. SNR calculation includes distortion and noise components.

TABLE 4. 7872 DC ELECTRICAL CHARACTERISTICS FOR ACCURACY

($V_{DD} = 5\text{V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$, $T_A = -55$ TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUGROUPS	MIN	TYP	MAX	UNIT
Resolution	--	1, 2, 3	14	--	--	Bits
Resolution for Which No Missing Codes are Guaranteed	--	1, 2, 3	14	--	--	Bits
Integral Nonlinearity @ 25 °C	--	1, 2, 3	--	± 1	--	LSB
Integral Nonlinearity T_{MIN} to T_{MAX}	--	1, 2, 3	--	--	± 2	LSB
Bipolar Zero Error	--	1, 2, 3	--	--	± 12	LSB
Positive Gain Error ¹	--	1, 2, 3	--	--	± 12	LSB
Negative Gain Error ¹	--	1, 2, 3	--	--	± 12	LSB

1. Measured with respect to internal reference.

TABLE 5. 7872 DC ELECTRICAL CHARACTERISTICS FOR ANALOG INPUT

($V_{DD} = 5\text{V} \pm 5\%$, $V_{SS} = -5\text{ V} \pm 5\%$, $T_A = -55$ TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
Input Voltage Range	--	1, 2, 3	-3	3	V
Input Current	--	1, 2, 3	-500	500	μA

TABLE 6. 7872 DC ELECTRICAL CHARACTERISTICS FOR REFERENCE OUTPUT

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125^\circ\text{C UNLESS OTHERWISE SPECIFIED})$

PARAMETER	SYMBOL	SUGGROUPS	MIN	MAX	UNIT
REF _{OUT} @ +25 °C	--	1, 2, 3	2.99	3.01	V
REF _{OUT} T _{MIN} to T _{MAX}	--	1, 2, 3	2.98	3.02	V
REF _{OUT} Tempco: Typically 35ppm	--	1, 2, 3	--	±40	ppm/°C
Reference Load Sensitivity (DREF _{OUT} /DI) Reference Load Current Change (0-300 μA); Reference Load Should Not Be Changed During Conversion	--	1, 2, 3	--	1.2	mV

TABLE 7. 7872 DC ELECTRICAL CHARACTERISTICS FOR LOGIC INPUTS

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125^\circ\text{C UNLESS OTHERWISE SPECIFIED})$

PARAMETER	SYMBOL	SUGGROUPS	MIN	MAX	UNIT
Input High Voltage: V _{DD} 5 V ± 5%	V _{INH}	1, 2, 3	2.4	--	V
Input Low Voltage: V _{DD} 5 V ± 5%	V _{INL}	1, 2, 3	--	0.8	V
Input Current: V _{IN} = 0 V to V _{DD}	I _{IN}	1, 2, 3	-10	10	μA
Input Current: (14/8/CLK input only) VIN = VSS to VDD	--	1, 2, 3	-10	10	μA
Input Capacitance ¹	C _{IN}	1, 2, 3	--	10	pF

1. Not tested.

TABLE 8. 7872 DC ELECTRICAL CHARACTERISTICS FOR LOGIC OUTPUTS

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125^\circ\text{C UNLESS OTHERWISE SPECIFIED})$

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
Output High Voltage I _{SOURCE} = 40 μA	V _{OH}	1, 2, 3	4.0	--	V
Output Low Voltage I _{SINK} = 1.6 mA	V _{OL}	1, 2, 3	--	0.4	V
Floating-State Leakage Current	--	1, 2, 3	--	10	μA
Floating-State Output Capacitance ¹	--	1, 2, 3	--	15	pF

1. Not tested.

TABLE 9. 7872 DC ELECTRICAL CHARACTERISTICS FOR CONVERSION TIME

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125^\circ\text{C UNLESS OTHERWISE SPECIFIED})$

PARAMETER	SYMBOL	SUBGROUPS	MIN	MAX	UNIT
External Clock	--	1, 2, 3	--	10	μs
Internal Clock: Nominal Value = 2 MHz	--	1, 2, 3	--	11	μs

TABLE 10. 7872 DC ELECTRICAL CHARACTERISTICS FOR POWER REQUIREMENTS

 $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125^\circ\text{C UNLESS OTHERWISE SPECIFIED})$

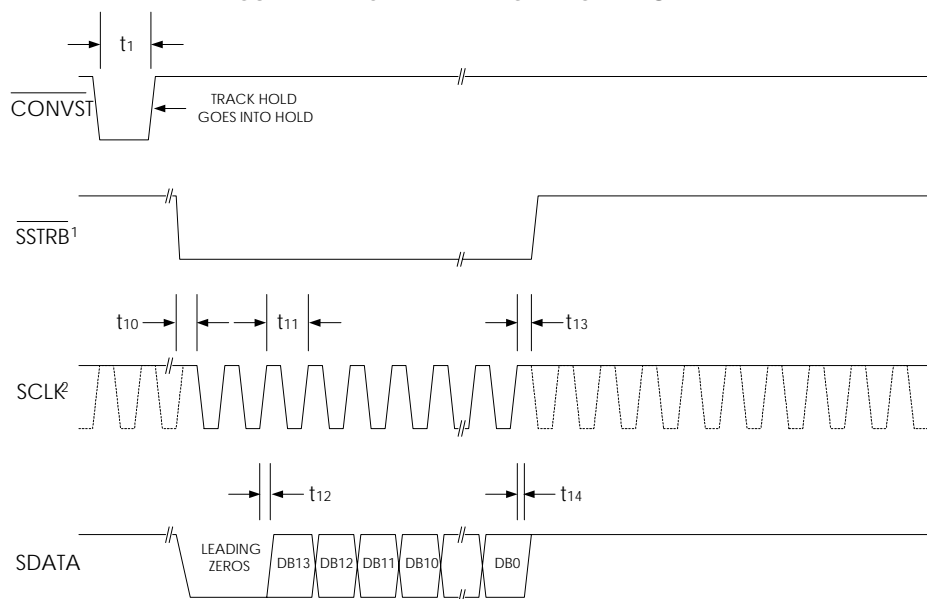
PARAMETER	SYMBOL	CONDITIONS	REQUIREMENTS	UNITS
Positive Supply Voltage	V_{DD}	5% for Specified Performance	5	V
Negative Supply Voltage	V_{SS}	5% for Specified Performance	-5	V
Positive Supply Current	I_{DD}	Typically 6mA	13	mA max
Negative Supply Current	I_{SS}	Typically 4mA	6	mA max
Power Dissipation	P_D	Typically 50mW	95	mW max

TABLE 11. 7872 TIMING CHARACTERISTICS ^{1,2} $(V_{DD} = 5V \pm 5\%, V_{SS} = -5V \pm 5\%, T_A = -55 \text{ TO } 125^\circ\text{C UNLESS OTHERWISE SPECIFIED})$

PARAMETER/CONDITION	SYMBOL	SUBGROUPS	MIN	MAX	UNITS
$\overline{\text{CONVST}}$ Pulse Width	t_1	9, 10, 11	50	--	ns
$\overline{\text{SSTRB}}$ to SCLK Falling Edge Setup Time	t_{10}	9, 10, 11	100	--	ns
SCLK Cycle Time ³	t_{11}	9, 10, 11	440	--	ns
SCLK to Valid Data Delay: $C_L = 35 \text{ pF}$ ⁴	t_{12}	9, 10, 11	--	155	ns
SCLD Rising Edge to $\overline{\text{SSTRB}}$	t_{13}	9, 10, 11	20	150	ns
Bus Relinquish Time After SCLK	t_{14}	9, 10, 11	4	100	ns

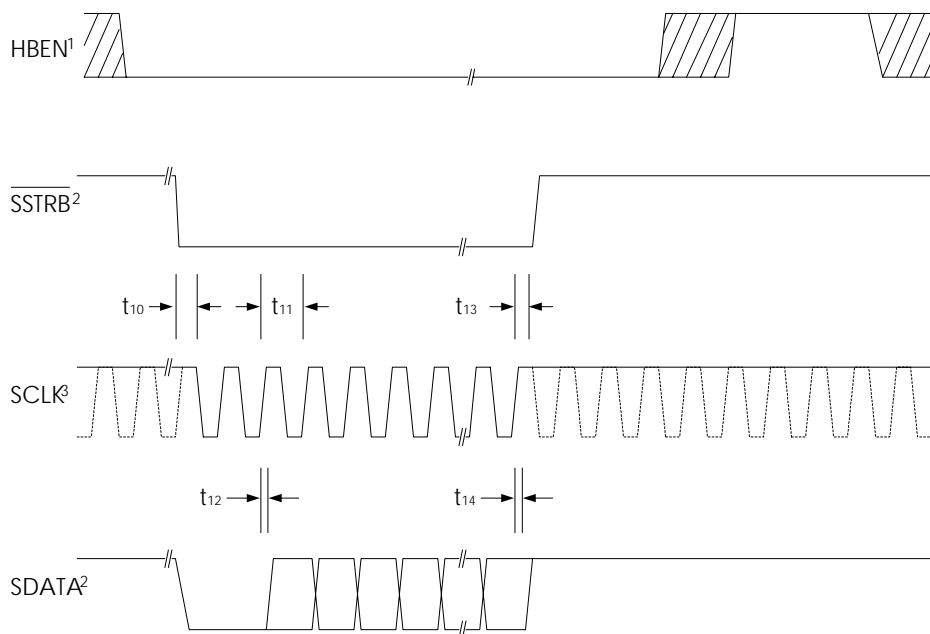
1. All input signals are specified with $t_r = t_f = 5 \text{ ns}$ (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
2. Serial timing is measured with a $4.7 \text{ k}\Omega$ pull-up resistor on SDATA and $\overline{\text{SSTRB}}$ and a $2 \text{ k}\Omega$ pull-up resistor on SCLK. The capacitance on all three outputs is 35 pF.
3. SCLK mark/space ration (measured from a voltage level of 1.6 V) is 40/60 to 60/40.
4. SDATA will drive higher capacitive loads, but this will add to t_{12} since it increases the external RC time constant ($4.7\text{k}\Omega/C_L$) and hence, the time to reach 2.4 V.

FIGURE 1. MODE 1 TIMING DIAGRAM SERIAL



1. External 4.7 k Ω pull-up resistor.
2. External 2 k Ω pull-up resistor continuous SCLK (DASHED LINE) when 14/8/CLK (CONTROL) = -5 V; noncontinuous when 14/8/CLK (CONTROL) = 0 V.

FIGURE 2. MODE 2 TIMING DIAGRAM, SERIAL READ



1. Times t_{15} , t_{18} , t_{19} and t_{20} are the same for a high byte read as for a low byte read.
2. External 4.7 k Ω pull-up resistor.
3. Continuous SCLK (DASHED LINE) when 14/8/CLK (CONTROL) = -5 V; noncontinuous when 14/8/CLK (CONTROL) = 0 V. External 2 k Ω pull-up resistor.

FIGURE 3. LOAD CIRCUIT FOR ACCESS TIME

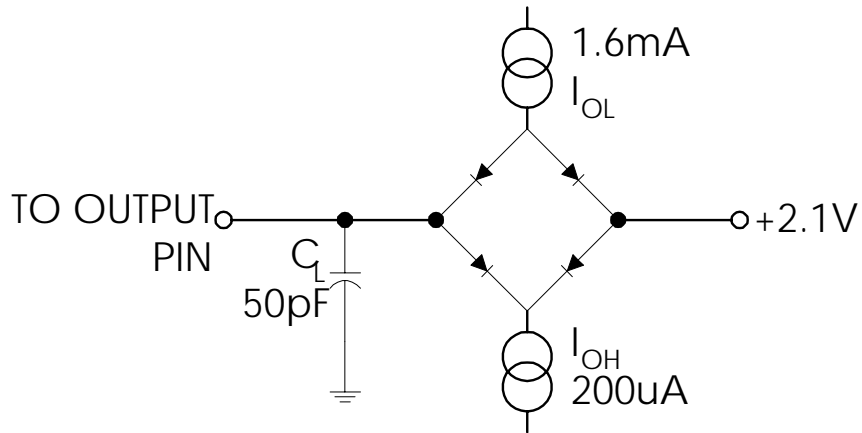
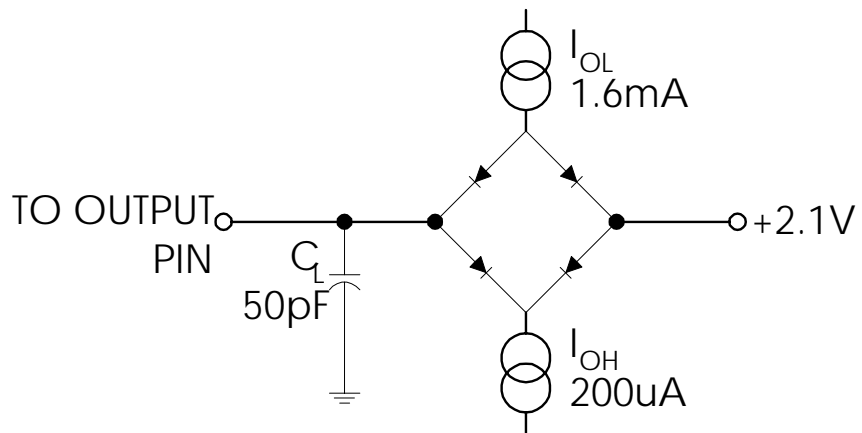
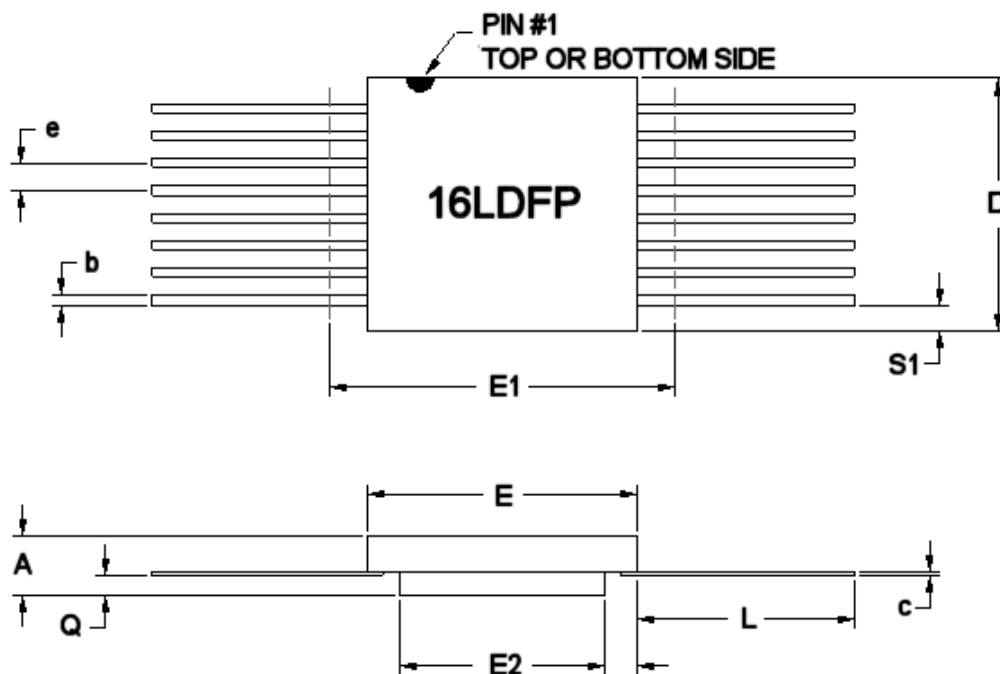


FIGURE 4. LOAD CIRCUIT FOR OUTPUT FLOAT DELAY



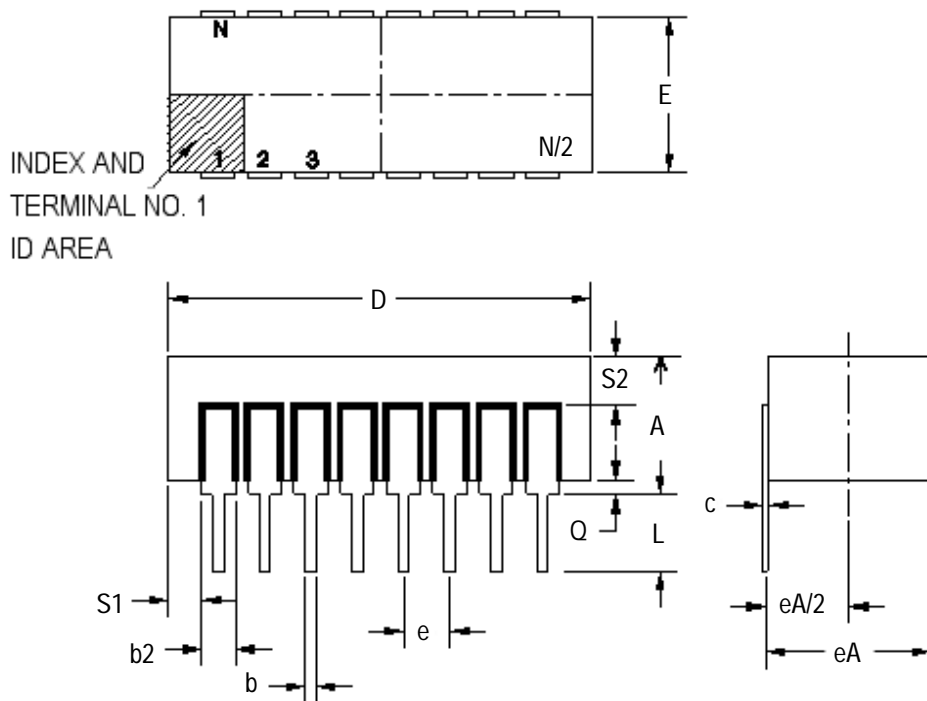


16 PIN RAD-PAK® FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.116	0.130	0.143
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.415	0.440
E	0.245	0.280	0.285
E1	--	--	0.315
E2	0.130	0.156	--
E3	0.030	0.062	--
e	0.050 BSC		
L	0.325	0.335	0.345
Q	0.020	0.033	0.045
S1	0.005	0.024	--
N	16		

F16-01

Note: All dimensions in inches



16 PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.157	0.200
b	0.014	0.018	0.026
b2	0.045	0.047	0.065
c	0.008	0.010	0.018
D	--	0.800	0.840
E	0.220	0.295	0.310
eA	0.300 BSC		
eA/2	0.150 BSC		
e	0.100 BSC		
L	0.135	0.145	0.155
Q	0.000	0.002	0.060
S1	0.005	0.027	--
S2	0.005	--	--
N	16		

D16-01

Note: All dimensions in inches

Important Notice:

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