SGS-THOMSON MICROELECTRONICS

EF6808R2

8–BIT MICROCOMPUTER WITH A/D

HARDWARE FEATURES

- A/D CONVERTER
  - 8-BIT CONVERSION, MONOTONIC
  - 4 MULTIPLEXED ANALOG INPUTS
  - RATIOMETRIC CONVERSION
- 32 TTL/CMOS COMPATIBLE I/O LINES
  - 24 BIDIRECTIONAL (8 Lines are LED Compatible)
  - 8 INPUT-ONLY
- 2048 BYTES OF USER ROM
- 64 BYTES OF RAM
- SELF-CHECK MODE
- ZERO-CROSSING DETECT/INTERRUPT
- INTERNAL 8-BIT TIMER WITH 7-BIT MASK PROGRAMMABLE PRESCALER AND CLOCK SOURCE
- 5V SINGLE SUPPLY

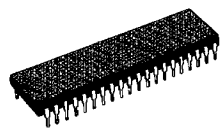
SOFTWARE FEATURES

- 10 POWERFUL ADDRESSING MODES
- BYTE EFFICIENT INSTRUCTION SET WITH TRUE BIT MANIPULATION, BIT TEST, AND BRANCH INSTRUCTIONS
- SINGLE INSTRUCTION MEMORY EXAMINE/CHANGE
- POWERFUL INDEXED ADDRESSING FOR TABLES
- FULL SET OF CONDITIONAL BRANCHES
- MEMORY USABLE AS REGISTER/FLAGS
- COMPLETE DEVELOPMENT SYSTEM SUPPORT INICE®

USER SELECTABLE OPTIONS

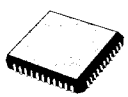
- INTERNAL 8-BIT TIMER WITH SELECTABLE CLOCK SOURCE (external timer input or internal machine clock)
- TIMER PRESCALER OPTION (7 Bits, 2^n)
- 8 BIDIRECTIONAL I/O LINES WITH TTL OR TTL/CMOS INTERFACE OPTION
- 8 BIDIRECTIONAL I/O LINES WITH TTL OR OPEN-DRAIN INTERFACE OPTION
- CRYSTAL OR LOW-COST RESISTOR OSCILLATOR OPTION
- LOW VOLTAGE INHIBIT OPTION
- VECTORED INTERRUPTS : TIMER, SOFTWARE, AND EXTERNAL
- USER CALLABLE SELF-CHECK SUBROUTINES

CB-182



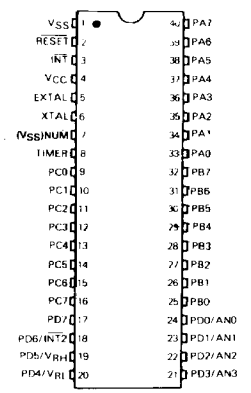
P SUFFIX
Plastic Package

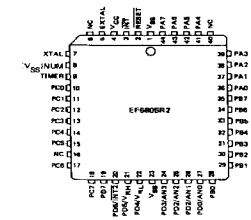
CB-521



FN SUFFIX
PLCC44

PIN CONNECTIONS

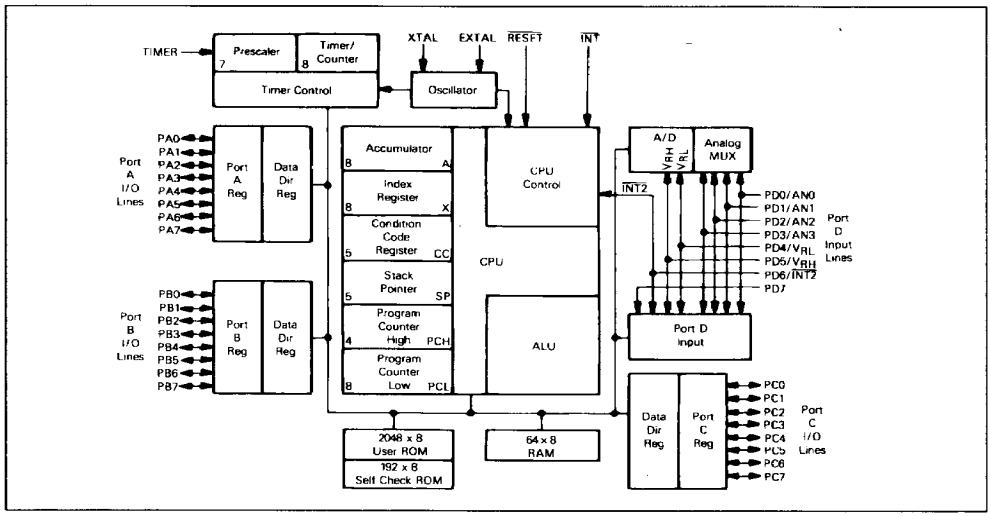




DESCRIPTION

The EF6805R2 Microcomputer Unit (MCU) is a member of the 6805 Family of low-cost single-chip Microcomputers. The 8-bit microcomputer contains a CPU, on-chip CLOCK, ROM, RAM, I/O, 4-channel 8-bit A/D, and TIMER. It is designed for the user who needs an economical microcomputer with the proven capabilities of the 6800-based instruction set. A comparison of the key features of several members of the 6805 Family of Microcomputers is shown **at the end of this data sheet. The following are some of the hardware and software highlights of the EF6805R2 MCU.**

Figure 1 : EF6805R2 HMOS Microcomputer Block Diagram.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	− 0.3 to + 7.0	V
V_{in}	Input Voltage (except TIMER in self-check mode and open-drain inputs)	− 0.3 to + 7.0	V
V_{in}	Input Voltage (open-drain pins, TIMER pin in self-check mode)	− 0.3 to + 15.0	V
T_A	Operating Temperature Range V Suffix (T_L to T_H) T Suffix	0 to + 70 − 40 to + 85 − 40 to + 105	°C
T_{stg}	Storage Temperature Range	− 55 to + 150	°C
T_J	Junction Temperature Plastic Package PLCC	150 150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electrical fields ; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{CC}$. Reliability of operation is enhanced if unused inputs except EXTAL are tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{CC}).

THERMAL DATA

θ_{JA}	Thermal Resistance	Plastic PLCC	50 80	°C/W

POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from :

$T_J = T_A + (PD \cdot \theta_{JA})$ (1)

Where :

T_A = Ambient Temperature, °C

θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{PORT}$

$P_{INT} = I_{CC} \times V_{CC}$, Watts - Chip Internal Power

P_{PORT} = Port Power Dissipation, Watts - User Determined

For most applications $P_{PORT} << P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is :

$P_D = K \div (T_J + 273°C)$ (2)

Solving equations 1 and 2 for K gives :

$K = PD \cdot (T_A + 273°C) + \theta JA \cdot P_D^2$ (3)

Where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

ELECTRICAL CHARACTERISTICS

(V_{CC} = + 5.25Vdc ± 0.5Vdc, V_{SS} = 0Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage				V
	RESET (4.75 ≤ V_{CC} ≤ 5.75)	4.0		V_{CC}	
	(V_{CC} < 4.75)	V_{CC} − 0.5		V_{CC}	
	INT (4.75 ≤ V_{CC} ≤ 5.75)	4.0	•	V_{CC}	
	(V_{CC} < 4.75)	V_{CC} − 0.5	•	V_{CC}	
	All Other (except timer)	2.0		V_{CC}	
V_{IH}	Input High Voltage Timer				V
	Timer Mode	2.0		V_{CC} + 1.0	
	Self-check Mode	9.0	10.0	15.0	
V_{IL}	Input Low Voltage				V
	RESET	V_{SS}		0.8	
	INT	V_{SS}	•	1.5	
	All Other (except A/D inputs)	V_{SS}		0.8	
	RESET Hystereris Voltages (see figures 10, 11 and 12)				V
V_{IRES+}	"Out of Reset"	2.1		4.0	
V_{IRES-}	"Into Reset"	0.8		2.0	
V_{INT}	INT Zero Crossing Input Voltage, Through a Capacitor	2		4	$V_{ac\ p\text{-}p}$
P_D	Power Dissipation - (no port loading, V_{CC} = 5.75V)				mW
	T_A = 0°C		520	740	
	T_A = − 40°C		580	800	
C_{in}	Input Capacitance				pF
	EXTAL		25		
	All Other Except Analog Inputs (see note)		10		
V_{LVR}	Low Voltage Recover			4.75	V
V_{LVI}	Low Voltage Inhibit	2.75	3.75	4.70	V
I_{in}	Input Current				µA
	TIMER (V_{in} = 0.4V)			20	
	INT (V_{in} = 2.4V to V_{CC})		20	50	
	EXTAL (V_{in} = 2.4V to V_{CC} - crystal option)			10	
	(V_{in} = 0.4V - crystal option)			− 1600	
	RESET (V_{in} = 0.8V) - External Capacitor Charging Current	− 4.0		− 40	

Note : Port D Analog Inputs, when selected, C_{in} = 25pF for the first 5 out of 30 cycles.
* Due to internal biasing this input (when unused) floats to approximately 2.2V.

SWITCHING CHARACTERISTICS

(V_{CC} = + 5.25Vdc ± 0.5Vdc, V_{SS} = 0Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit
f_{osc}	Oscillator Frequency	0.4		4.2	MHz
t_{cyc}	Cycle Time ($4/f_{osc}$)	0.95		10	µs
t_{WL}, t_{WH}	$\overline{INT}$, $\overline{INT2}$, and TIMER Pulse Width (see interrupt section)	t_{cyc} + 250			ns
t_{RWL}	$\overline{RESET}$ Pulse Width	t_{cyc} + 250			ns
f_{INT}	$\overline{INT}$ Zero-crossing Detection Input Frequency	0.03		1	kHz
	External Clock Input Duty Cycle (EXTAL)	40	50	60	%
	Crystal Oscillator Start-up Time*			100	ms

* See Figure 16 for typical crystal parameters.

A/D CONVERTER CHARACTERISTICS

(V_{CC} = + 5.25Vdc ± 0.5Vdc, V_{SS} = 0Vdc, $T_A = T_L$ to T_H unless otherwise noted)

Parameter	Comments	Min.	Typ.	Max.	Unit
Resolution		8	8	8	Bits
Non-linearity	For V_{RH} = 4.0 to 5.0V and V_{RL} = 0V			± 1/2	LSB
Quantizing Error				± 1/2	LSB
Conversion Range		V_{RL}		V_{RH}	V
V_{RH}	A/D accuracy may decrease proportionately as V_{RH} is reduced below 4.0V. The sum of V_{RH} and V_{RL} must not exceed V_{CC}.			V_{CC}	V
V_{RL}		V_{SS}		0.2	V
Conversion Time	Includes Sampling Time	30	30	30	t_{cyc}
Monotonicity	Inherent (within total error)				
Zero Input Reading	V_{in} = 0	00	00	01	Hexa-decimal
Ratiometric Reading	$V_{in} = V_{RH}$	FE	FF	FF	Hexa-decimal
Sample Time		5	5	5	t_{cyc}
Sample/hold Capacitance, Input				25	pF
Analog Input Voltage	Negative transients on any analog lines (pins 19-24) are not allowed at any time during conversion	V_{RL}		V_{RH}	V

PORT ELECTRICAL CHARACTERISTICS

(V_{CC} = + 5.25Vdc ± 0.5Vdc, V_{SS} = 0Vdc, $T_A = T_L$ to T_H unless otherwise noted)

PORT A WITH CMOS DRIVE ENABLED

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage (I_{Load} = 1.6mA)			0.4	V
V_{OH}	Output High Voltage I_{Load} = – 100µA I_{Load} = – 10µA	 2.4 V_{CC} – 1.0			V
V_{IH}	Input High Voltage (I_{Load} = – 300µA max.)	2.0		V_{CC}	V
V_{IL}	Input Low Voltage (I_{Load} = – 500µA max.)	V_{SS}		0.8	V
I_{IH}	High Z State Input Current (V_{in} = 2.0V to V_{CC})			– 300	µA
I_{IL}	High Z State Input Current (V_{in} = 0.4V)			– 500	µA

PORT B

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage I_{Load} = 3.2mA I_{Load} = 10mA (sink)			 0.4 1.0	V
V_{OH}	Output High Voltage I_{Load} = – 200µA	2.4			V
I_{OH}	Darlington Current Drive (source) V_O = 1.5V	– 1.0		– 10	mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	V_{SS}		0.8	V
I_{TSI}	High Z State Input Current		< 2	10	µA

PORT C AND PORT A WITH CMOS DRIVE DISABLED

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	Output Low Voltage I_{Load} = 1.6mA			0.4	V
V_{OH}	Output High Voltage I_{Load} = – 100µA	2.4			V
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	V_{SS}		0.8	V
I_{TSI}	High Z State Input Current		< 2	10	µs

PORT C (open-drain option)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		13.0	V
V_{IL}	Input Low Voltage	V_{SS}		0.8	V
I_{LOD}	Input Leakage Current		< 3	15	µA
V_{OL}	Output Low Voltage I_{Load} = 1.6mA			0.4	V

PORT D (digital inputs only)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	2.0		V_{CC}	V
V_{IL}	Input Low Voltage	V_{SS}		0.8	V
I_{in}	Input Current*		< 1	5	µA

* PD4/VRL – PD5/VRH : The A/D conversion resistor (15kΩ typical) is connected internally between these two lines, impacting their use as digital inputs in some applications.

Figure 2 : TTL Equivalent Test Load (port B).

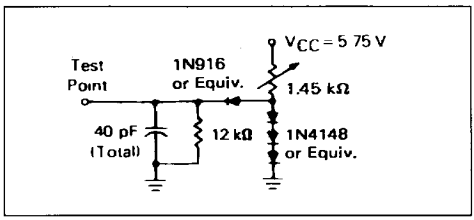


Figure 3 : CMOS Equivalent Test Load (port A).

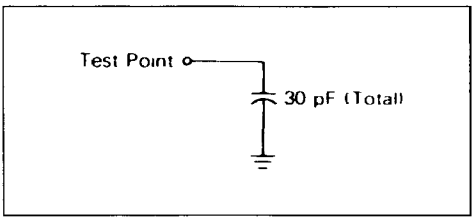


Figure 4 : TTL Equivalent Test Load (port A and C).

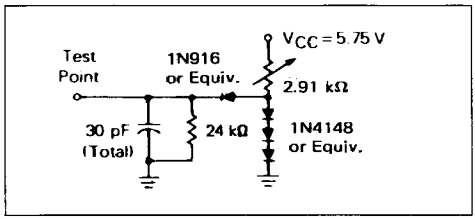
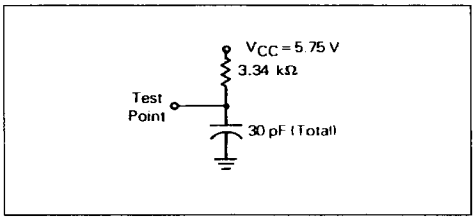


Figure 5 : Open–Drain Equivalent Test Load (port C).



SIGNAL DESCRIPTION

The input and output signals for the MCU, shown in figure 1, are described in the following paragraphs.

V_{CC} and V_{SS} - Power is supplied to the MCU using these two pins. V_{CC} is power and V_{SS} is the ground connection.

INT - This pin provides the capability for asynchronously applying an external interrupt to the MCU. Refer to Interrupts Section for additional information.

NUM (NON USER MODE) - This pin is not for user application and must be connected to V_{SS}.

XTAL AND EXTAL - These pins provide control input for the on-chip clock oscillator circuit. A crystal, a resistor, or an external signal, depending on user selectable manufacturing mak option, can be connected to these pins to provide a system clock with various degrees of stability/cost tradeoffs. Lead length and stray capacitance on these two pins should be minimized. Refer to Internal Clock Generator Options Section for recommendations about these inputs.

TIMER - The pin allows an external input to be used to control the internal timer circuitry and also to initiate the self test program. Refer to Timer Section for additional information about the timer circuitry.

RESET - This pins allows resetting of the MCU at times other than the automatic resetting capability already in the MCU. The MCU can be reset by pulling $\overline{\text{RESET}}$ low. Refer to Resets Section for additional information.

INPUT/OUTPUT LINES (PA0-PA7, PB0-PB7, PC0-PC7, PD0-PD7) - These 32 lines are arranged into four 8-bit ports (A, B, C, and D). Ports A, B, and C are programmable as either inputs or outputs under software control of the data direction registers (DDRs). Port D has up to four analog inputs, plus two voltage reference inputs when the A/D converter is used ($PD5/V_{RH}$, $PD4/V_{RL}$), and an INT2 input, and from one to eight digital inputs. If any analog input is used, then the voltage reference pins ($PD5/V_{RH}$, $PD4/V_{RL}$) must be used in the analog mode. Refer to Input/Output Section, A/D Converter Section, and Interrupts Section for additional information.

MEMORY - The MCU is capable of addressing 4096 bytes of memory and I/O registers with its program counter. The EF6805R2 MCU has implemented 2316 of these bytes. This consists of : 2048 user ROM bytes, 192 self-check ROM bytes, 64 user RAM bytes, 7 port I/O bytes, 2 timer registers. 2 A/D registers, and a miscellaneous register ; see figure 6 for the Address map. The user ROM has been split into three areas. The main user ROM area is from $080 to $OFF and from $7C0 to $F37. The last 8 user ROM locations at the bottom of memory are for the interrupt vectors.

The MCU reserves the first 16 memory locations for I/O features, of which 12 have been implemented.

These locations are used for the ports, the ports DDRs, the timer, the INT2 miscellaneous register, and the A/D. Of the 64 RAM bytes, 31 bytes are shared with the stack area. The stack must be used with care when data shares the stack area.

The shared stack area is used during the processing of an interrupt or subroutine calls to save the contents of the CPU state. The register contents are pushed onto the stack in the order shown in figure 7. Since the stack pointer decrements during pushes, the low order byte (PCL) of the program counter is stacked first, then the high order four bits (PCH) are stacked. This ensures that the program counter is loaded correctly during pulls from the stack since the stack pointer increments when it pulls data from the stack. A subroutine call results in only the program counter (PCL, PCH) contents being pushed onto the stack ; the remaining CPU registers are not pushed.

Figure 6 : EF6805R2 MCU Address Map.

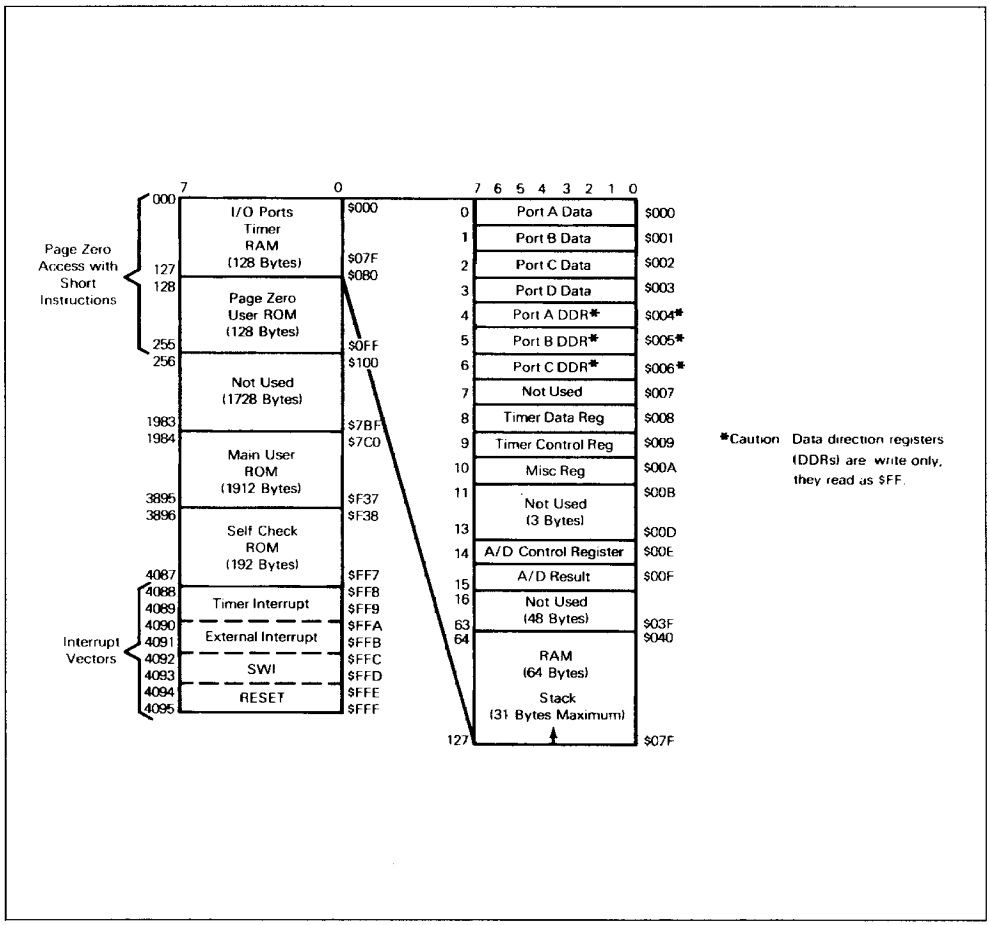
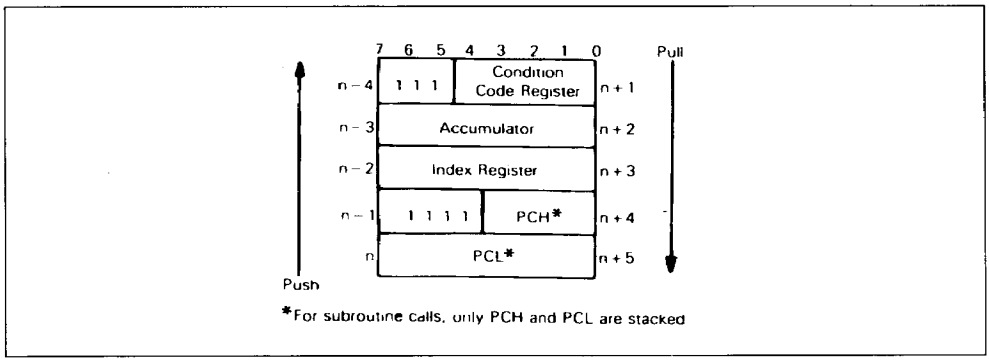


Figure 7 : Interrupt Stacking Order.



CENTRAL PROCESSING UNIT

The CPU of the EF6805 Family is implemented independently from the I/O or memory configuration. Consequently, it can be treated as an independent central processor communicating with I/O and memory via internal address, data, and control buses.

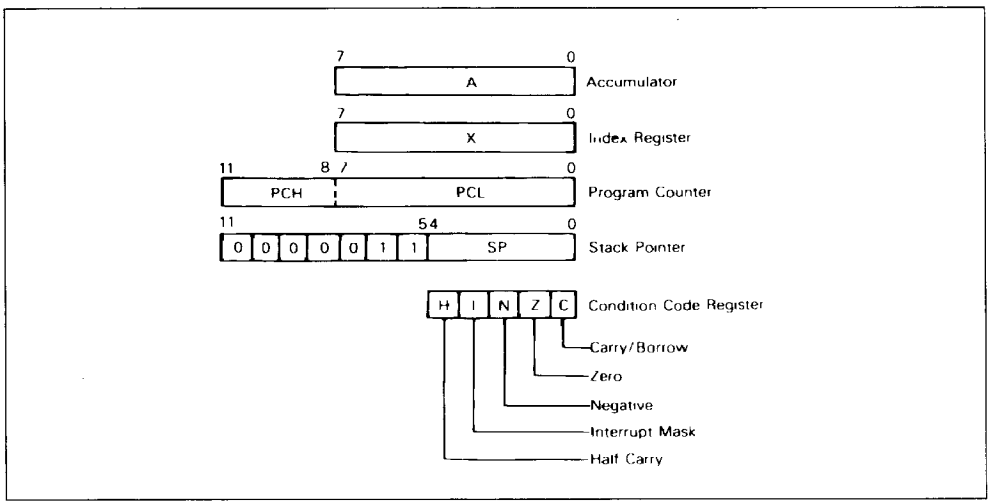
REGISTERS

The 6805 Family CPU has five registers available to the programmer. They are shown in figure 8 and are explained in the following paragraphs.

ACCUMULATOR (A) - The accumulator is a general purpose 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.

INDEX REGISTER (X) - The index register is an 8-bit register used for the indexed addressing mode. It contains an 8-bit value that may be added to an instruction value to create an effective address. The index register can also be used for data manipulations using the read-modify-write instructions. The Index Register may also be used as a temporary storage area.

Figure 8 : Programming Model.



PROGRAM COUNTER (PC) - The program counter is a 12-bit register that contains the address of the next instruction to be executed.

STACK POINTER (SP) - The stack pointer is a 12-bit register that contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $07F.

The stack pointer is then decremented as data is pushed onto the stack and incremented as data is then pulled from the stack. The seven most significant bits of the stack pointer are permanently set to 0000011. Subroutines and interrupts may be nested down to location $061 (31 bytes maximum) which allows the programmer to use up to 15 levels of subroutine calls (less if interrupts are allowed).

CONDITION CODE REGISTER (CC) - The condition code register is a 5-bit register in which four bits are used to indicate the results of the instruction just executed. These bits can be individually tested by a program and specific action taken as a result of their state. Each bit is explained in the following paragraphs.

Half Carry (H) - Set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I) - When this bit is set, the timer and external interrupt ($\overline{INT}$ and $\overline{INT2}$) are masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and is processed as soon as the interrupt bit is cleared.

Negative (N) - When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative (bit 7 in the result is a logical "1").

Zero (Z) - When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was zero.

Carry/Borrow (C) - When set, this bit indicates that a carry or borrow out of the Arithmetic Logic Unit (ALU) occurred during the last arithmetic operation. This bit is also affected during bit test and branch instructions plus shifts and rotates.

TIMER

The timer circuitry for the MC6805R2 is shown in figure 10. The 8-bit counter may be loaded under program control and is decremented toward zero by the clock input (or prescaler output). When the timer reaches zero, the timer interrupt request bit (bit 7) in the timer control register (TCR) is set. The timer interrupt can be masked (disabled) by setting the timer interrupt mask bit (bit 6) in the TCR. The interrupt bit (I bit) in the condition code register also prevents a timer interrupt from being processed. The MCU responds to this interrupt by saving the present CPU state on the stack, fetching the timer interrupt vector from locations $FF8 and $FF9 and executing the interrupt routine (see RESET, CLOCK, AND INTERRUPT STRUCTURE SECTIONS). *The timer interrupt request bit must be cleared by software. The TIMER and INT2 share the same interrupt vector. The interrupt routine must check the request bits to determine the source of the interrupt.*

The clock input to the timer can be from an external source (decrementing of timer counter occurs on a positive transition of the external source) applied to the TIMER input pin, or it can be the internal phase two signal. Three machine cycles are required for a change in state of the TIMER pin to decrement the timer prescaler. The maximum frequency of a signal that can be recognized by the TIMER pin logic is dependent on the parameter labeled t_{WH}. The pin logic that recognizes the high state on the pin must also recognize the low state on the pin in order to "re-arm" the internal logic. Therefore, the period can be calculated as follows (assumes 50/50 duty cycle for a given period) :

$$t_{cyc} \times 2 + 250ns = period = \frac{1}{freq}$$

The period is not simply $t_{WL} + t_{WH}$. This computation is allowable, but it does reduce the maximum allowable frequency by defining an unnecessarily longer period (250 nanoseconds times two).

When the phase two signal is used as the source, it can be gated by an input applied to the TIMER input pin allowing the user to easily perform pulse-width measurements. The source of the clock input is one of the mask options that is specified before manufacture of the MCU.

NOTE

For ungated phase two clock input to the timer prescaler, the TIMER pin should be tied to V_{CC}.

A prescaler option, divide by 2^n, can be applied to the clock input that extends the timing interval up to a maximum of 128 counts before decrementing the counter. This prescaling mask option is also specified before manufacture. To avoid truncation errors, the prescaler is cleared when bit 3 of the timer control register is written to a logic one (this bit always reads a logic zero). See figure 9.

Figure 9 : Timer Register (TCR).

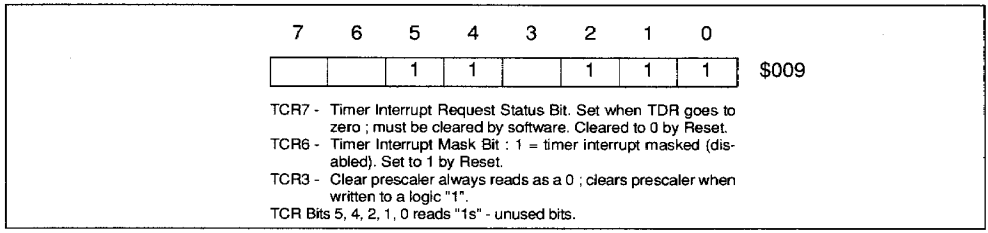
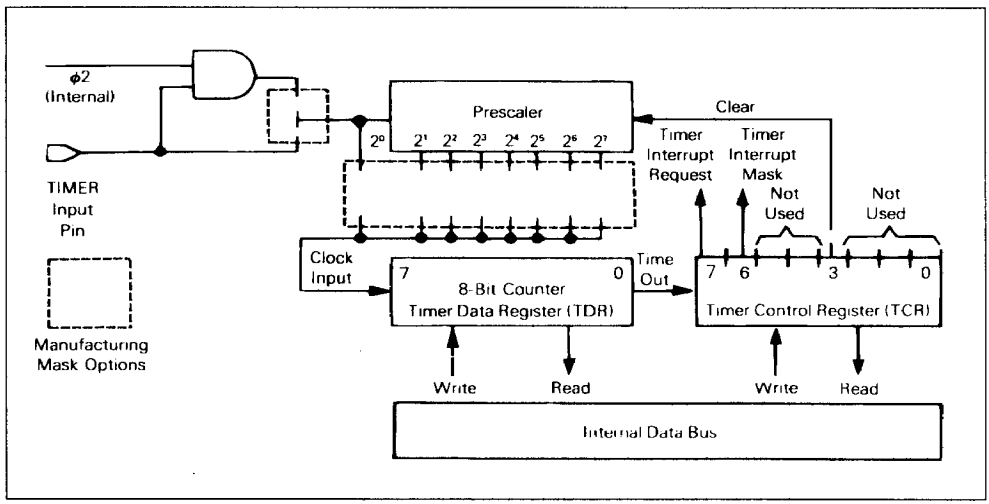


Figure 10 : Timer Block Diagram.



The timer continues to count past zero, falling through to $FF from $00 and then continuing the countdown. Thus, the counter can be read at any time by reading the timer data register (TDR). This allows a program to determine the length of time since a timer interrupt has occurred, and not disturb the counting process.

At power up or reset, the prescaler and counter are initialized with all logic ones ; the timer interrupt request bit (bit 7) is cleared and the timer interrupt mask bit (bit 6) is set.

SELF-CHECK

The self-check capability of the EF6805R2 MCU provides an internal check to determine if the part is functional. Connect the MCU as shown in figure 11 and monitor the output of Port C bit 3 for an oscillation of approximately 7Hz. A 10-volt level (through a 10k resistor) on the timer input, pin 8 and pressing then releasing the RESET button, energizes the ROM-based self-check feature. The self-check program exercises the RAM, ROM, TIMER, A/D, interrupts, and I/O ports.

Several of the self-check subroutines can be called by a user program with a JSR or BSR instruction. They are the RAM, ROM, and 4-channel A/D tests. The timer routine may also be called if the timer input is the internal φ2 clock.

To call those subroutines in customer applications, please contact your local SGS THOMSON sales office in order to obtain the complete description of the self-check program and the entrance/exit conditions.

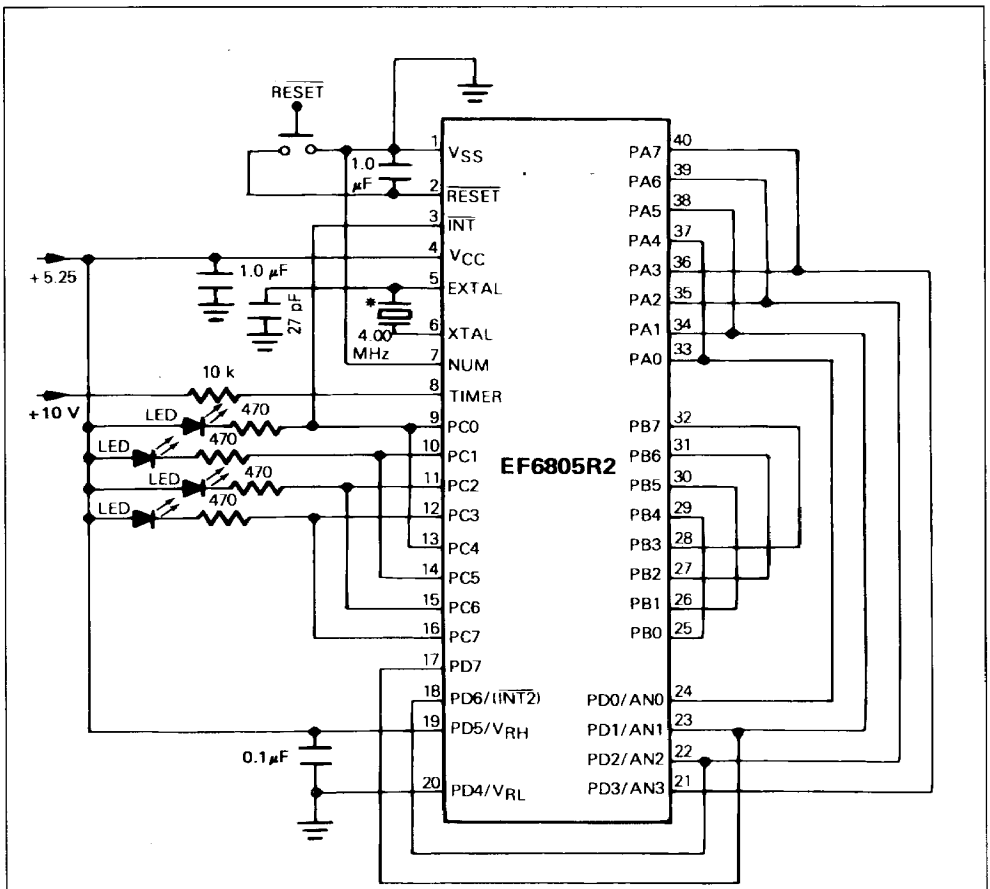
RAM SELF-CHECK SUBROUTINE - The RAM self-check is called at location $F6F and returns with the Z bit clear if any error is detected ; otherwise the Z bit is set. The walking diagnostic pattern method is used on the EF6805R2.

The RAM test must be called with the stack pointer at $07F. When run, the test checks every RAM cell except for $07F and $07E which are assumed to contain the return address.

The A and X registers and all RAM locations except $07F and $07E are modified.

ROM CHECKSUM SUBROUTINE - The ROM self-check is called at location $F8A. If any error is detected, it returns with the Z bit cleared ; otherwise Z = 1, X = 0 on return, and A is zero if the test passes. RAM location $040 to $043 is overwritten. The checksum is the complement of the execution OR of the contents of the user ROM.

Figure 11 : Self–Check Connections.



* This connection on clock oscillator user selectable mask option. Use jumper if the RC mask option is selected.

LED MEANINGS

PC0	PC1	PC2	PC3	Remarks [1 : LED ON ; 0 : LED OFF]
1	0	1	0	Bad I/O
0	0	1	0	Bad Timer
1	1	0	0	Bad RAM
0	1	0	0	Bad ROM
1	0	0	0	Bad A/D
0	0	0	0	Bad Interrupts or Request Flag
Any Flashing				Good Device

Anything else bad Device. Bad Port C, etc.

ANALOG-TO-DIGITAL CONVERTER SELF-CHECK - The A/D self-check is called at location $FA4 and returns with the Z bit cleared if any error was found, otherwise Z = 1.

The A and X register contents are lost. The X register must be set to 4 before the call. On return, X = 8 and A/D channel 7 is selected. The A/D test uses the internal voltage references and confirms port connections.

TIMER SELF-CHECK SUBROUTINE - The timer self-check is called at location $FCF and returns with the Z bit cleared if any error was found ; otherwise Z = 1.

In order to work correctly as a user subroutine, the internal 2 clock must be the clocking source and interrupts must be disabled. Also, on exit, the clock is running and the interrupt mask is not set so the caller must protect from interrupts if necessary.

The A and X register contents are lost. The timer self-check routine counts how many times the clock counts in 128 cycles. The number of counts should be a power of 2 since the prescaler is a power of 2. If not, the timer is probably not counting correctly. The routine also detects a timer which is not running.

RESET

The MCU can be reset three ways : by initial power-up, by the external reset input (RESET) and by an optional internal low-voltage detect circuit. The RESET input consists mainly of a Schmitt trigger which senses the RESET line logic level. A typical reset Schmitt trigger hysteresis curve is shown in figure 12. The Schmitt trigger provides an internal reset voltage if it senses a logical zero on the RESET pin.

Power-On Reset (POR) - An internal reset is generated upon powerup that allows the internal clock generator to stabilize. A delay of t_{RHL} milliseconds is required before allowing the RESET input to go high. Refer to the power and reset timing diagram of figure 13. Connecting a capacitor to the RESET input (as illustrated in figure 14) typically provides sufficient delay. During powerup, the Schmitt trigger switches on (removes reset) when RESET rises to V_{IRES+}.

Figure 12 : Typical Reset Schmitt Trigger Hysteresis.

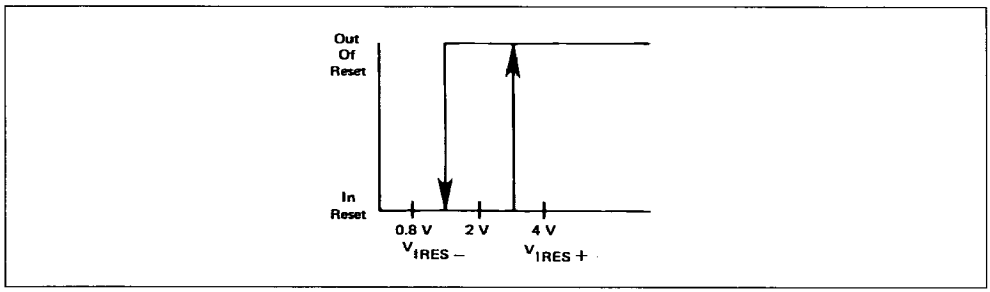


Figure 13 : Power and Reset Timing.

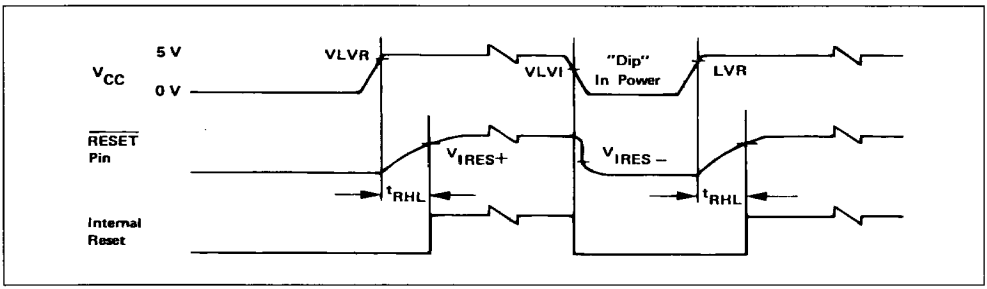
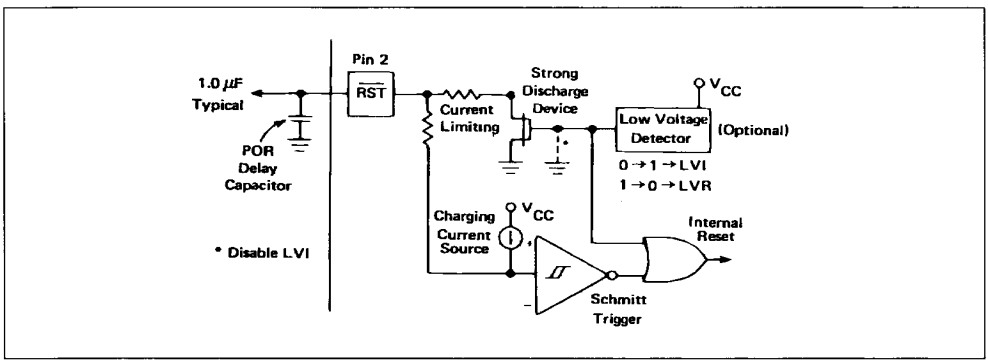


Figure 14 : RESET Configuration.



External Reset Input - The MCU will be reset if a logical zero is applied to the RESET input for a period longer than one machine cycle (t_{cyc}). Under this type of reset, the Schmitt trigger switches off at V_{IRES-} to provide an internal reset voltage.

Low-Voltage Inhibit (LVI) - The optional low-voltage detection circuit causes a reset of the MCU if the power supply voltage falls below a certain level (V_{LVI}). The only requirement is that V_{CC} remains at or below the V_{LVI} threshold for one t_{cyc} minimum. In typical applications, the V_{CC} bus filter capacitor will eliminate negative-going voltage glitches of less than one t_{cyc}. The output from the low-voltage detector is connected directly to the internal reset circuitry. It also forces the RESET pin low via a strong discharge device through a resistor. The internal reset will be removed once the power supply voltage rises above a recovery level (V_{LVR}), at which time a normal power-on-reset occurs.

INTERNAL CLOCK GENERATOR OPTIONS

The internal clock generator circuit is designed to require a minimum of external components. A crystal, a resistor, a jumper wire, or an external signal may be used to generate a system clock with various stability/cost tradeoffs. The oscillator frequency is internally divided by four to produce the internal system clocks. A manufacturing mask option is used to select crystal or resistor operation.

The different connection methods are shown in figure 15. Crystal specifications and suggested PC board layouts are given in figure 16. A resistor selection graph is given in figure 17.

The crystal oscillator start-up time is a function of many variables : crystal parameters (especially R_S), oscillator load capacitances, IC parameters, ambient temperature, and supply voltage. To ensure rapid oscillator start up, neither the crystal characteristics nor the load capacitances should exceed recommendations.

When utilizing the on-board oscillator, the MCU should remain in a reset condition (reset pin voltage below V_{IRES+}) until the oscillator has stabilized at its operating frequency. Several factors are involved in calculating the external reset capacitor required to satisfy this condition : the oscillator start-up voltage,

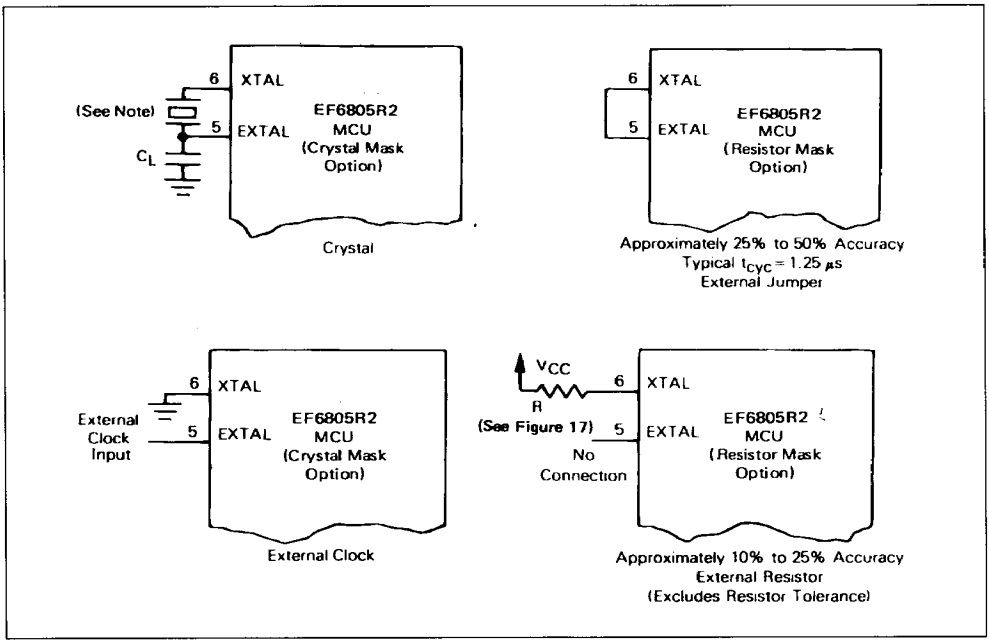
the oscillator stabilization time, the minimum V_{IRES+}, and the reset charging current specification.

Once V_{CC} minimum is reached, the external $\overline{RESET}$ capacitor will begin to charge at a rate dependent on the capacitor value. The charging current is supplied from V_{CC} through a large resistor, so it appears almost like a constant current source until the reset voltage rises above V_{IRES+}. Therefore, the $\overline{RESET}$ pin will charge at approximately :

$$(V_{IRES+}) \cdot C_{ext} = I_{RES} \cdot t_{RHL}$$

Assuming the external capacitor is initially discharged.

Figure 15 : Clock Generator Options.



Note : The recommended C_L value with a 4.0MHz crystal is 27pF, maximum, including system distributed capacitance. There is an internal capacitance of approximately 25pF on the XTAL pin. For crystal frequencies other than 4MHz, the total capacitance on each pin should be scaled as the inverse of the frequency ratio. For example, with a 2MHz crystal, use approximately 50pF on EXTAL and approximately 25pF on XTAL. The exact value depends on the Motional-Arm parameters of the crystal used.

Figure 16 : Crystal Monotial Arm Parameters and Suggested PC Board Layout.

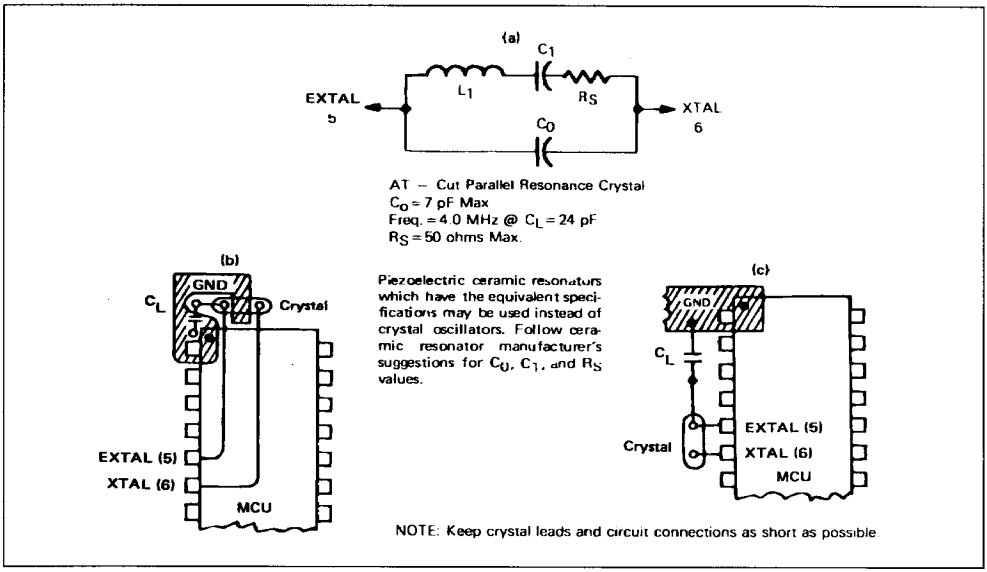
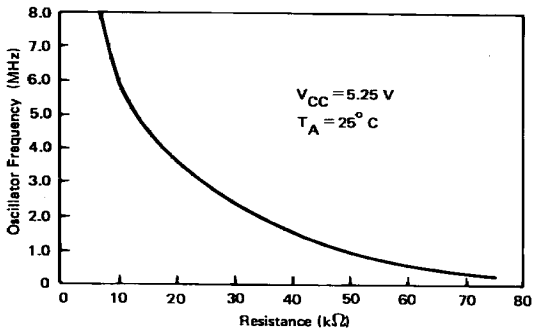


Figure 17 : Typical Frequency Selection for Resistor (oscillator option).



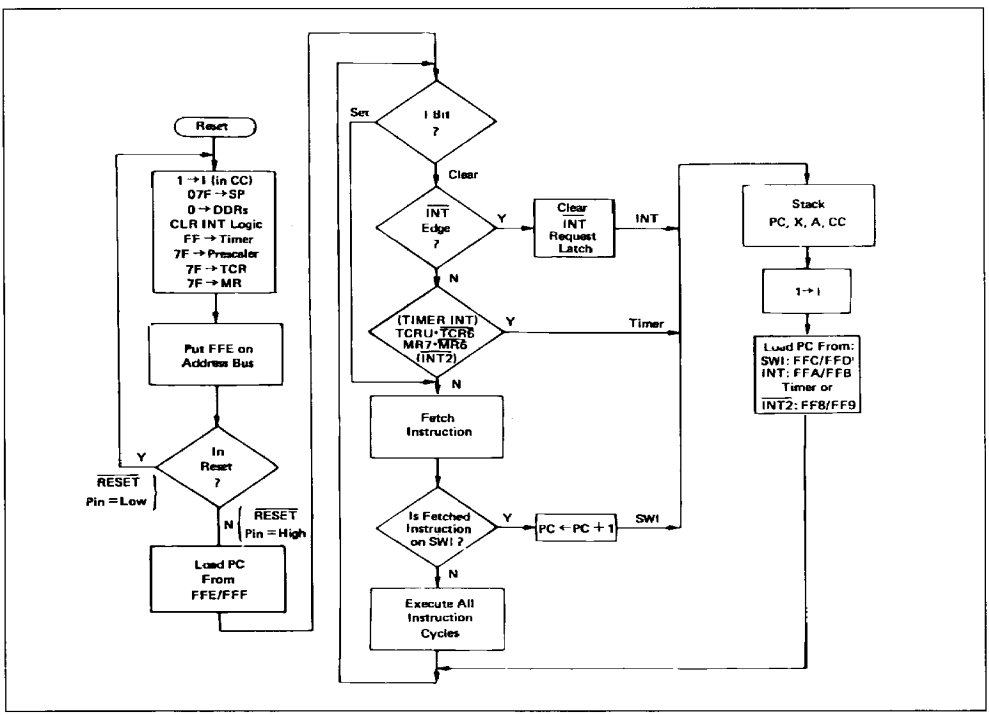
INTERRUPTS

The microcomputers can be interrupted four different ways : through the external interrupt (INT) input pin, the internal timer interrupt request, the external port D bit 6 (INT2) input pin, or the software interrupt instruction (SWI). When any interrupt occurs : the current instruction (including SWI) is completed, processing is suspended, the present CPU state is pushed onto the stack, the interrupt bit (I) in the condition code register is set, the address of the interrupt routine is obtained from the appropriate interrupt vector address, and the interrupt routine is executed. Stacking the CPU register, setting the I bit, and vector fetching require a total of 11 t_{cyc} periods for completion. A flowchart of the interrupt sequence is shown in figure 18. The interrupt service routine must end with a return from interrupt (RTI) instruction which allows the MCU to resume processing of the program prior to the interrupt (by unstacking the previous CPU state). Unlike RESET, hardware interrupts do not cause the current instruction execution to be halted, but are considered pending until the current instruction execution is complete.

When the current instruction is complete, the processor checks all pending hardware interrupts and if unmasked, proceedswith interrupt processing ; otherwise the next instruction is fetched and executed. Note that masked interrupts are latched for later interrupt service.

If both an external interrupt and a timer interupt are pending at the end of an instruction execution, the external interrupt is serviced first. The SWI is executed as any other instruction.

Figure 18 : Reset and Interrupt Processing Flowchard.



NOTE

The timer and $\overline{INT2}$ interrupts share the same vector address. The interrupt routine must determine the source by examining the interrupt request bits (TCR b7 and MR b7). Both TCR b7 and MR b7 can only be written to zero by software.

The external interrupt, $\overline{INT}$ and $\overline{INT2}$, are synchronized and then latched on the falling edge of the input signal. The $\overline{INT2}$ interrupt has an interrupt request bit (bit 7) and a mask bit (bit 6) located in the miscellaneous register (MR). The $\overline{INT2}$ interrupt is inhibited when the mask bit is set. The $\overline{INT2}$ is always read as a digital input on port D. The $\overline{INT2}$ and timer interrupt request bits, if set, cause the MCU to process an interrupt when the condition code I bit is clear.

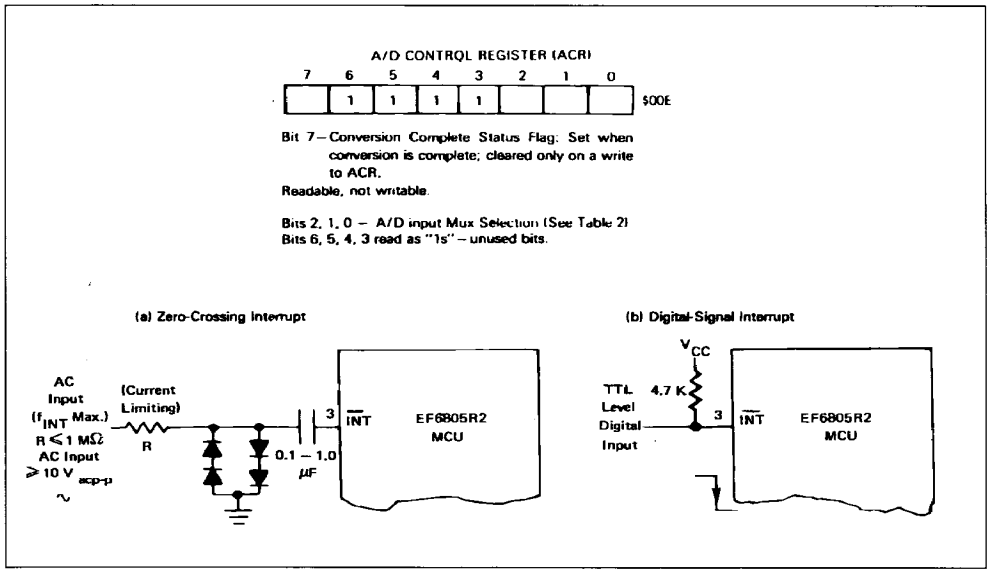
A sinusoidal input signal (f_{INT} maximum) can be used to generate an external interrupt for use as a zero-crossing detector. This allows applications such as servicing time-of-day routines and engaging/disengaging ac power control devices. Off-chip full wave rectification provides an interrupt at every zero crossing of the ac signal and thereby provides a 2f clock. See figure 19.

NOTE

The $\overline{INT}$ (pin 3) is internally biased at approximately 2.2V due to the internal zero-crossing detection.

A software interrupt (SWI) is an executable instruction which is executed regardless of the state of the I bit in the condition code register. SWIs are usually used as break-points for debugging or as systems calls.

Figure 19 : Typical Interrupt Circuits.



INPUT/OUTPUT CIRCUITRY

There are 32 input/output pins. The $\overline{INT}$ pin may be polled will branch instructions to provide an additional input pin. All pins on ports A, B, and C are programmable as either inputs or outputs under software control of the corresponding data direction register (DDR). See below I/O port control registers configuration. The port I/O programming is accomplished by writing the corresponding bit in the port DDR to a logic one for output or a logic zero for input. On reset all the DDRs are initialized to a logic zero state, placing the ports in the input mode. The port output registers are not initialized on reset and should be initialized by software before changing the DDRs from input to output. A read operation on a port programmed as an output will read the contents of the output latch regardless of the logic at the output pin, due to output loading. Refer to figure 20.

PORT DATA REGISTER

7 0

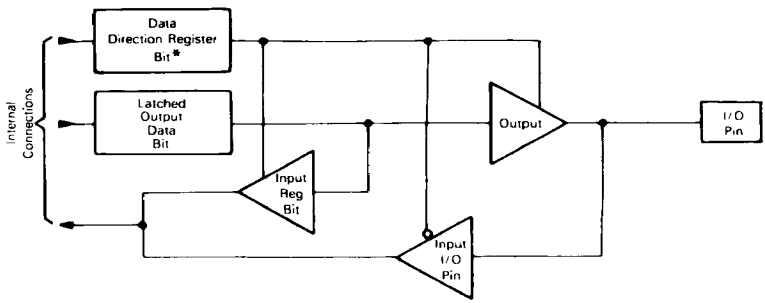
Port A Addr = $000
Port B Addr = $001
Port C Addr = $002
Port D Addr = $003

PORT DATA DIRECTION REGISTER (DDR)

7 0

(1) Write Only ; reads as all "1s"
(2) 1 = Output, 0 = Input Cleared to 0 by Reset
(3) Port A Addr = $004
Port B Addr = $005
Port C Addr = $006

Figure 20 : Typical Port I/O Circuitry.



Data Direction Register Bit	Latched Output Data Bit	Output State	Input to MCU
1	0	0	0
1	1	1	1
0	X	High-Z**	Pin

* DDR is a write-only register and reads as all "1s".
* Ports B, and C are three-state ports.
Port A has optional internal pullup devices to provide CMOS data drive capability. See Electrical Characteristics tables for complete information.

All input/output lines are TTL compatible as both inputs and outputs. Port A lines are CMOS compatible as outputs (mask option) while port B, C, and D lines are CMOS compatible as inputs. Port D lines are input only ; thus, there is no corresponding DDR. When programmed as outputs, port B is capable of sinking 10 milliamperes and sourcing 1 milliampere on each pin.

Port D provides the reference voltage, $\overline{INT2}$, and multiplexed analog inputs. All of these lines are shared with the port D digital inputs. Port D may always be used as digital inputs and may also be used as analog inputs providing V_{RH} and V_{RL} are connected to the appropriate reference voltages. The V_{RL} and V_{RH} lines (PD4 and PD5) are internally connected to the A/D resistor. Analog inputs may be prescaled to attain the V_{RL} and V_{RH} recommended input voltage range.

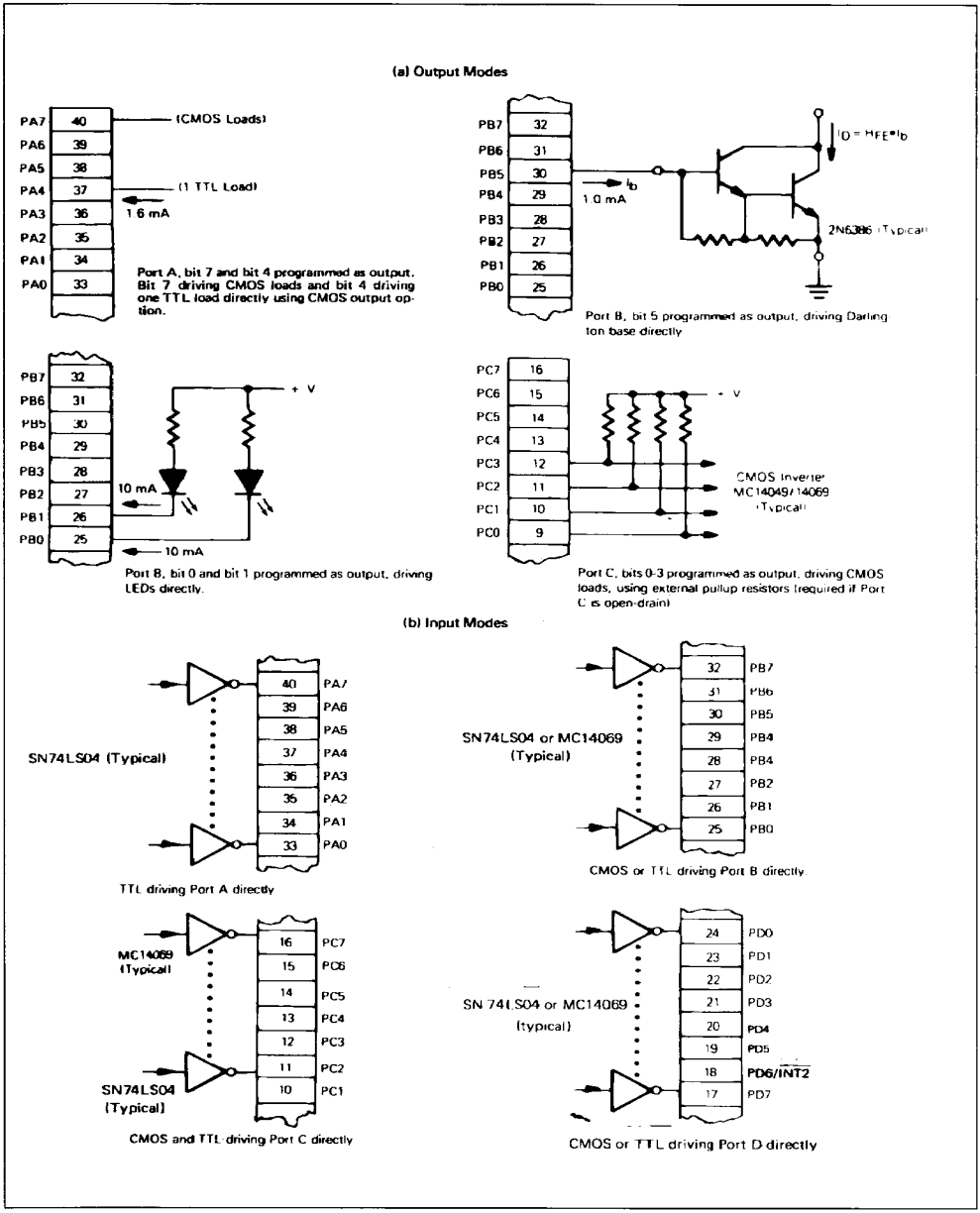
The address map (figure 6) gives the addresses of data registers and data direction registers. Figure 21 provides some examples of port connections.

CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be written using a single-store instruction.

The latched output data bit (see figure 20) must always be written. Therefore, any write to a port writes all of its data bits even though the port DDR is set to input. This may be used to initialize the data register and avoid undefined outputs ; however, care must be exercised when using read-modify-write instructions, since the data read corresponds to the pin level if the DDR is an input (zero) and corresponds to the latched output data when the DDR is an output (one).

Figure 21 : Typical Port Connections.



ANALOG-TO-DIGITAL CONVERTER

The EF6805R2 has an 8-bit analog-to-digital (A/D) converter implemented on the chip using a successive approximation technique, as shown in figure 22. Up to four external analog inputs, via port D, are connected to the A/D through a multiplexer. Four internal analog channels may be selected for calibration purposes (V_{RH}-V_{RL}, V_{RH}-$V_{RL}/2$, V_{RH}-$V_{RL}/4$, and V_{RL}). The accuracy of these internal channels will not necessarily meet the accuracy specifications of the external channels.

The multiplexer selection is controlled by the A/D control register (ACR) bits 0, 1, and 2 ; see table 1. This register is cleared during any reset condition.

Figure 22 : A/D Block Diagram.

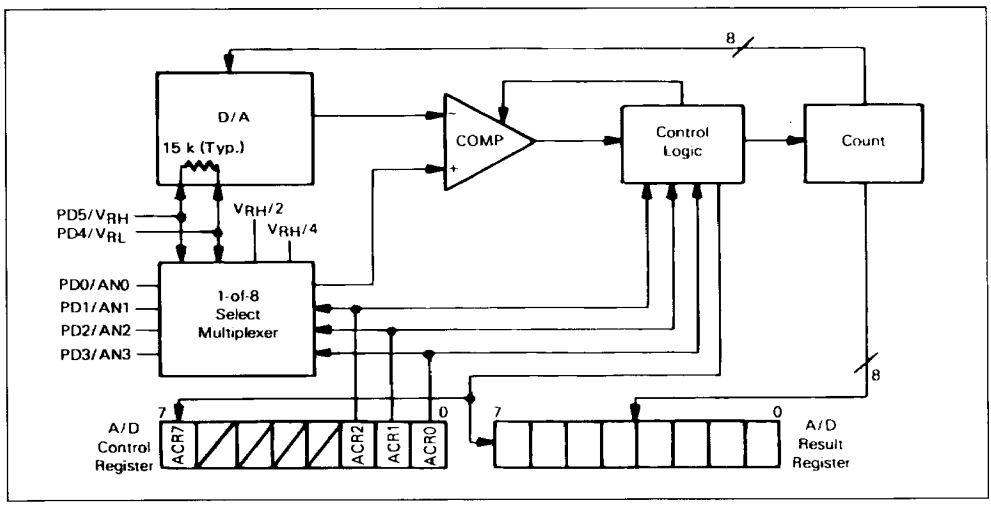


Table 1 : A/D Input Mux Selection.

A/D Control Register			Input Selected	A/D Output (hex)		
ACR2	ACR1	ACR0		Min.	Typ.	Max.
0	0	0	AN0			
0	0	1	AN1			
0	1	0	AN2			
0	1	1	AN3			
1	0	0	V_{RH}*	FE	FF	FF
1	0	1	V_{RL}*	00	00	01
1	1	0	$V_{RH/4}$*	3F	40	41
1	1	1	$V_{RH/2}$*	7F	80	81

* Internal (calibration) levels.

MISCELLANEOUS REGISTER (MR)

MR7 Bit 7 – $\overline{INT2}$ Interrupt Request Bit : Set when falling edge detected on $\overline{INT2}$ pin, must be cleared by software. Cleared to 0 by Reset.

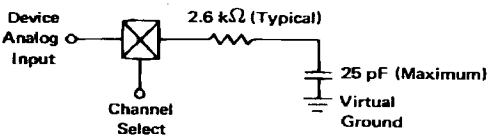
MR6 Bit 6 – $\overline{INT2}$ Interrupt Mask Bit : 1 = $\overline{INT2}$ Interrupt masked (disabled). Set to 1 by Reset.

MR Bits 5, 4, 3, 2, 1, 0 – Read as "1s" – unused bits.

A/D RESULT REGISTER (ARR)

Whenever the ACR is written, the conversion in progress is aborted, the conversion complete flag (ACR bit 7) is cleared, and the selected input is sampled for five machine cycles and held internally. During these five cycles, the analog input will appear approximately like a 25 picofarad (maximum) capacitor (plus approximately 10pF for packaging) charging through a 2.6 kiloohm resistor (typical). Refer to figure 23.

Figure 23 : Effective Analog Input Impedance (during sampling only).



The converter operates continuously using 30 machine cycles to complete a conversion of the sampled analog input. When the conversion is complete, the digitized sample of digital value is placed in the A/D result register (ARR), the conversion complete flag is set, the selected input is sampled again, and a new conversion is started.

The A/D is ratiometric. Two reference voltages (V_{RH} and V_{RL}) are supplied to the converter via port D pins. An input voltage equal to V_{RH} converts to $FF (full scale) and an input voltage equal to V_{RL} converts to $00. An input voltage greater than V_{RH} converts to SFF and no overflow indication is provided. Similarly, an input voltage less than V_{RL}, but greater than V_{SS} converts to $00. Maximum and minimum ratings must not be exceeded. For ratiometric conversion, the source of each analog input should use V_{RH} as the supply voltage and be referenced to V_{RL}. To maintain the full accuracy on the A/D, V_{RH} should be equal to or less than V_{DD}, V_{RL} should be equal to or greater than V_{SS} but less than the maximum specification and (V_{RH}-V_{RL}) should be equal to or greater than 4 volts.

The A/D has a built-in LSB offset intended to reduce the magnitude of the quantizing error to LSB, rather than + 0, - 1 LSB with no offset. This implies that, ignoring errors, the transition point from $00 to $01 occurs at LSB above V_{RL}. Similarly, the transition from $FE to $FF occurs 1 1/2 LSB below V_{RH}, ideally. Refer to figure 24 and 25.

On release of reset, the A/D control register (ACR) is cleared therefore after reset, channel zero will be selected and the conversion complete flag will be clear.

Figure 24 : Ideal Converter Transfer Characteristic.

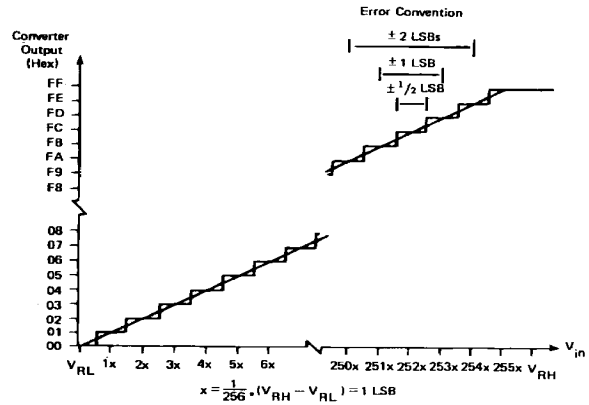
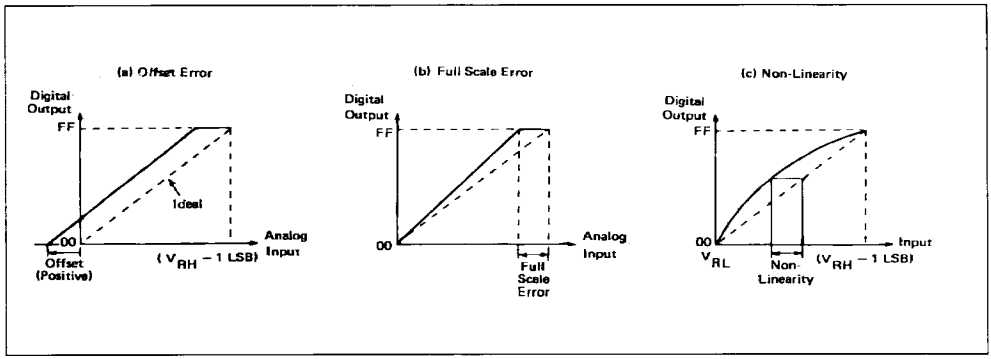


Figure 25 : Types of Conversion Errors.



BIT MANIPULATION

The EF6805R2 as the ability to set or clear any single RAM or I/O bit (except the data direction registers) with a single instruction (BSET, BCLR) (see Caution below). Any bit in page zero can be tested using the BRSET and BRCLR instructions and the program branches as a result of its state. The carry bit equals the value of the bit references by BRSET or BRCLR. The capability to working with any bit in RAM, ROM, or I/O allows the user to have individual flags in RAM or to handle single I/O bits as control lines.

CAUTION

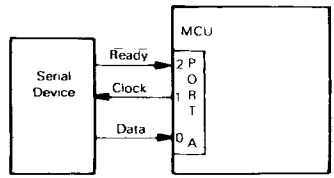
The corresponding data direction registers for ports A, B, and C are write-only registers locations $004, $005, and $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write functions, they cannot be used to set a data direction register bit (all "unaffected" bits would be set). It is recommended that all data direction register bits in a port be written using a single-store instruction.

The coding examples shown in figure 26 illustrate the usefulness of the bit manipulation and test instruction. Assume that the microcomputer is to communicate with an external serial device. The external device has a data ready signal, a data output line, and a clock line to clock data one bit at a time, least significant bit first out, of the device. The microcomputer waits until the data is ready, clocks the external device, picks up the data in the carry flag, clears the clock line, and finally accumulates the data bit in a random-access memory location.

Figure 26 : Bit Manipulation Example.

```
        BRSET   2, PORTA, *     WAIT FOR READY

        BSET    1, PORTA        CLOCK NEXT BIT IN
        BRCLR   0, PORTA, NEXT  PICKUP BIT IN C-BIT
NEXT    BCLR    1, PORTA        RETURN CLOCK LINE HIGH
        ASR     RAMLOC          MOVE C-BIT INTO RAM
```



ADDRESSING MODES

The EF6805R2 MCU has ten addressing modes available for use by the programmer. They are explained briefly in the following paragraphs. For additional details and graphical illustrations, refer to the EF6805 Family Users Manual.

The term "effective address" (EA) is used in describing the addressing modes. EA is defined as the address from which the argument for an instruction is fetched or stored.

IMMEDIATE - In the immediate addressing mode, the operand is contained in the byte immediately following the opcode. The immediate addressing mode is used to access constants which do not change during program execution (e.g., a constant used to initialize a loop counter).

DIRECT - In the direct addressing mode, the effective address of the argument is contained in a single byte following the opcode byte. Direct addressing allows the user to directly address the lowest 256 bytes in memory with a single 2-byte instruction. This address area includes all on-chip RAM and I/O registers and 128 bytes of ROM. Direct addressing is an effective use of both memory and time.

EXTENDED - In the extended addressing mode, the effective address of the argument is contained in the two bytes following the opcode. Instructions with extended addressing mode are capable of referencing arguments anywhere in memory with a single 3-byte instruction. When using the assembler, the user need not specify whether an instruction uses direct or extended addressing. The assembler automatically selects the shortest form of the instruction.

RELATIVE - The relative addressing mode is only used in branch instructions. In relative addressing, the contents of the 8-bit signed byte following the opcode (the offset) is added to the PC if, and only if, the branch condition is true. Otherwise, control proceeds to the next instruction. The span of relative addressing is from - 126 to + 129 from the opcode address. The programmer need not worry about calculating the correct offset if he uses the assembler, since it calculates the proper offset and checks to see if it is within the span of the branch.

INDEXED, NO OFFSET - In the indexed, no offset addressing mode, the effective address of the argument is contained in the 8-bit index register. Thus, this addressing mode can access the first 256 memory locations. These instructions are only one byte long. This mode is often used to move a pointer through a table or to hold the address of a frequently referenced RAM or I/O location.

INDEXED, 8-BIT OFFSET - In the indexed, 8-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the unsigned byte following the opcode. This addressing mode is useful in selecting the kth element in an n element table. With this 2-byte instruction, k would typically be in X with the address of the beginning of the table in the instruction. As such, tables may begin anywhere within the first 256 addressable locations and could extend as far as location 510 ($1FE is the last location at which the instruction may begin).

INDEXED, 16-BIT OFFSET - In the indexed, 16-bit offset addressing mode, the effective address is the sum of the contents of the unsigned 8-bit index register and the two unsigned bytes following the opcode. This addressing mode can be used in a manner similar to indexed, 8-bit offset except that this 3-byte instruction allows tables to be anywhere in memory. As with direct and extended, the assembler determines the shortest form of indexed addressing.

BIT SET/CLEAR - In the bit set/clear addressing mode, the bit to be set or cleared is part of the opcode, and the byte following the opcode specifies the direct address of the byte in which the specified bit is to be set or cleared. Thus, any read/write bit in the first 256 locations of memory, including I/O, can be selectively set or cleared with a single 2-byte instruction.

CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be must written using a single-store instruction.

BIT TEST AND BRANCH - The bit test and branch addressing mode is a combination of direct addressing and relative addressing. The bit which is to be tested and condition (set or clear) is included in the opcode, and the address of the byte immediately following the opcode byte. The signed relative 8-bit offset in the third byte is added to the PC if the specified bit is set or cleared in the specified memory location. This single 3-byte instruction allows the program to branch based on the condition of any readable bit in the first 256 locations of memory. The span of branching is from - 125 to + 130 from the opcode address. The state of the tested bit is also transferred to the carry bit of the condition code registers.

CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be must written using a single-store instruction.

INHERENT - In the inherent addressing mode, all the information necessary to execute the instruction is contained in the opcode. Operations specifying only the index register or accumulator, as well as control instructions with no other arguments, are included in this mode. These instructions are one byte long.

INSTRUCTION SET

The EF6805R2 MCU has a set of 59 basic instructions, which when combined with the 10 addressing modes produce 207 usable opcodes. They can be divided into five different types : register/memory, read-modify-write, branch, bit manipulation, and control. The following paragraphs briefly explain each type. All the instructions within a given type are presented in individual tables.

REGISTER/MEMORY INSTRUCTIONS - Most of these instructions use two operands. One operand is either the accumulator or the index register. The other operand is obtained from memory using one of the addressing modes. The jump unconditional (JMP) and jump to subroutine (JSR) instructions have no register operand. Refer to table 1.

READ-MODIFY-WRITE INSTRUCTIONS - These instructions read a memory location or a register, modify or test its contents, and write the modified value back to memory or to the register ; see Caution under Input/Output section. The test for negative or zero (TST) instruction is included in the read-modify-write instruction though it does not perform the write. Refer to table 2.

BRANCH INSTRUCTIONS - The branch instructions cause a branch from the program when a certain condition is met. Refer to table 3.

BIT MANIPULATION INSTRUCTIONS - The instructions are used on any bit in the first 256 bytes of the memory ; One group either sets or clears. The other group performs the bit test and branch operations. Refer to table 4.

CAUTION

The corresponding DDRs for ports A, B, and C are write-only registers (registers at $004, $005, $006). A read operation on these registers is undefined. Since BSET and BCLR are read-modify-write in function, they cannot be used to set or clear a single DDR bit (all "unaffected" bits would be set). It is recommended that all DDR bits in a port be must written using a single-store instruction.

CONTROL INSTRUCTION - The control instructions control the MCU operations during program execution. Refer to table 5.

ALPHABETICAL LISTING - The complete instruction set is given in alphabetical order in table 6.

OPCODE MAP - Table 8 is an opcode map for the instruction used on the MCU.

Table 1 : Register/memory Instructions.

Function	Mnemonic	Addressing Modes																			
		Immediate			Direct			Extended			Indexed (no offset)			Indexed (8 bit offset)			Indexed (16 bit offset)				
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles		
Load A from Memory	LDA	A6	2	2	B6	2	4	C6	3	5	F6	1	4	E6	2	5	D6	3	6		
Load X from Memory	LDX	AE	2	2	BE	2	4	CE	3	5	FE	1	4	EE	2	5	DE	3	6		
Store A in Memory	STA				B7	2	5	C7	3	6	F7	1	5	E7	2	6	D7	3	7		
Store X in Memory	STX				BF	2	5	CF	3	6	FF	1	5	EF	2	6	DF	3	7		
Add Memory to A	ADD	AB	2	2	BB	2	4	CB	3	5	FB	1	4	EB	2	5	DB	3	6		
Add Memory and Carry to A	ADC	A9	2	2	B9	2	4	C9	3	5	F9	1	4	E9	2	5	D9	3	6		
Subtract Memory	SUB	A0	2	2	B0	2	4	C0	3	5	F0	1	4	E0	2	5	D0	3	6		
Subtract Memory from A with Borrow	SBC	A2	2	2	B2	2	4	C2	3	5	F2	1	4	E2	2	5	D2	3	6		
AND Memory to A	AND	A4	2	2	B4	2	4	C4	3	5	F4	1	4	E4	2	5	D4	3	6		
OR Memory with A	ORA	AA	2	2	BA	2	4	CA	3	5	FA	1	4	EA	2	5	DA	3	6		
Exclusive OR Memory with A	EOR	A8	2	2	B8	2	4	C8	3	5	F8	1	4	E8	2	5	D8	3	6		
Arithmetic Compare A with Memory	CMP	A1	2	2	B1	2	4	C1	3	5	F1	1	4	E1	2	5	D1	3	6		
Arithmetic Compare X with Memory	CPX	A3	2	2	B3	2	4	C3	3	5	F3	1	4	E3	2	5	D3	3	6		
Bit Test Memory with A (logical compare)	BIT	A5	2	2	B5	2	4	C5	3	5	F5	1	4	E5	2	5	D5	3	6		
Jump Unconditional	JMP				BC	2	3	CC	3	4	FC	1	3	EC	2	4	DC	3	5		
Jump to Subroutine	JSR				BD	2	7	CD	3	8	FD	1	7	ED	2	8	DD	3	9		

Table 2 : Read- Modify-Write Instructions.

Function	Mnem	Addressing Modes															
		Inherent (A)			Inherent (X)			Direct			Indexed (no offset)			Indexed (8 bit offset)			
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Increment	INC	4C	1	4	5C	1	4	3C	2	6	7C	1	6	6C	2	7
Decrement	DEC	4A	1	4	5A	1	4	3A	2	6	7A	1	6	6A	2	7
Clear	CLR	4F	1	4	5F	1	4	3F	2	6	7F	1	6	6F	2	7
Complement	COM	43	1	4	53	1	4	33	2	6	73	1	6	63	2	7
Negate (2's complement)	NEG	40	1	4	50	1	4	30	2	6	70	1	6	60	2	7
Rotate Left Thru Carry	ROL	49	1	4	59	1	4	39	2	6	79	1	6	69	2	7
Rotate Right Thru Carry	ROR	46	1	4	56	1	4	36	2	6	76	1	6	66	2	7
Logical Shift Left	LSL	48	1	4	58	1	4	38	2	6	78	1	6	68	2	7
Logical Shift Right	LSR	44	1	4	54	1	4	34	2	6	74	1	6	64	2	7
Arithmetic Shift Right	ASR	47	1	4	57	1	4	37	2	6	77	1	6	67	2	7
Test for Negative or Zero	TST	4D	1	4	5D	1	4	3D	2	6	7D	1	6	6D	2	7

Table 3 : Branch Instructions.

Function	Mnemonic	Relative Addressing Mode		
		Op Code	# Bytes	# Cycles
Branch Always	BRA	20	2	4
Branch Never	BRN	21	2	4
Branch IFF Higher	BHI	22	2	4
Branch IFF Lower or Same	BLS	23	2	4
Branch IFF Carry Clear	BCC	24	2	4
Branch IFF Higher or Same	BHS	24	2	4
Branch IFF Carry Set	BCS	25	2	4
Branch IFF Lower	BLO	25	2	4
Branch IFF Not Equal	BNE	26	2	4
Branch IFF Equal	BEQ	27	2	4
Branch IFF Half Carry Clear	BHCC	28	2	4
Branch IFF Half Carry Set	BHCS	29	2	4
Branch IFF Plus	BPL	2A	2	4
Branch IFF Minus	BMI	2B	2	4
Branch IFF interrupt mask bit is clear.	BMC	2C	2	4
Branch IFF interrupt mask bit is set.	BMS	2D	2	4
Branch IFF interrupt line is low.	BIL	2E	2	4
Branch IFF interrupt line is high.	BIH	2F	2	4
Branch to Subroutine	BSR	AD	2	8

Table 4 : Bit Manipulation Instructions.

Function	Mnemonic	Addressing Modes					
		Bit Set/Clear			Bit Test and Branch		
		Op Code	# Bytes	# Cycles	Op Code	# Bytes	# Cycles
Branch IFF bit n is set.	BRSET n (n = 0...7)				2 • n	3	10
Branch IFF bit n is clear.	BRCLR n (n = 0...7)				01 + 2 • n	3	10
Set Bit n	BSET n (n = 0...7)	11 + 2 • n	2	7			
Clear Bit n	BCLR n (n = 0...7)	11 + 2 • n	2	7			

Table 5 : Control Instructions.

		Inherent		
Function	**Mnemonic**	**Op Code**	**# Bytes**	**# Cycles**
Transfer A to X	TAX	97	1	2
Transfer X to A	TXA	9F	1	2
Set Carry Bit	SEC	99	1	2
Clear Carry Bit	CLC	98	1	2
Set Interrupt Mask Bit	SEI	9B	1	2
Clear Interrupt Mask Bit	CLI	9A	1	2
Software Interrupt	SWI	83	1	11
Return from Subroutine	RTS	81	1	6
Return from Interrupt	RTI	80	1	9
Reset Stack Pointer	RSP	9C	1	2
No-operation	NOP	9D	1	2

Table 6 : Instruction Set.

	Addressing Modes										Condition Code				
Mnem	Inherent	Immediate	Direct	Extended	Relative	Indexed (no offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/Clear	Bit Test & Branch	H	I	N	Z	C
ADC		X	X	X		X	X	X			^	●	^	^	^
ADD		X	X	X		X	X	X			^	●	^	^	^
AND		X	X	X		X	X	X			●	●	^	^	●
ASL	X		X			X	X				●	●	^	^	^
ASR	X		X			X	X				●	●	^	^	^
BCC					X						●	●	●	●	●
BCLR									X		●	●	●	●	●
BCS					X						●	●	●	●	●
BEQ					X						●	●	●	●	●
BHCC					X						●	●	●	●	●
BHCS					X						●	●	●	●	●
BHI					X						●	●	●	●	●
BHS					X						●	●	●	●	●
BIH					X						●	●	●	●	●
BIL					X						●	●	●	●	●
BIT		X	X	X		X	X	X			●	●	^	^	●
BLO					X						●	●	●	●	●
BLS					X						●	●	●	●	●
BMC					X						●	●	●	●	●
BMI					X						●	●	●	●	●
BMS					X						●	●	●	●	●
BNE					X						●	●	●	●	●
BPL					X						●	●	●	●	●
BRA					X						●	●	●	●	●
BRN					X						●	●	●	●	●
BRCLR										X	●	●	●	●	^
BRSET										X	●	●	●	●	^
BSET									X		●	●	●	●	●
BSR					X						●	●	●	●	●
CLL	X										●	●	●	●	0

Condition Code Symbols :

H Half Carry (from bit 3)
I Interrupt Mask
N Negative (sign bit)
Z Zero
C Carry/borrow
^ Test and Set if True, Cleared Otherwise
· Not Affected

Table 6 : Instruction Set (continued).

	Addressing Modes										Condition Code				
Mnem	Inherent	Immediate	Direct	Extended	Relative	Indexed (no offset)	Indexed (8 Bits)	Indexed (16 Bits)	Bit Set/clear	Bit Test & Branch	H	I	N	Z	C
CLI	X										●	0	●	●	●
CLR	X		X			X	X				●	●	0	1	●
CMP		X	X	X		X	X	X			●	●	^	^	^
COM	X		X			X	X				●	●	^	^	1
CPX		X	X	X		X	X	X			●	●	^	^	^
DEC	X		X			X	X				●	●	^	^	●
EOR		X	X	X		X	X	X			●	●	^	^	●
INC	X		X			X	X				●	●	^	^	●
JMP			X	X		X	X	X			●	●	●	●	●
JSR			X	X		X	X	X			●	●	●	●	●
LDA		X	X	X		X	X	X			●	●	^	^	●
LDX		X	X	X		X	X	X			●	●	^	^	●
LSL	X		X			X	X				●	●	^	^	^
LSR	X		X			X	X				●	●	0	^	^
NEQ	X		X			X	X				●	●	^	^	^
NOP	X										●	●	●	●	●
ORA		X	X	X		X	X	X			●	●	^	^	●
ROL	X		X			X	X				●	●	^	^	^
RSP	X										●	●	●	●	●
RTI	X										?	?	?	?	?
RTS	X										●	●	●	●	●
SBC		X	X	X		X	X	X			●	●	^	^	^
SEC	X										●	●	●	●	1
SEI	X										●	1	●	●	●
STA			X	X		X	X	X			●	●	^	^	●
STX			X	X		X	X	X			●	●	^	^	●
SUB		X	X	X		X	X	X			●	●	^	^	^
SWI	X										●	1	●	●	●
TAX	X										●	●	●	●	●
TST	X		X			X	X				●	●	^	^	●
TXA	X										●	●	●	●	●

Condition Code Symbols :

H Half Carry (from bit 3)
I Interrupt Mask
N Negative (sign bit)
Z Zero
C Carry/borrow
^ Test and Set if True, Cleared Otherwise
• Not Affected
? Load CC Register from Stack

EF6805 HMOS FAMILY

Features	EF6805P2	EF6805P6	EF6805R2	EF6805R3	EF6805U2	EF6805U3
Technology	HMOS	HMOS	HMOS	HMOS	HMOS	HMOS
Number of Pins	28	28	40	40	40	40
On-chip RAM (bytes)	64	64	64	112	64	112
On-chip User ROM (bytes)	1100	1796	2048	3776	2048	3776
External Bus	None	None	None	None	None	None
Bidirectional I/O Lines	20	20	24	24	24	24
Unidirectional I/O Lines	None	None	6 Inputs	6 Inputs	8 Inputs	8 Inputs
Other I/O Features	Timer	Timer	Timer, A/D	Timer, A/D	Timer	Timer
External Interrupt Inputs	1	1	2	2	2	2
STOP and WAIT	No	No	No	No	No	No

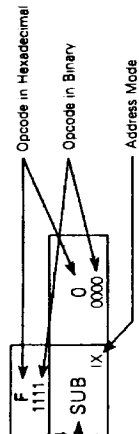
Table 7 : 6805 HMOS Family Instruction Set Opcode Map.

	Bit Manipulation		Branch		Read-Modify-Write				Control			Register / Memory								
	BTB	BSC	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX				
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F				
HI / Low	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111				
0 0000	0 BRSET0 3 BTB	BSET0 2 BSC	BRA 2 REL	NEG 6 DIR	NEG 4 INH	NEG 4 INH	NEG 7 IX1	NEG 6 IX	RTI 1 INH		SUB 2 IMM	SUB 3 DIR	SUB 4 EXT	SUB 5 IX2	SUB 4 IX1	SUB 3 IX				0 0000
1 0001	0 BRCLR0 3 BTB	BCLR0 2 BSC	BRN 2 REL							6 RTS 1 INH	CMP 2 IMM	CMP 4 DIR	CMP 5 EXT	CMP 6 IX2	CMP 5 IX1	CMP 4 IX				1 0001
2 0010	0 BRSET1 3 BTB	BSET1 2 BSC	BHI 2 REL								SBC 2 IMM	SBC 4 DIR	SBC 5 EXT	SBC 6 IX2	SBC 5 IX1	SBC 4 IX				2 0010
3 0011	0 BRCLR1 3 BTB	BCLR1 2 BSC	BLS 2 REL	COM 6 DIR	COMA 4 INH	COMX 4 INH	COM 7 IX1	COM 6 IX	SWI 11 INH		CPX 2 IMM	CPX 4 DIR	CPX 5 EXT	CPX 6 IX2	CPX 5 IX1	CPX 4 IX				3 0011
4 0100	0 BRSET2 3 BTB	BSET2 2 BSC	BCC 2 REL	LSR 6 DIR	LSRA 4 INH	LSRX 4 INH	LSR 7 IX1	LSR 6 IX			AND 2 IMM	AND 4 DIR	AND 5 EXT	AND 6 IX2	AND 5 IX1	AND 4 IX				4 0100
5 0101	0 BRCLR2 3 BTB	BCLR2 2 BSC	BCS 2 REL								BIT 2 IMM	BIT 4 DIR	BIT 5 EXT	BIT 6 IX2	BIT 5 IX1	BIT 4 IX				5 0101
6 0110	0 BRSET3 3 BTB	BSET3 2 BSC	BNE 2 REL	ROR 6 DIR	RORA 4 INH	RORX 4 INH	ROR 7 IX1	ROR 6 IX			LDA 2 IMM	LDA 4 DIR	LDA 5 EXT	LDA 6 IX2	LDA 5 IX1	LDA 4 IX				6 0110
7 0111	0 BRCLR3 3 BTB	BCLR3 2 BSC	BEQ 2 REL	ASR 6 DIR	ASRA 4 INH	ASRX 4 INH	ASR 7 IX1	ASR 6 IX	TAX 2 INH			STA 4 DIR	STA 5 EXT	STA 6 IX2	STA 5 IX1	STA 4 IX				7 0111
8 1000	0 BRSET4 3 BTB	BSET4 2 BSC	BHCC 2 REL	LSL 6 DIR	LSLA 4 INH	LSLX 4 INH	LSL 7 IX1	LSL 6 IX	CLC 2 INH		EOR 2 IMM	EOR 4 DIR	EOR 5 EXT	EOR 6 IX2	EOR 5 IX1	EOR 4 IX				8 1000
9 1001	0 BRCLR4 3 BTB	BCLR4 2 BSC	BHCS 2 REL	ROL 6 DIR	ROLA 4 INH	ROLX 4 INH	ROL 7 IX1	ROL 6 IX	SEC 2 INH		ADC 2 IMM	ADC 4 DIR	ADC 5 EXT	ADC 6 IX2	ADC 5 IX1	ADC 4 IX				9 1001
A 1010	0 BRSET5 3 BTB	BSET5 2 BSC	BPL 2 REL	DEC 6 DIR	DECA 4 INH	DECX 4 INH	DEC 7 IX1	DEC 6 IX	CLI 2 INH		ORA 2 IMM	ORA 4 DIR	ORA 5 EXT	ORA 6 IX2	ORA 5 IX1	ORA 4 IX				A 1010
B 1011	0 BRCLR5 3 BTB	BCLR5 2 BSC	BMI 2 REL						SEI 2 INH		ADD 2 IMM	ADD 4 DIR	ADD 5 EXT	ADD 6 IX2	ADD 5 IX1	ADD 4 IX				B 1011
C 1100	0 BRSET6 3 BTB	BSET6 2 BSC	BMC 2 REL	INC 6 DIR	INCA 4 INH	INCX 4 INH	INC 7 IX1	INC 6 IX	RSP 2 INH			JMP 3 DIR	JMP 4 EXT	JMP 5 IX2	JMP 4 IX1	JMP 3 IX				C 1100
D 1101	0 BRCLR6 3 BTB	BCLR6 2 BSC	BMS 2 REL	TST 6 DIR	TSTA 4 INH	TSTX 4 INH	TST 7 IX1	TST 6 IX	NOP 2 INH	BSR 8 REL	JSR 2 IMM	JSR 4 DIR	JSR 5 EXT	JSR 6 IX2	JSR 5 IX1	JSR 4 IX				D 1101
E 1110	0 BRSET7 3 BTB	BSET7 2 BSC	BIL 2 REL								LDX 2 IMM	LDX 4 DIR	LDX 5 EXT	LDX 6 IX2	LDX 5 IX1	LDX 4 IX				E 1110
F 1111	0 BRCLR7 3 BTB	BCLR7 2 BSC	BIH 2 REL	CLR 6 DIR	CLRA 4 INH	CLRX 4 INH	CLR 7 IX1	CLR 6 IX	TXA 2 INH			STX 4 DIR	STX 5 EXT	STX 6 IX2	STX 5 IX1	STX 4 IX				F 1111
Low																				Low

Abbreviations for Address Modes

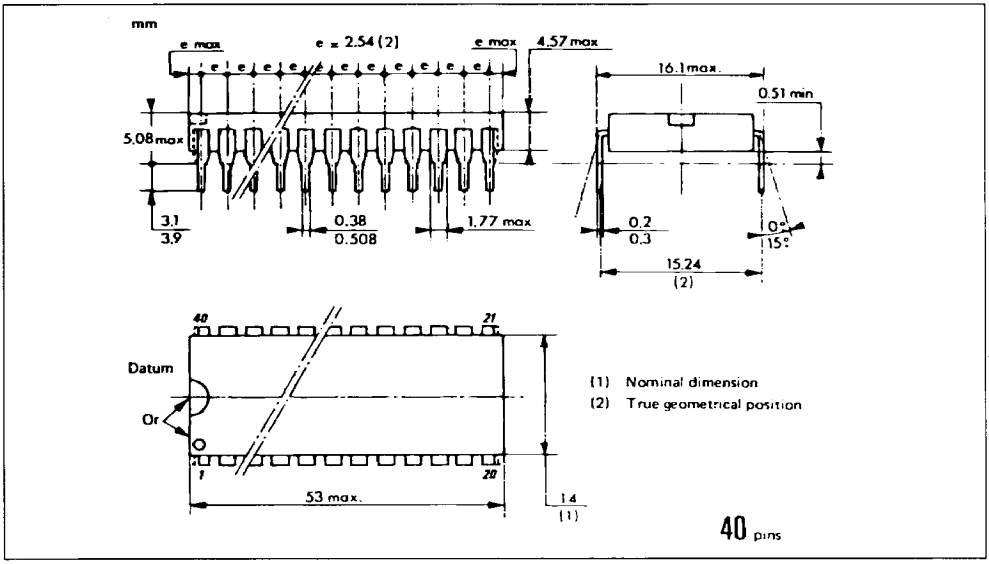
INH	Inherent
IMM	Immediate
DIR	Direct
EXT	Extended
REL	Relative
BSC	Bit Set/Clear
BTB	Bit Test and Branch
IX	Indexed (No Offset)
IX1	Indexed, 1 Byte (8-Bit) Offset
IX2	Indexed, 2 Byte (16-Bit) Offset

LEGEND

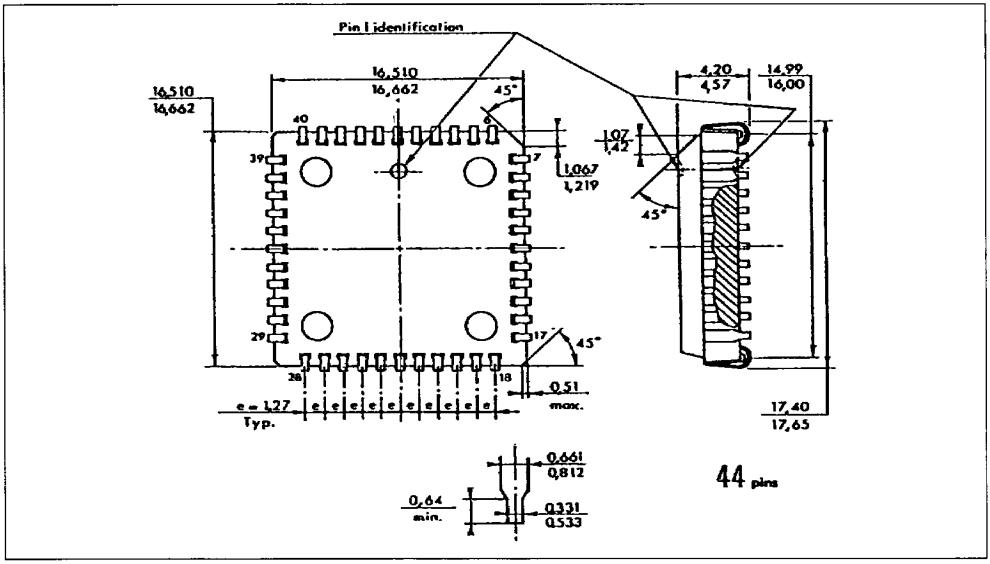


PACKAGE MECHANICAL DATA

P SUFFIX – PLASTIC PACKAGE



FN SUFFIX – PLCC44



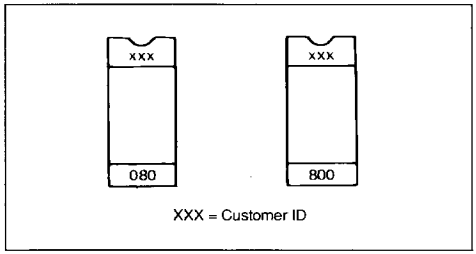
ORDERING INFORMATION

The information required when ordering a custom MCU is listed below. The ROM program may be transmitted to SGS–THOMSON on EPROM(s) or an EFDOS/MDOS* disk file.

To initiate a ROM pattern for the MCU, it is necessary to first contact your local SGS THOMSON representative or distributor.

EPROMs

Two 2716 or one 2732 type EPROMs, programmed with the customer program (positive logic sense for address and data), may be submitted for pattern generation. The EPROM must be clearly marked to indicate which EPROM corresponds to which address space. The recommended marking procedure is illustrated below :



After the EPROM(s) are marked, they should be placed in conductive IC carriers and securely packed. Do not use styrofoam.

VERIFICATION MEDIA

All original pattern media (EPROMs or floppy disk) are filled for contractual purposes and are not returned. A computer listing of the ROM code will be generated and returned along with a listing verification form. The listing should be thoroughly checked and the verification form completed, signed, and returned to SGS THOMSON. The signed verification form constitutes the contractual agreement for creation of the customer mask. If desired, SGS–THOMSON will program on blank EPROM from the data file used to create the custom mask and aid in the verification process.

ROM VERIFICATION UNITS (RVUs)

Ten MCUs containing the customer's ROM pattern will be sent for program verification. These units will have been made using the custom mask but are for the purpose of ROM verification only. For expediency they are usually unmarked, packaged in ceramic, and tested only at room temperature and 5 volts. These RVUs are included in the mask charge and are not production parts. The RVUs are thus not guaranteed by SGS–THOMSON. Quality Assurance, and should be discarded after verification is completed.

FLEXIBLE DISKS

The disk media submitted must be single-sided, EFDOS/MDOS* compatible floppies.

The customer must write the binary file name and company name on the disk with a felt-tip-pen. The minimum EFDOS/MDOS* system files, as well as the absolute binary object file (Filename .LO type of file) from the 6805 cross assembler, must be on the disk. An object file made from a memory dump using the ROLLOUT command is also acceptable. Consider submitting a source listing as well as the following files : filename .LX (DEVICE/EXORciser loadable format) and filename .SA (ASCII Source Code). These files will of course be kept confidential and are used 1) to speed up the process in-house if any problems arise, and 2) to speed up the user-to-factory interface if the user finds any software errors and needs assistance quickly from SGS–THOMSON factory representatives.

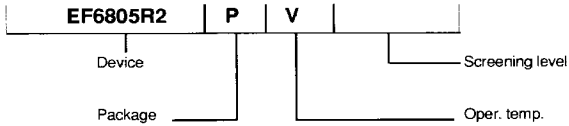
EFDOS is SGS THOMSON' Disk Operating System available on development systems such as DEVICE...

MDOS* is MOTOROLA's Disk Operating System available on development systems such as EXORciser, ...

* Requires prior factory approval.

Whenever ordering a custom MCU is required, please contact your local SGS THOMSON representative or SGS THOMSON distributor and/or complete and send the attached "MCU customer ordering sheet" to your local SGS THOMSON representative.

ORDER CODES



The table below horizontally shows all available suffix combinations for package, operating and screening level. Other possibilities on request.

Device	Package					Oper. Temp			ScreeningLevel			
	C	J	P	E	FN	L*	V	T	Std	D	G/B	B/B
EF6805R2			●		●	●	●	●	●	●		
Examples: EF6805R2P, EF6805R2FN, EF6805R2PV, EF6805R2FNV.												

Package : C : Ceramic DIL, **J :** Cerdip DIL, **P :** Plastic DIL, **E :** LCCC, **FN :** PLCC.
Oper. temp. : L* : 0°C to +70°C, **V :** –40°C to +85°C, **T :** –40°C to +105°C, *** :** may be omitted.
Screening level : Std : (no-end suffix), **D :** NFC 96883 level D,
G/B : NFC 96883 level G, **B/B :** NFC 96883 level B and MIL-STD-883C level B.

EXORciser is a registered trademark of MOTOROLA Inc.

EF6805 FAMILY - MCU CUSTOMER ORDERING SHEET

Commercial reference : |_|_|_|_|_|_|_|_|_|_|

Customer's marking : |_|_|_|_|_|_|_|_|_|_|

Application : .....

.....

Customer name : .....
Company : .....
Address : .....
Phone : .....

Specification reference ;
- ❑ SGS-THOMSON Microelectronic reference
  .....
- ❑ Special customer data reference*
  .....

ROM capacity required : |_|_|_|_| bytes

Temperature range :
- ❑ 0°C / + 70°C
- ❑ – 25°C / + 70°C
- ❑ – 40°C / + 85°C

Quality level :
- ❑ STD
- ❑ D
- ❑ Other* (customer's quality specification ref.) :
  .....

Package
- ❑ Plastic
- ❑ PLCC

Software developped by :
- ❑ SGS-THOMSON Microelectronic application lab.
- ❑ External lab.
- ❑ Customer

PATTERN MEDIA (a listing may be supplied in addition for checking purpose) :
- ❑ EPROM Reference :
- ❑ EFDOS/MDOS* disk file
  - ❑ 8" floppy
  - ❑ 5" 1/4 floppy
- ❑ Other *

OPTION LIST

-Oscillator input
- ❑ Xtal
- ❑ RC

- Low voltage inhibit :
- ❑ Enabled
- ❑ Disabled

- Port A output drive :
- ❑ CMOS and TTL
- ❑ TTL only

- Port C output drive :
- ❑ TTL
- ❑ Open drain

- Timer clock source :
- ❑ Internal f2 clock
- ❑ Timer input pin

* Requires prior factory approval

Yearly quantity forecast

- start of production date :
- for a shipment period of :

CUSTOMER CONTACT NAME : DATE : SIGNATURE :