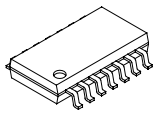
SONY

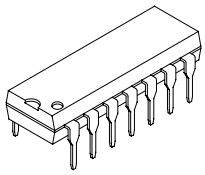
CXL5005M/P

CMOS-CCD 1H Delay Line for NTSC with PLL

CXL5005M
14 pin SOP (Plastic)



CXL5005P
14 pin DIP (Plastic)



Description

The CXL5005M/P are general-purpose CCD delay line ICs which provide 1H delay time of NTSC.

Features

- Low power consumption 90mW (Typ.)
- Small size package (14-pin SOP, DIP)
- Low differential gain DG = 3% (Typ.)
- Input signal ampiitude 180 IRE (= 1.28Vp-p, max.)
- Low input clock amplitude operation 200mVp-p (Min.)
- Built-in triple PLL circuit
- Built-in peripheral circuits (clock driver, timing generator, auto-bias and output circuits)

Functions

- 680-bit CCD register
- Clock drivers
- Autobias circuit
- Sync tip clamp circuit
- Sample-and-hold circuit
- PLL (triple)

Structure

CMOS-CCD

Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	V_{DD}	11	V
• Supply voltage	V_{CL}	6	V
• Operating temperature	Topr	–10 to +60	°C
• Storage temperature	Tstg	–55 to +150	°C
• Allowable power dissipation	P_D		
	CXL5005M	400	mW
	CXL5005P	800	mW

Recommended Operating Conditions

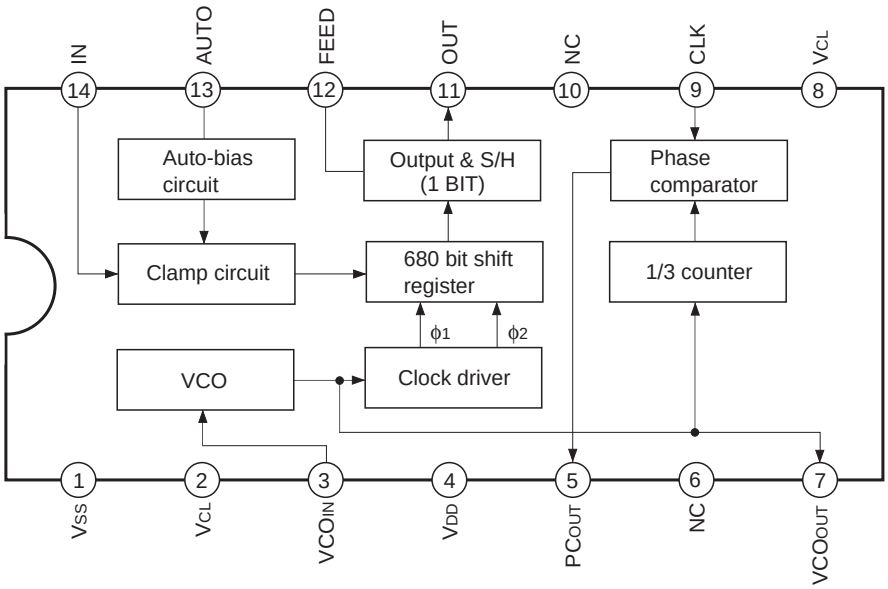
Supply voltage	V_{DD}	9 ± 5%	V
	V_{CL}	5 ± 5%	V

Recommended Clock Conditions

• Input clock amplitude	V_{CLK}	200mVp-p to 1.0Vp-p (300mVp-p typ.)
• Clock frequency	f_{CLK}	3.579545MHz

E88Z40A79-PS

Blook Diagram and Pin configuration



Pin Description

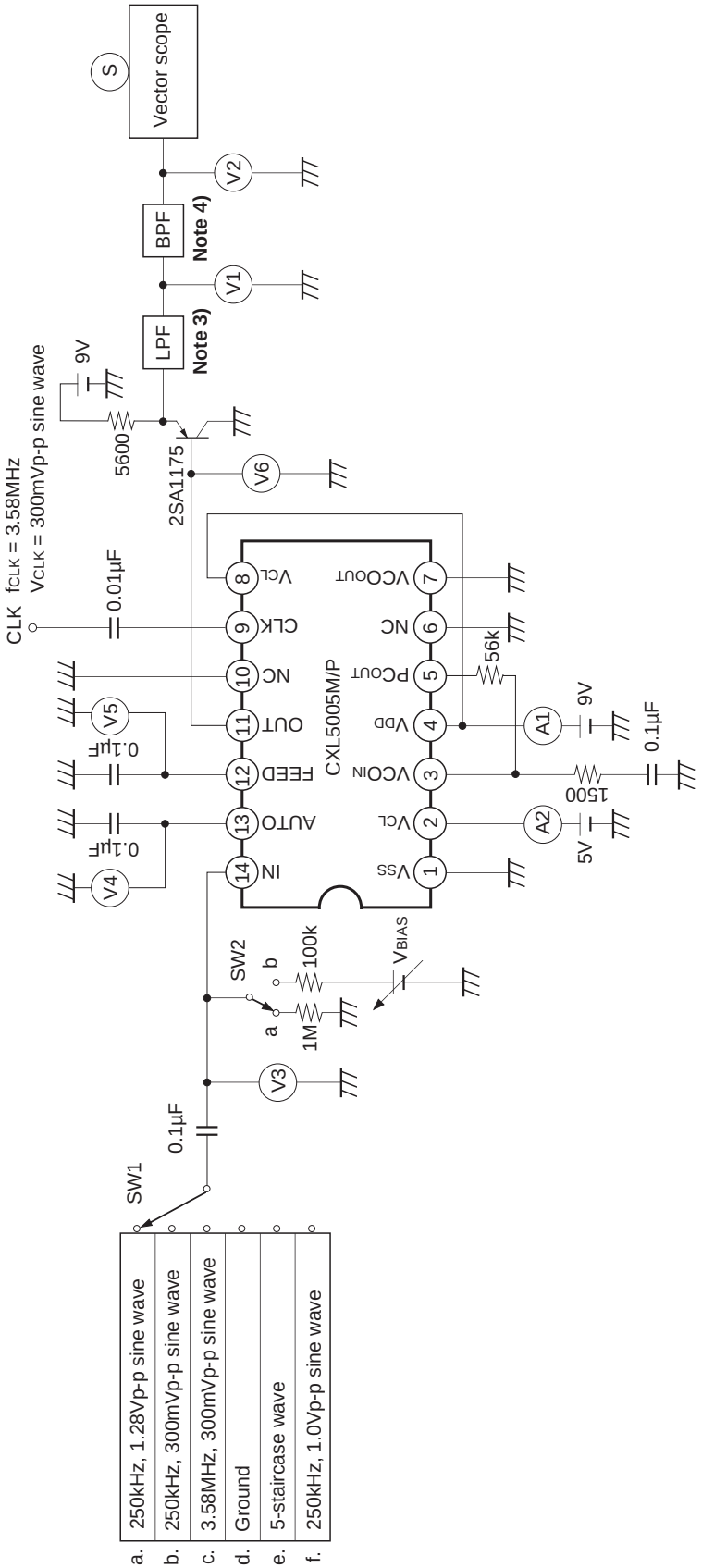
Pin No.	Symbol	Description	Impedance [Ω]
1	V_{SS}	GND	
2	V_{CL}	5V power supply	
3	VCO_{IN}	VCO input	> 100k
4	V_{DD}	9V power supply	
5	PC_{OUT}	Phase comparator output	≈ 5k
6	NC		
7	VCO_{OUT}	VCO output	≈ 5k
8	V_{CL}	5V power supply	
9	CLK	Clock input	≈ 5k
10	NC		
11	OUT	Signal output	600 to 1k
12	FEED	Feedback DC output	> 100k
13	AUTO	Autobias DC output	≈ 10k
14	IN	Signal input	> 100k

Electrical Characteristics

(Ta = 25°C, V_{DD} = 9.0V, V_{CL} = 5.0V, f_{CLK} = 3.58MHz, V_{CLK} = 300mVp-p sine wave, See "Electrical Characteristics Test Circuit")

Item	Symbol	Test condition	SW condition 1	SW condition 2	Measuring point	Min.	Typ.	Max.	Unit
Supply current	I_{DD}	250kHz, 1.28Vp-p, sine wave input	a	a	A1	—	4.0	5.0	mA
	I_{CL}				A2	—	9.0	12.0	mA
Insertion gain	IG	250kHz, 1.28Vp-p, sine wave input IG = 20 log (Output voltage [Vp-p] / 1.28 [Vp-p])	a	a	V1	–3.0	0.0	3.0	dB
Frequency response	fG	Dissipation at 3.58MHz in relation to 250kHz fG = 20 log ($V_{3.58MHz}$/ V_{250kHz}) **(Note 1)**	b, c	b	V1	–3.0	–2.1	—	dB
Differential gain	DG	5-staircase wave input Y = 140 IRE (= 1.0Vp-p) Measure with vector scope **(Note 2)**	e	a	S	—	3.0	5.0	%
Differential phase	DP					—	3.0	5.0	deg
Allowable input amplitude	V_{IN-AC}		—	—	—	—	—	1.28	Vp-p
Noise	S/N	S: Input = 250kHz, 1.0Vp-p output (Vp-p)	f	a	V2	55	60	—	dB
		N: Input = DC GND output (Vrms)	d	a					
DC output voltage	V_{IN-DC}		d	a	V3	3.5	5.0	6.5	V
	$V_{AUTO-DC}$				V4	3.5	5.0	6.5	V
	$V_{FEED-DC}$	250kHz, 1.28Vp-p, sine wave input	a	a	V5	1.3	2.3	3.3	V
	V_{OUT-DC}				V6	1.7	2.7	3.7	V

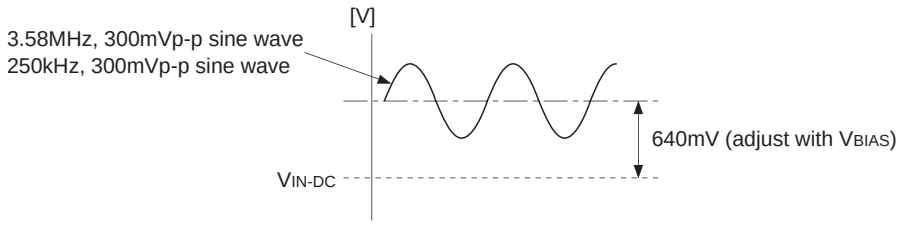
Electrical Characteristics Test Circuit



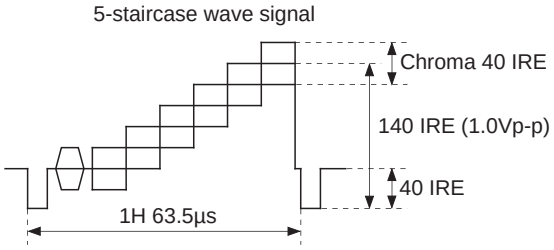
Note 1) Frequency response test condition

$V_{3.58MHz}$ (Output signal voltage [Vp-p] at 3.58MHz input)
V_{250kHz} (Output signal voltage [Vp-p] at 250kHz input)

Set Pin 14 (IN) voltage [V] = V_{IN-DC} + 640mV.

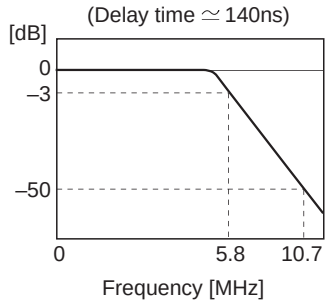


Note 2) Differential gain and differential phase test condition

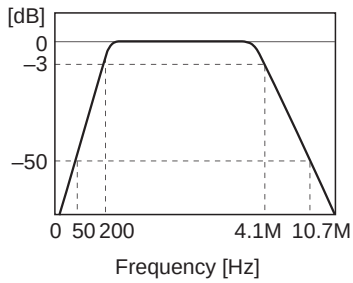


DG and DP are measured at output S point by vector scope.

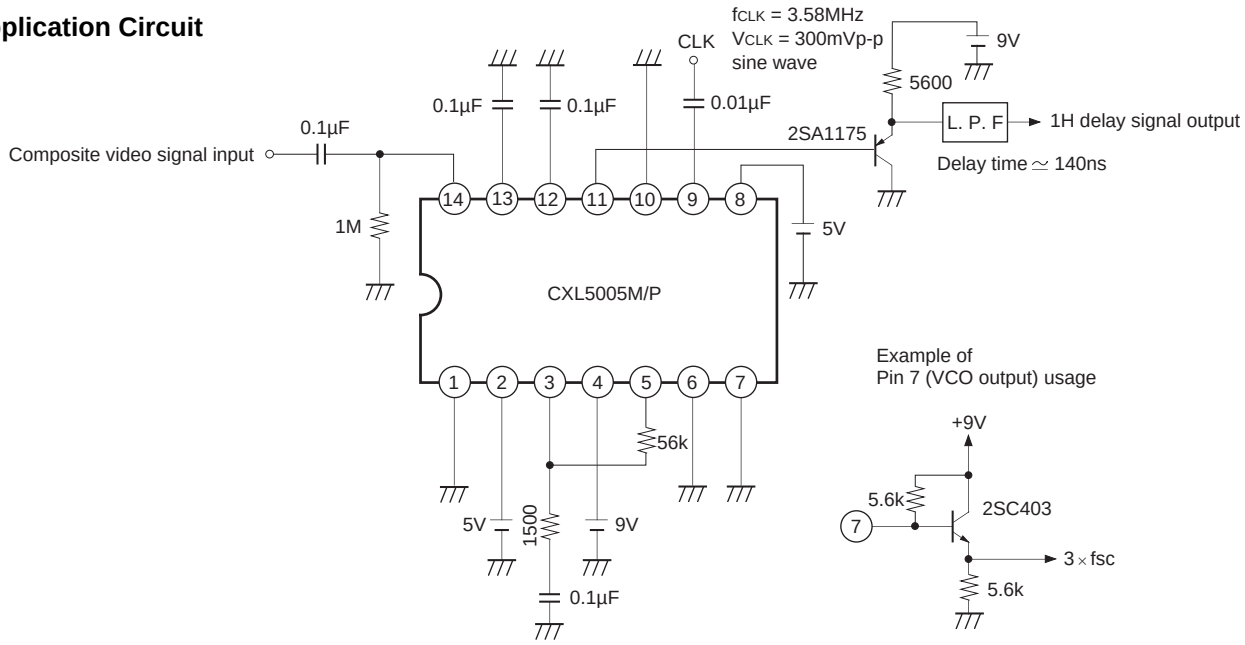
Note 3) LPF frequency response



Note 4) BPF frequency response



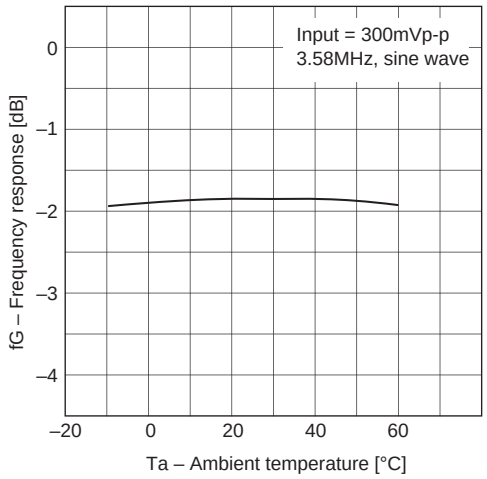
Application Circuit



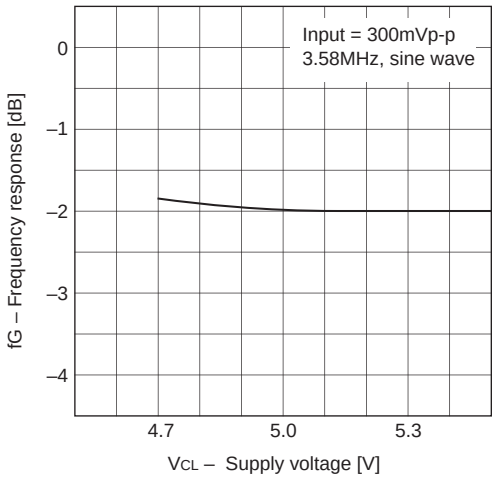
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

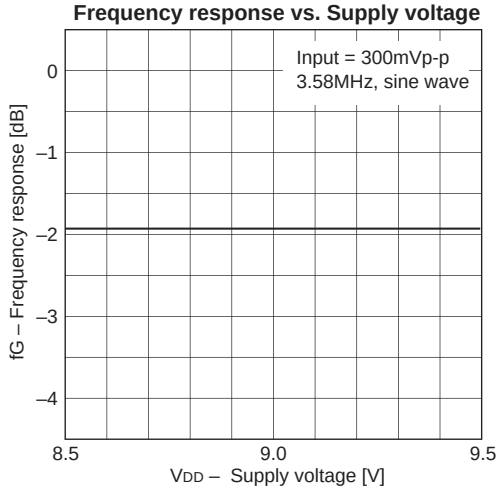
Frequency response vs. Ambient temperature



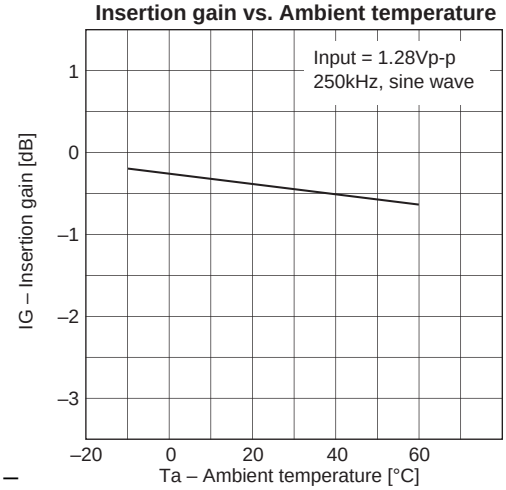
Frequency response vs. Supply voltage



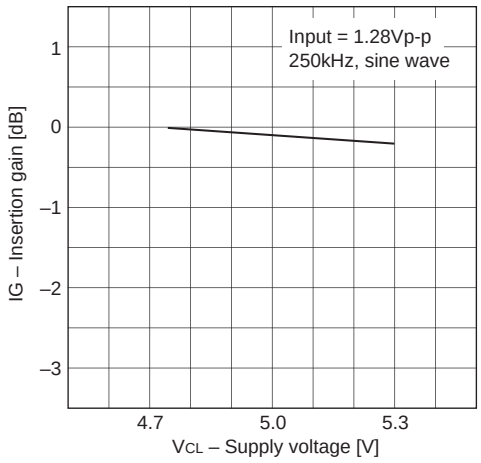
Frequency response vs. Supply voltage



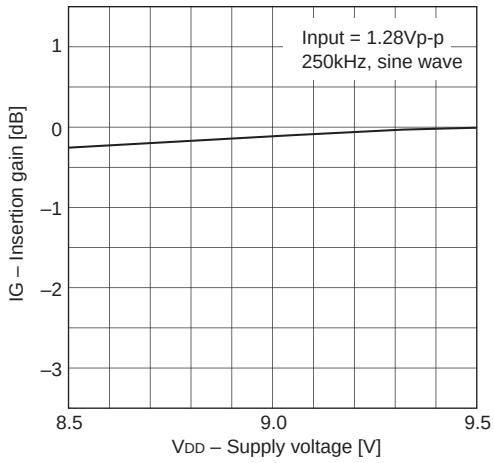
Insertion gain vs. Ambient temperature



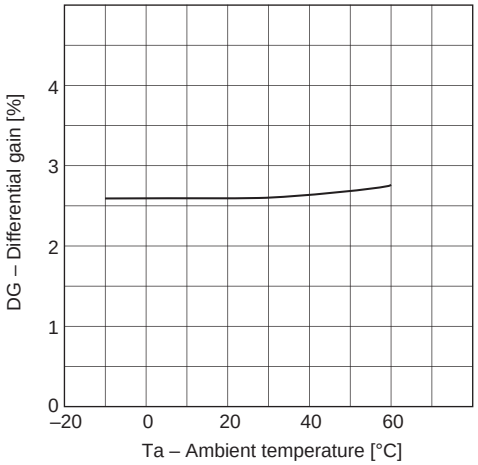
Insertion gain vs. Supply voltage



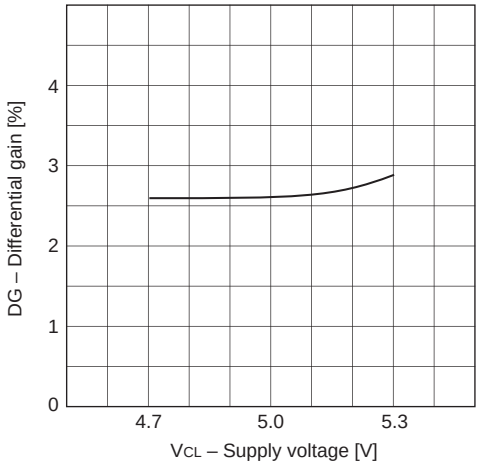
Insertion gain vs. Supply voltage



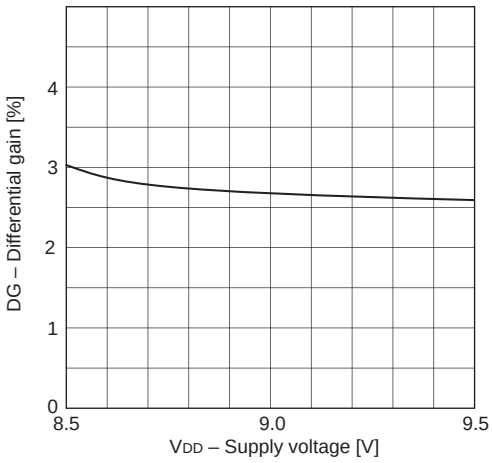
Differential gain vs. Ambient temperature



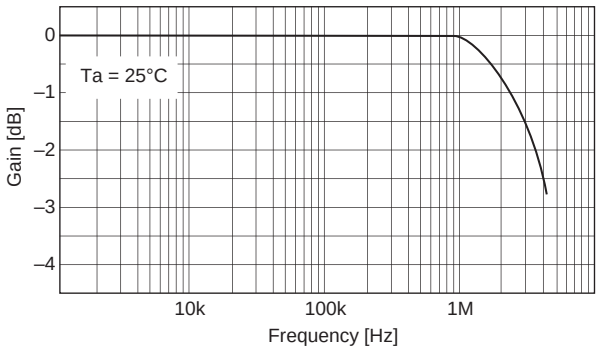
Differential gain vs. Supply voltage



Differential gain vs. Supply voltage



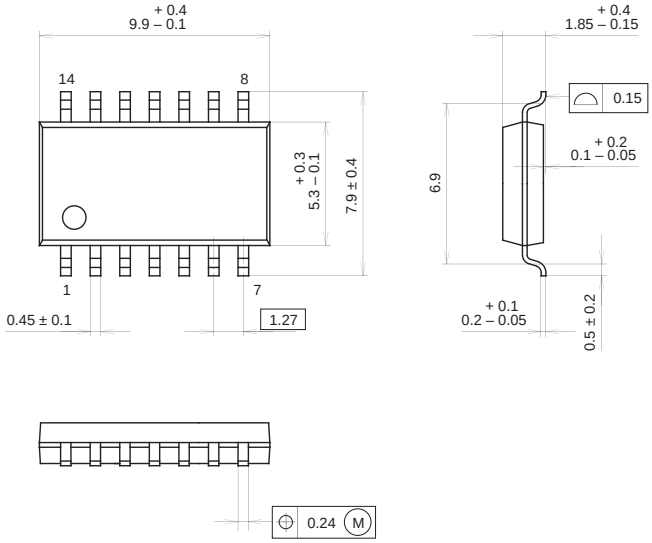
Frequency response



Package Outline Unit: mm

CXL5005M

14PIN SOP (PLASTIC)



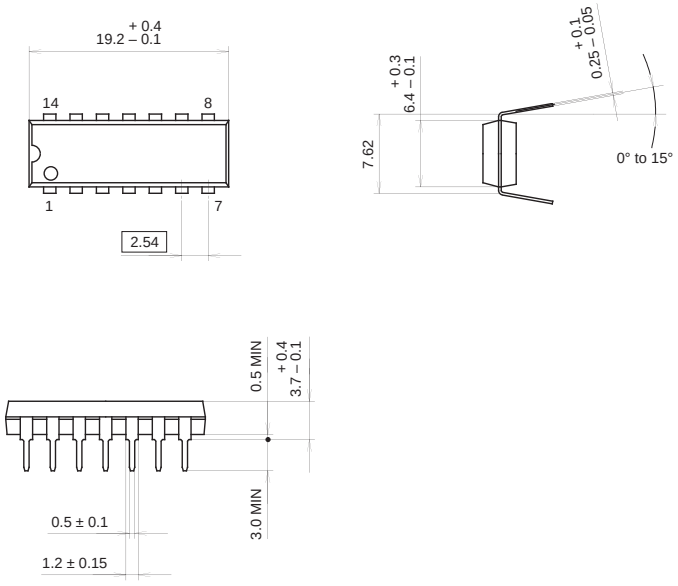
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.2g

SONY CODE	SOP-14P-L01
EIAJ CODE	SOP014-P-0300
JEDEC CODE	————

CXL5005P

14PIN DIP (PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.9g

SONY CODE	DIP-14P-01
EIAJ CODE	DIP014-P-0300
JEDEC CODE	Similar to MO-001-AH