普誠科技股份有限公司
Princeton Technology Corp.
Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT2257 is an Electronic Volume Controller IC utilizing CMOS Technology specially designed for the new generation of AV entertainment products. It has two (2) built-in channels making it ideally suitable for mono and stereo sound applications. PT2257 provides an I^2C Control Interface, an attenuation range of 0 to -79dB, low noise, and high channel separation. It is housed in an 8 pins, DIP or SOP Package, PT2257's pin assignments and application circuit are optimized for easy PCB layout and cost saving advantages.

FEATURES

- CMOS Technology
- Low Power Consumption
- Least External Components
- Attenuation Range: 0 to -79dB at 1dB/step
- Operating Voltage: 4 to 9V
- Low Noise, S/N Ratio>100dB (A-weighting)
- Two Channel Output
- Available in 8 pins, DIP or SOP

APPLICATIONS

- AV Surround Audio Equipment
- Car Audio
- Mini Compo
- Computer Multi-Media Speaker
- Other Audio Equipment

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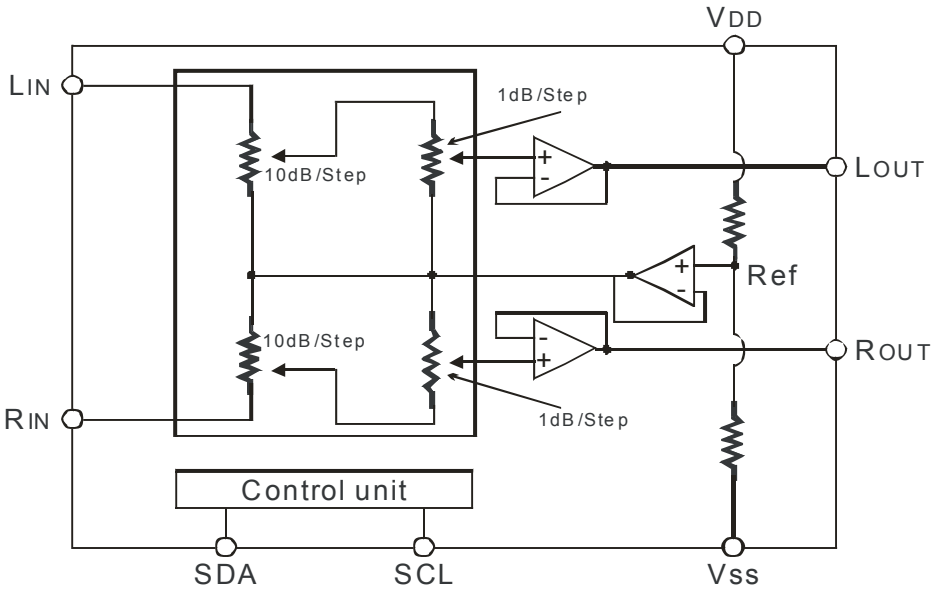
BLOCK DIAGRAM



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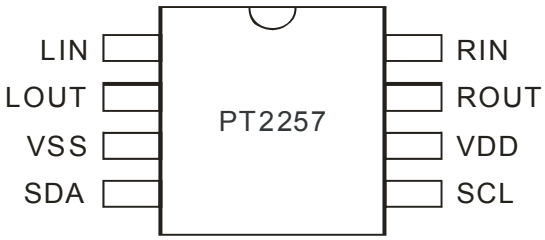
PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
L_{IN}	I	Left Input Channel Connect a Capacitor to Audio Source	1
L_{OUT}	O	Left Output Channel Connect a Capacitor to Audio Output	2
V_{SS}	-	Ground	3
SDA	I	I^2C Data Input	4
SCL	I	I^2C Clock Input	5
V_{DD}	-	Power Supply	6
R_{OUT}	O	Right Output Channel Connect a Capacitor to Audio Output	7
R_{IN}	I	Right Input Channel Connect a Capacitor to Audio Source	8

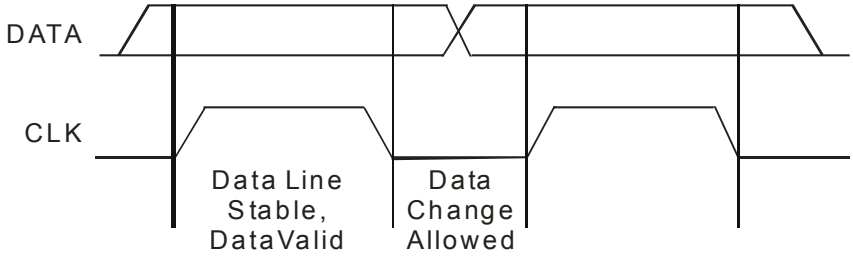
FUNCTION DESCRIPTION

BUS INTERFACE

Data are transmitted to and from the microprocessor to the PT2257 via the SDA and SCL. The SDA and SCL make up the BUS Interface. It should be noted that the pull-up resistors must be connected to the positive supply voltage.

DATA VALIDITY

A data on the SDA Line is considered valid and stable only when the SCL Signal is in HIGH State. The HIGH and LOW States of the SDA Line can only change when the SCL signal is LOW. Please refer to the figure below.



START AND STOP CONDITIONS

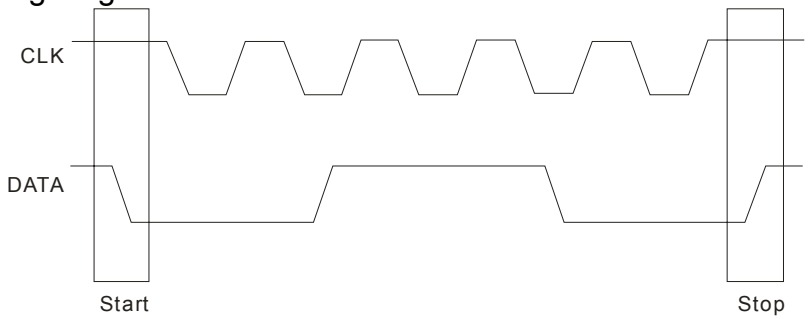
A Start Condition is activated when

1. the SCL is set to HIGH and
2. SDA shifts from HIGH to LOW State.

The Stop Condition is activated when

1. SCL is set to HIGH and
2. SDA shifts from LOW to HIGH State.

Please refer to the timing diagram below.

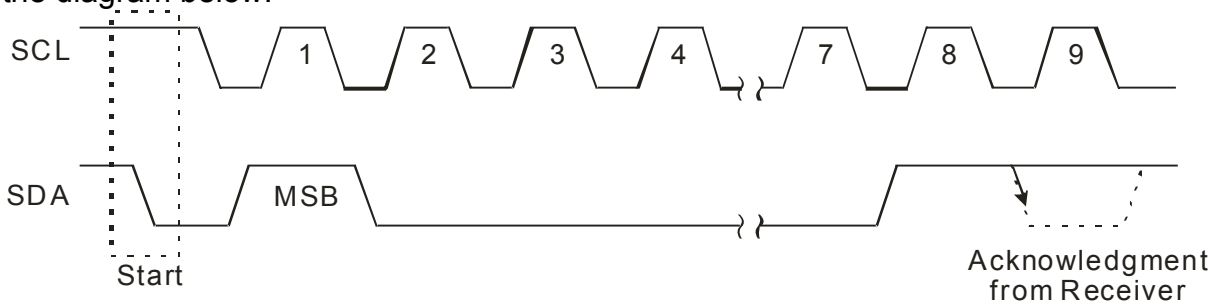


BYTE FORMAT

Every byte transmitted to the SDA Line consists of 8 bits. Each byte must be followed by an Acknowledge Bit. The MSB is transmitted first.

ACKNOWLEDGE

During the Acknowledge Clock Pulse, the master (μP) puts a resistive HIGH level on the SDA Line. The peripheral (audio processor) that acknowledges has to pull-down (LOW) the SDA line during the Acknowledge Clock Pulse so that the SDA Line is in a Stable Low State during this Clock Pulse. Please refer to the diagram below.



The audio processor that has been addressed has to generate an Acknowledge after receiving each byte; otherwise, the SDA Line will remain at the High Level during the ninth (9th) Clock Pulse. In this case, the master transmitter can generate the STOP Information in order to abort the transfer.

TRANSMISSION WITHOUT ACKNOWLEDGE

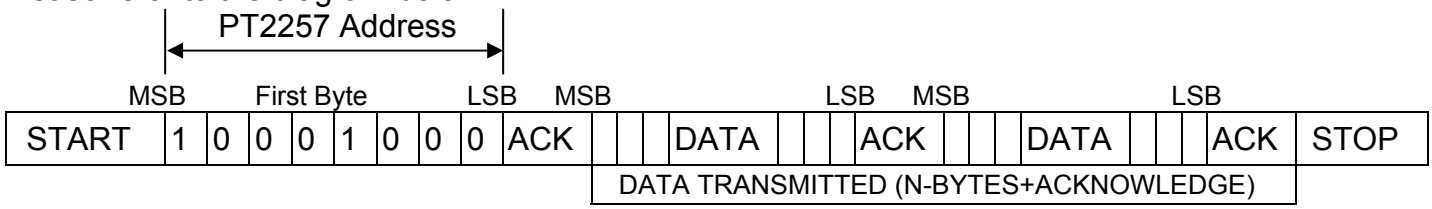
If you want to avoid the acknowledge detection of the audio processor, a simpler μP transmission may be used. Wait one clock and do not check the slave acknowledge of this same clock then send the new data. If you use this approach, there are greater chances of faulty operation as well as decrease in noise immunity.

INTERFACE PROTOCOL

The interface protocol consists of the following:

- A Start bit
- A Chip Address Byte=88H
- ACK=Acknowledge bit
- A Data byte
- A Stop bit

Please refer to the diagram below:



Note:
1. ACK=ACKNOWLEDGE
2. MAX. CLOCK SPEED=100K BITS/S

SOFTWARE SPECIFICATION

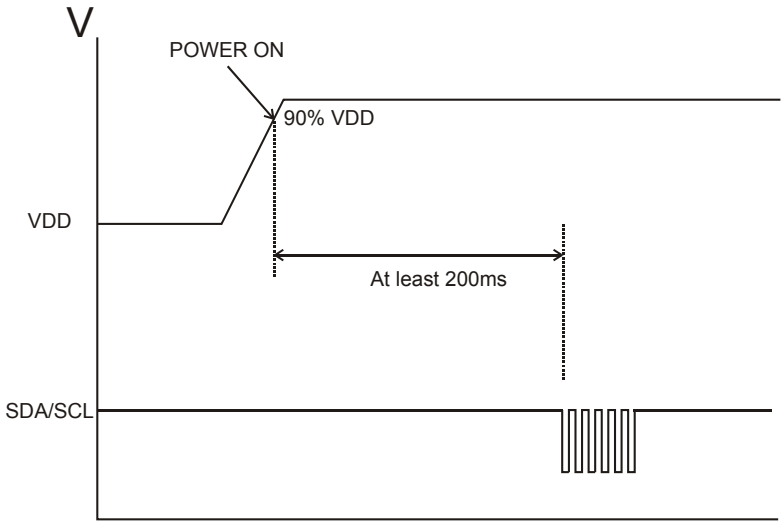
PT2257 ADDRESS

PT2257 Address is shown below:

1 MSB	0	0	0	1	0	0	0 LSB

I^2C BUS INTERFACE START TIME

After Power is turned ON, PT2257 needs to wait for a short time in order to insure stability. The waiting time period for PT2257 to send I^2C Bus Signal is at least 200ms. If the waiting time period is less than 200ms, I^2C Control may fail. Please refer to the diagram below.



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DATA BYTES DESCRIPTION

FUNCTION BITS

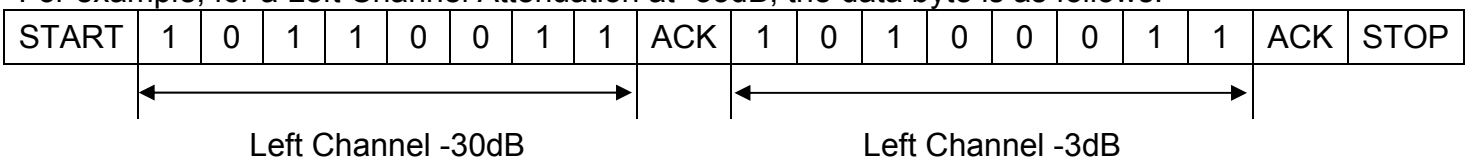
MSB	2	3	4	5	6	7	LSB	Function
1	1	1	1	1	1	1	1	Function OFF (-79dB)
1	1	0	1	A3	A2	A1	A0	2-Channel, -1dB/step
1	1	1	0	0	B2	B1	B0	2-Channel, -10dB/step
1	0	1	0	A3	A2	A1	A0	Left Channel, -1dB/step
1	0	1	1	0	B2	B1	B0	Left Channel, -10dB/step
0	0	1	0	A3	A2	A1	A0	Right Channel, -1dB/step
0	0	1	1	0	B2	B1	B0	Right Channel, -10dB/step
0	1	1	1	1	0	0	M	2-Channel, MUTE When M=1, MUTE=ON When M=0, MUTE=OFF

ATTENUATION UNIT BIT

A3	A2/B2	A1/B1	A0/B0	Attenuation Value (dB)
0	0	0	0	0/0
0	0	0	1	-1/-10
0	0	1	0	-2/-20
0	0	1	1	-3/-30
0	1	0	0	-4/-40
0	1	0	1	-5/-50
0	1	1	0	-6/-60
0	1	1	1	-7/-70
1	0	0	0	-8/
1	0	0	1	-9/

Where: Ax=-dB/step, Bx=-10dB/step

For example, for a Left Channel Attenuation at -33dB, the data byte is as follows:



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ABSOLUTE MAXIMUM RATING

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{CC}	12	V
Operating Temperature	Topr	-40 to +85	℃
Storage Temperature	Tstg	-65 to +150	℃
Input Voltage	V_I	-0.3 to V_{CC}+0.3	V

AUDIO SECTION ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Operating Voltage	V_{CC}			4	9	10	V
Operating Current	I_{CC}	V_{CC}=9V, V_I=0V		-	9	15	mA
Volume Attenuation Range	ARANGE	Minimum Attenuation		-	0	-	dB
		Maximum Attenuation		-	-79	-	
Attenuation Step	ASTEP			-	1	-	dB
Attenuation Step Gain Error	GERR			-	0.5	-	dB
Interchannel Attenuation Gain Error	CERR			-	0.5	-	dB
Maximum Output Voltage	Vomax	V_{CC}=9V, f=1KHz Volume Att=0dB Rload=50K, THD<1%		2.0	2.3	2.5	Vrms
Total Harmonic Distortion	THD	f=1KHz, Volume Att=0dB, A-weighted Rload=50K	Vout=2Vrms	-	0.07	0.09	%
			Vout=200m Vrms	-	0.003	0.005	
Noise Output	No	Vin=GND, MUTE=OFF Volume Att=0dB A-weighted		-	2	3	μVrms
Signal-to-Noise Ratio	SNR	0dB=1Vrms, ATT=0dB, A-weighted	No-weighted	95	100	103	dB
			A-weighted	110	120	125	
Channel Separation	CS	Vin=2.5Vrms, f=1KHz Volume Att=0dB		100	120	125	dB
Mute Attenuation	MUTE	Vin=2.5Vrms, f=1KHz Volume Att=0dB, A-weighted		90	95	97	dB
Frequency Response	FR	Vin=1Vrms, Volume Att=-10dB		-	1	1.3	MHz
Input Impedance	Rin	f=1KHz		18	20	-	KΩ
Output Impedance	Rout	f=1KHz, Vout=100m Vrms		-	100	-	Ω

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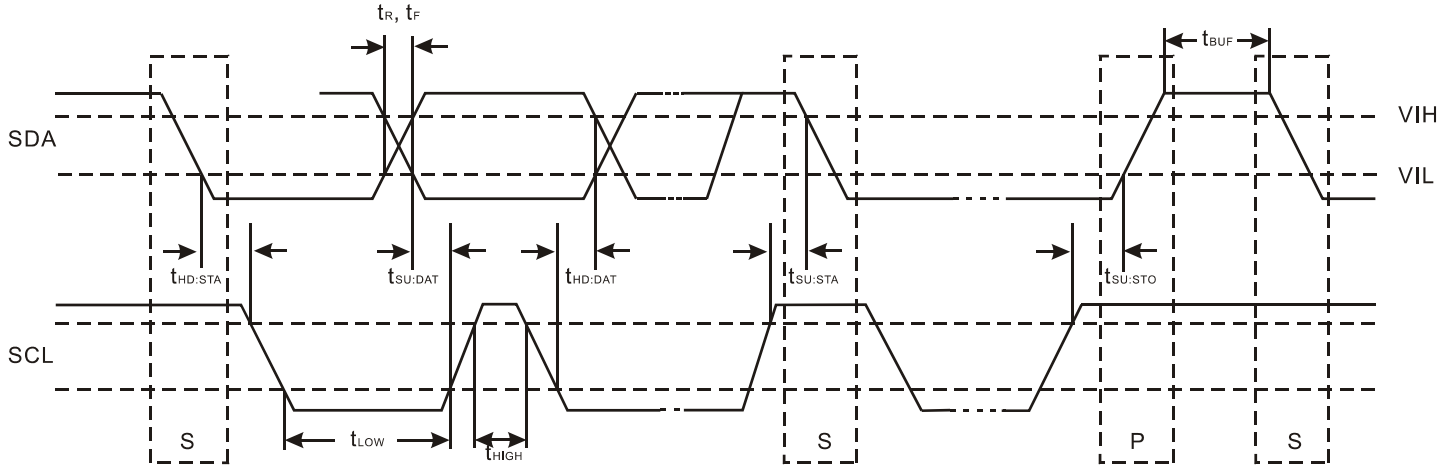
I²C BUS SECTION ELECTRICAL CHARACTERISTICS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bus High Input Level	VIH		0.5			VCC
Bus Low Input Level	VIL				0.2	VCC

BUS LINE TIMING CHARACTERISTICS

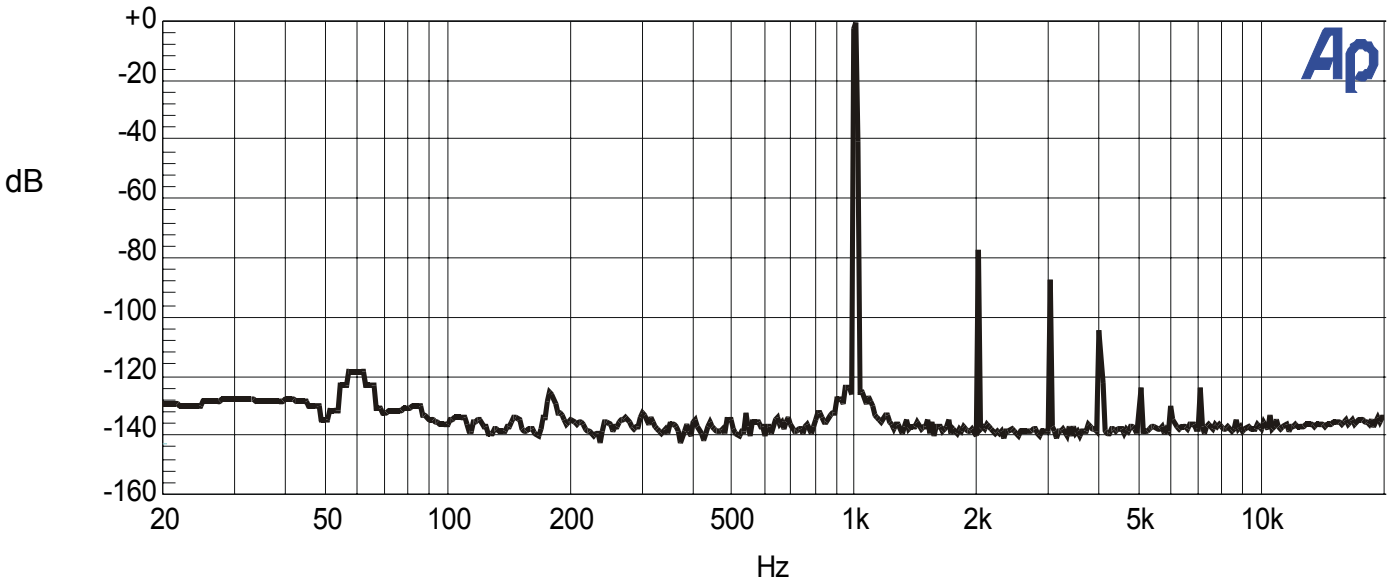


Parameter	Symbol	Condition	Min.	Max.	Unit
Low Level Input Voltage	V_{IL}	VDD=4.0V	-0.5	1.1	V
High level Input Voltage	V_{IH}	VDD=4.0V	1.6	4.0	V
SCL Clock Frequency	f_{SCL}		0	100	KHz
Time the bus must be free before a new transmission can start	t_{BUF}		5.0	-	μs
Hold Time Start Condition*	$t_{HD\text{-}STA}$		4.0	-	μs
Clock Low Period	t_{LOW}		5.0	-	μs
Clock High Period	t_{HIGH}		4.0	-	μs
Setup Time for Start Condition **	$t_{SU\text{-}STA}$		5.0	-	μs
Data Hold Time	$t_{HD\text{-}DAT}$		0	-	μs
Data Setup Time	$t_{SU\text{-}DAT}$		250	-	ns
Rise Time (SDA & SCL Lines)	t_R		-	1000	ns
Fall Time (SDA & SCL Lines)	t_F		-	300	ns
Stop Condition Setup Time	$t_{SU\text{-}STO}$		4.0	-	μs

Notes:
1. * = The first clock pulse is generated after this period.
2. ** = This is only relevant for a repeated start condition.

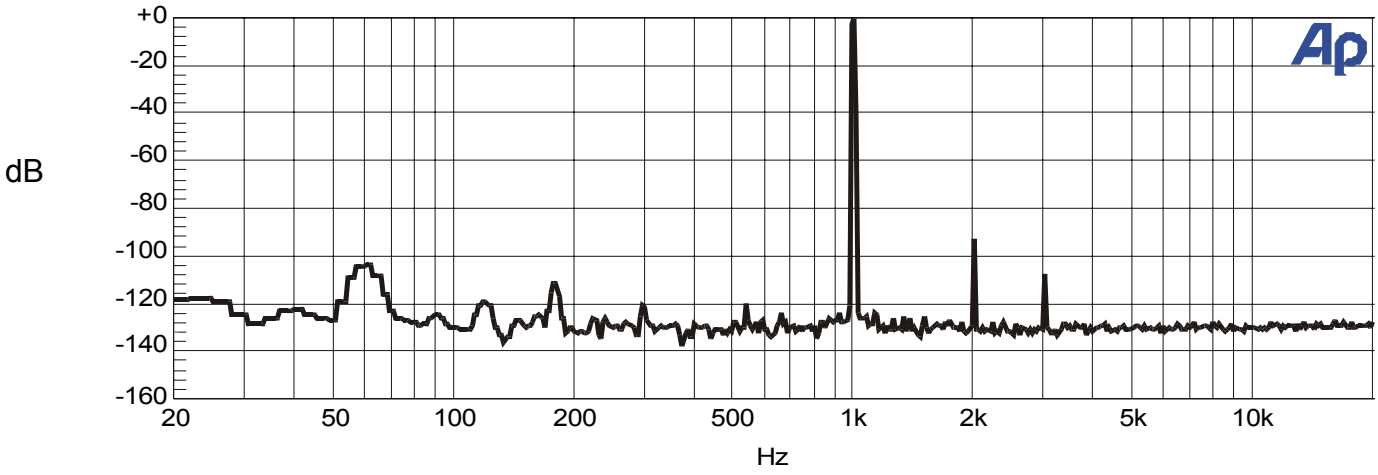
PT2257 THD - FAST FOURIER TRANSFORM (FFT) ANALYSIS 1

(Conditions: Rload=10K, Volume Att=0dB, VCC=9V, Output Level=1Vrms)



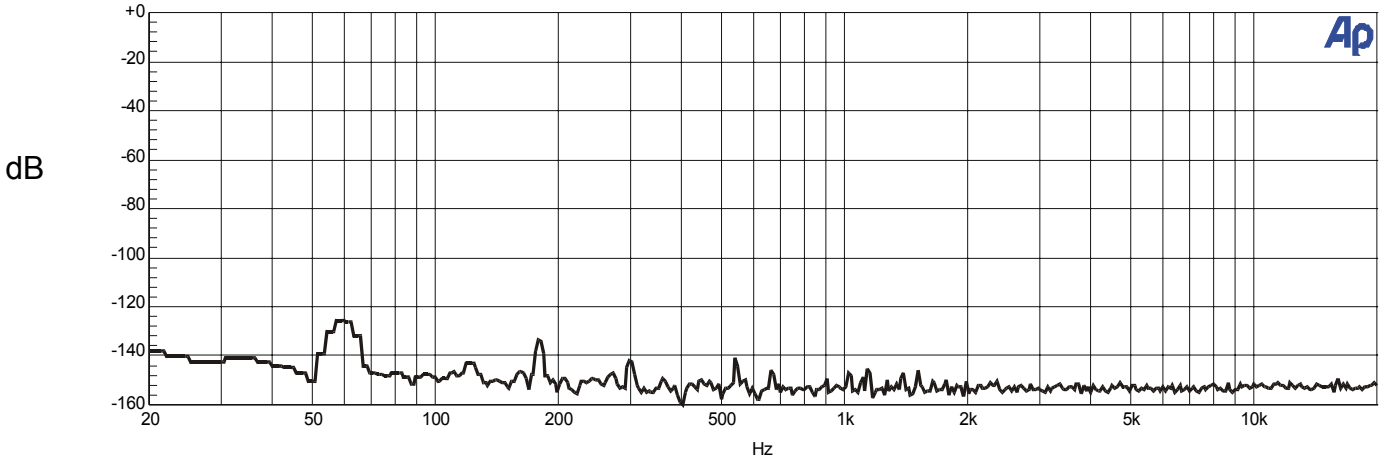
PT2257 THD - FAST FOURIER TRANSFORM (FFT) ANALYSIS 2

(Conditions: Rload=10K, Volume Att=0dB, VCC=9V, Output Level=200m Vrms)



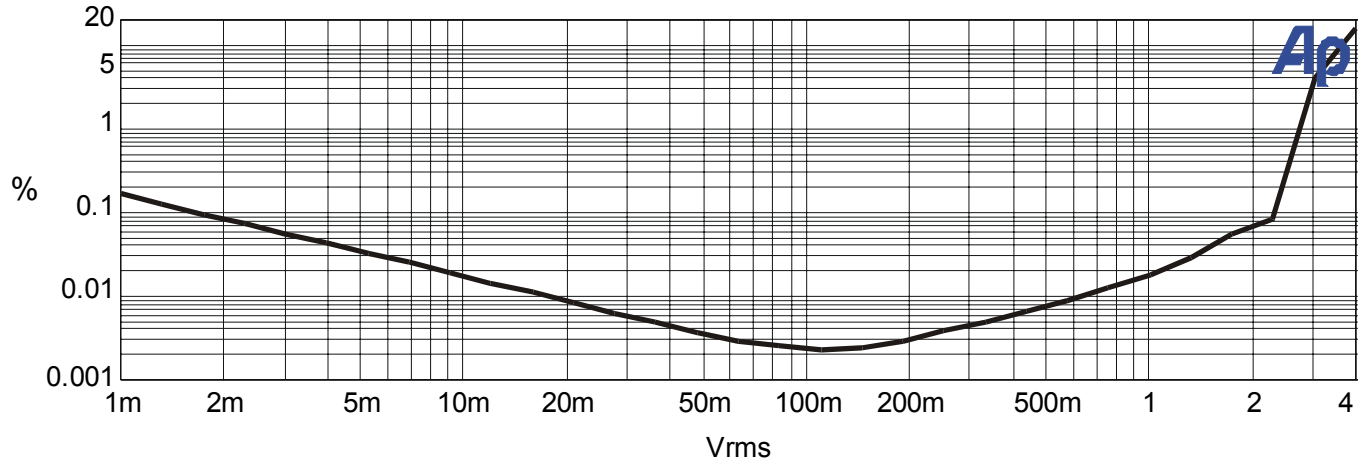
PT2257 NOISE FLOOR-FAST FOURIER TRANSFORM (FFT) ANALYSIS 3

(Conditions: Rload=10K, Volume Att=0dB, VCC=9V, Vin=GND)



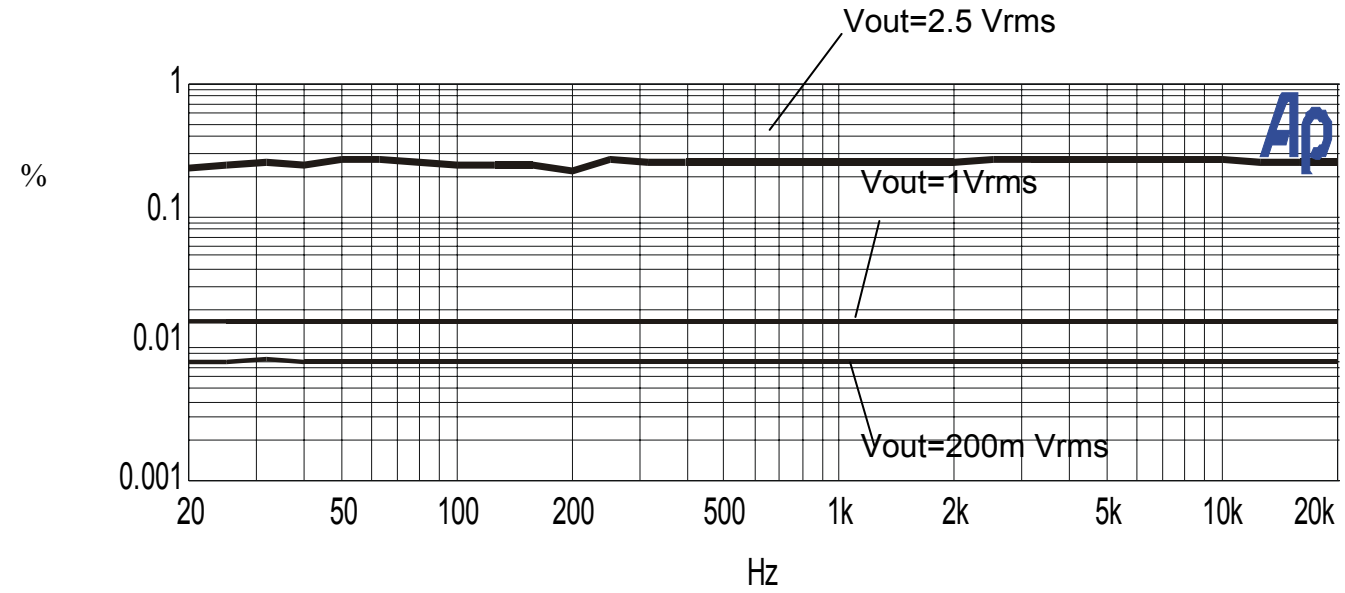
PT2257 THD VS. OUTPUT LEVEL

(Conditions: Rload=10K, Volume Att=0dB, VCC=9V, f=1KHz, A-weighted)



PT2257 THD VS FREQUENCY RESPONSE AT VARIOUS OUTPUT LEVELS

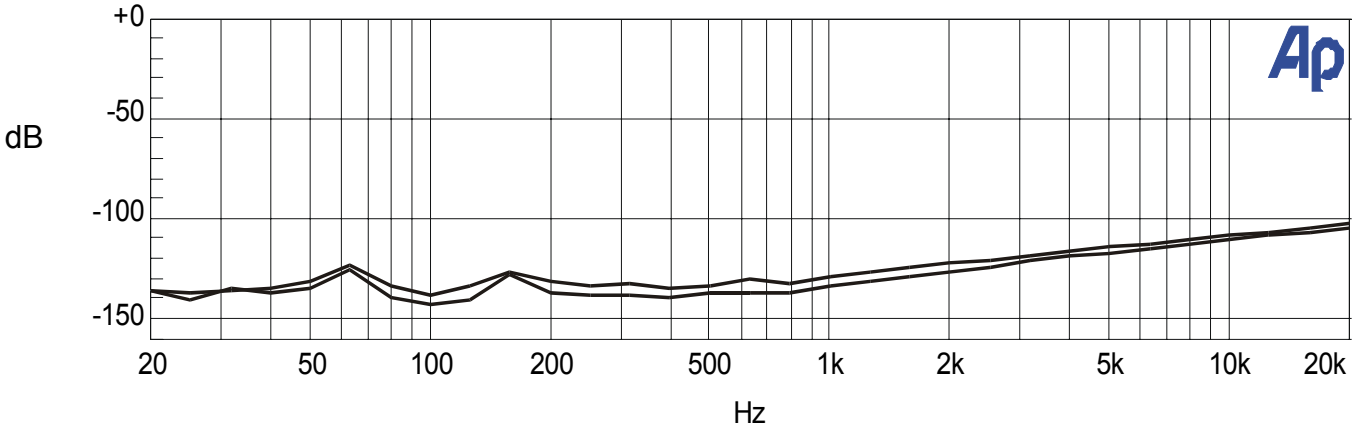
(Conditions: Rload=10K, Volume Att=0dB, No-weighted)



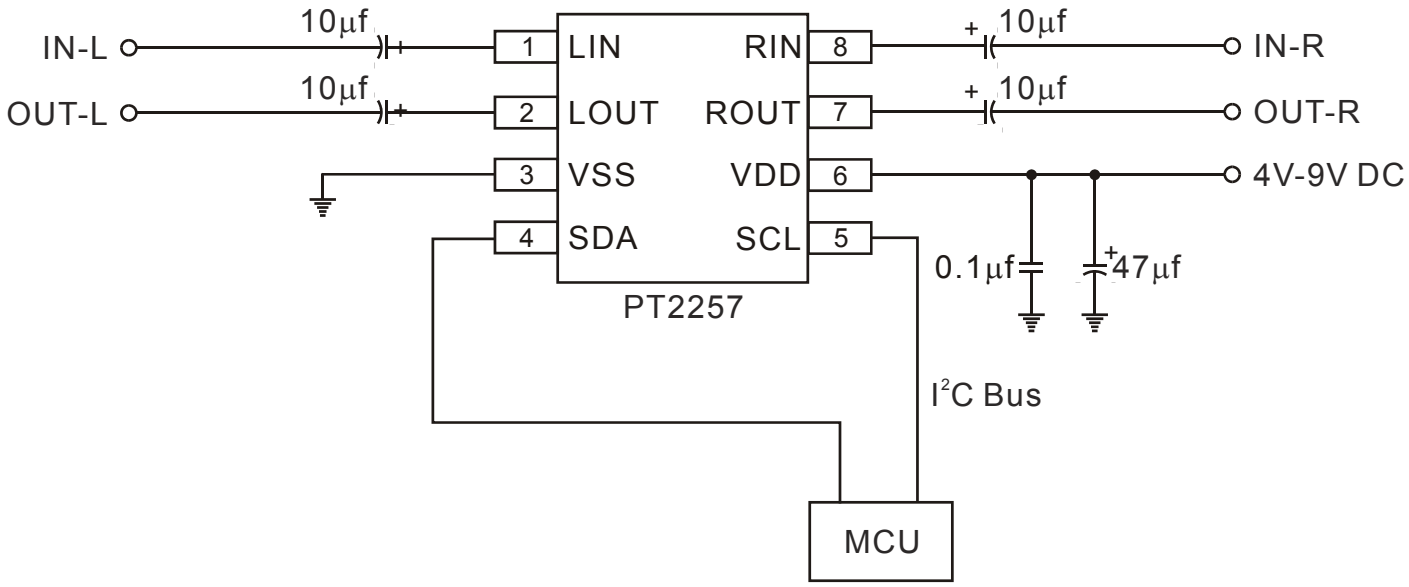
Note: From top to bottom: Vout=2.5Vrms, 1Vrms, 200mVrms

PT2257 INTERCHANNEL CROSSTALK

(Conditions: Rload=10K, Volume Att=0dB)



APPLICATION CIRCUIT



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ORDER INFORMATION

Valid Part Number	Package Type	Top Code
PT2257	8 Pins, DIP, 300mil	PT2257
PT2257-S	8 Pins, SOP, 150mil	PT2257-S
PT2257 (L)	8 Pins, DIP, 300mil	PT2257
PT2257-S (L)	8 Pins, SOP, 150mil	PT2257-S

Notes:
1. (L), (C) or (S) = Lead Free.
2. The Lead Free mark is put in front of the date code.

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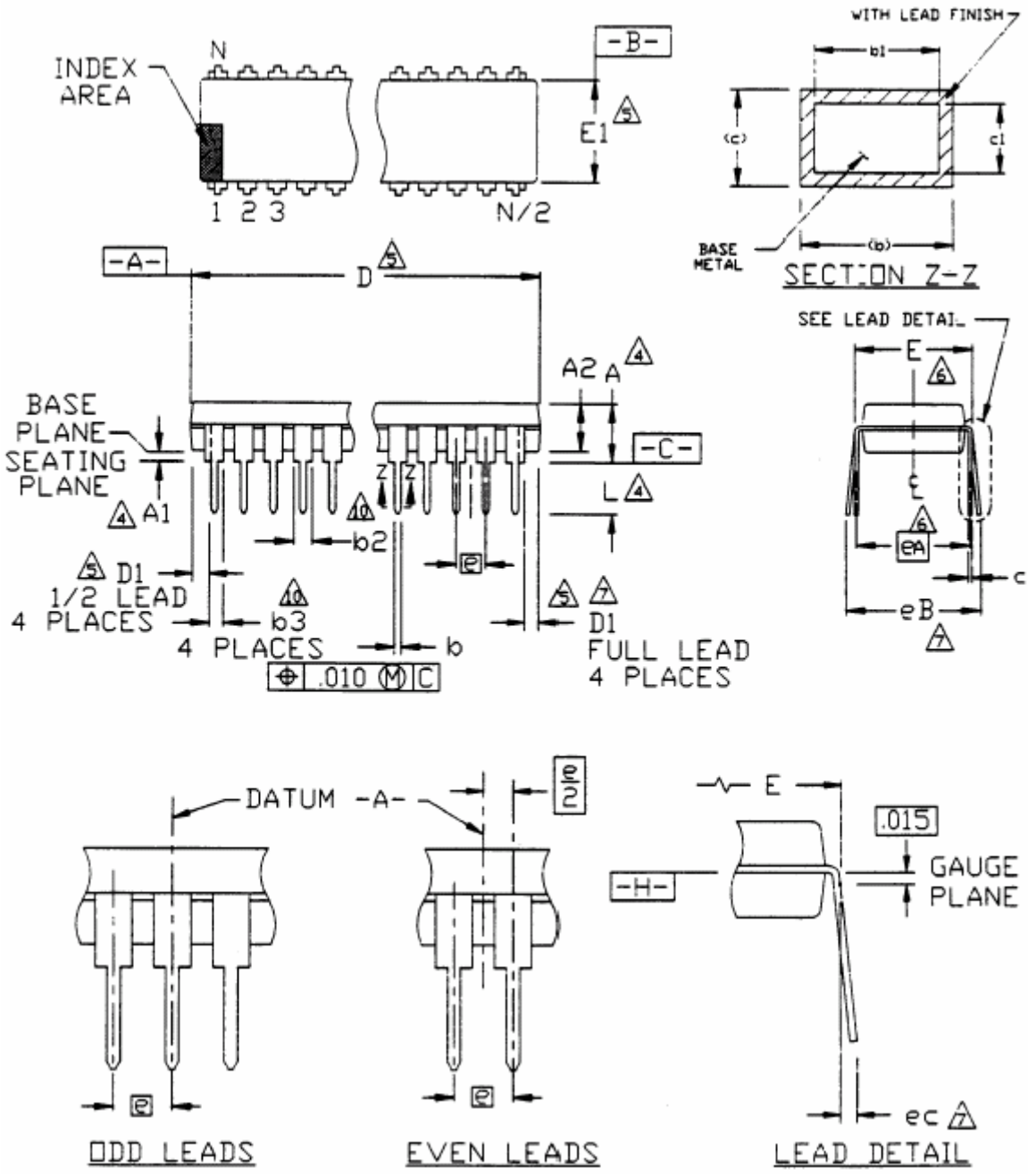
PACKAGE INFORMATION

8 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.355	0.365	0.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 BSC		
eA	0.300 BSC.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. Controlling Dimension: INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol LIST” in Section 2.2 of Publication No.95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
5. D, D1 and E1 dimension do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
6. E and eA measured with the leads constrained to be perpendicular to data -C- .
7. eB and eC are measured at the lead tips with the leads unconstrained.
8. N is the number of leads (N=8).
9. Pointed or rounded lead tips are preferred to ease insertion.
10. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25mm).
11. Variation BA has a b3 dimension and is 1/2 lead package.
12. Distance between the leads including dambar protrusions to be 0.005 inch minimum.
13. Datum plane -H- coincident with the bottom of lead where lead exits the body.
14. Refer to JEDEC MS-001 variation BA.

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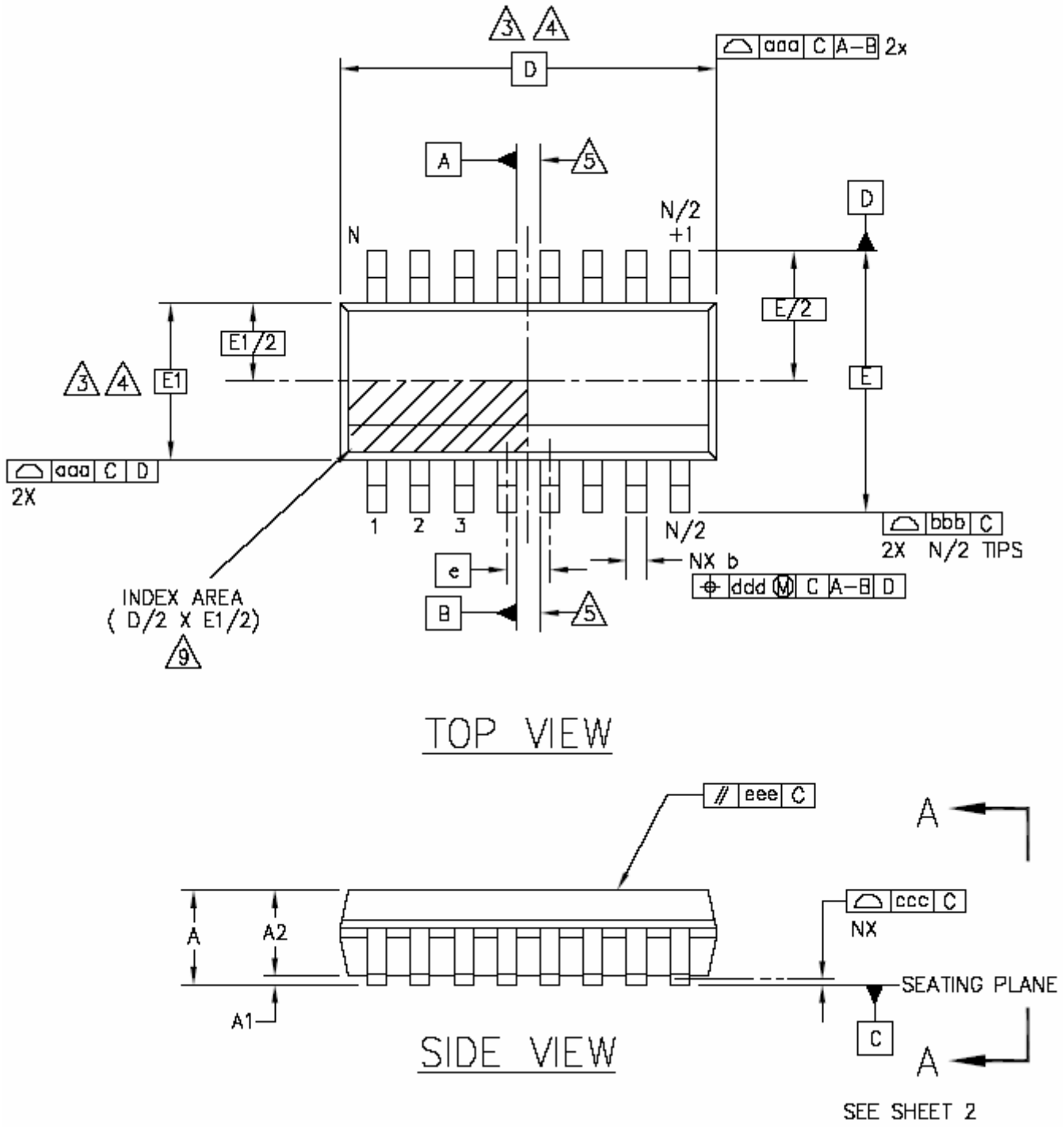
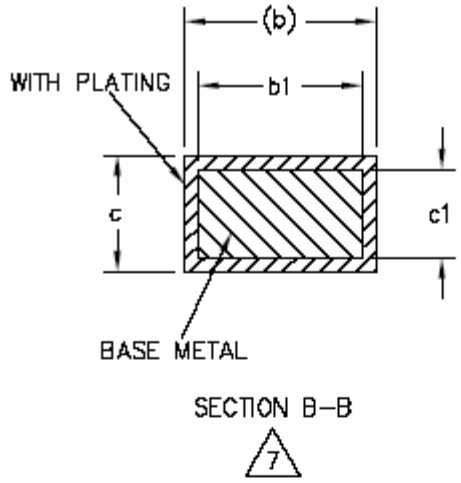
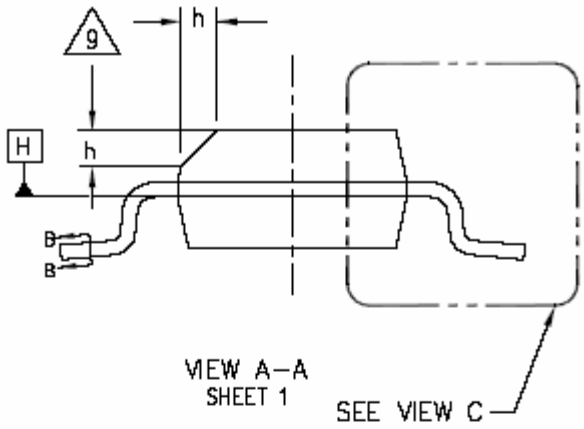
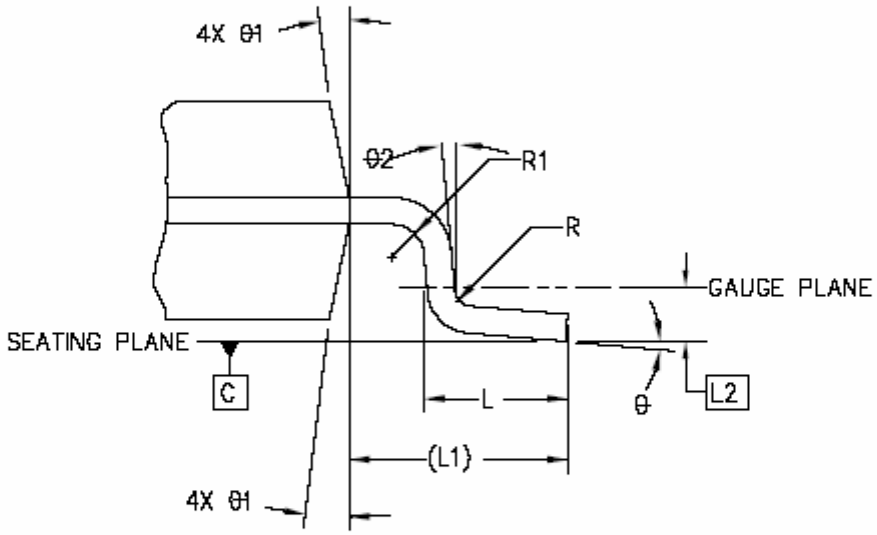
8 PINS, SOP, 150MIL

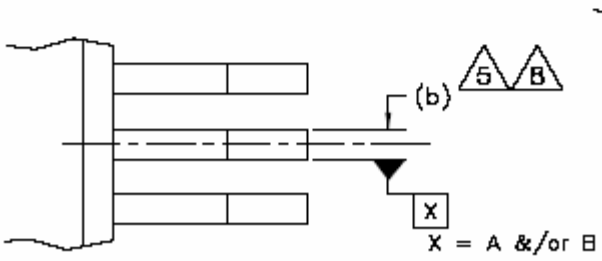




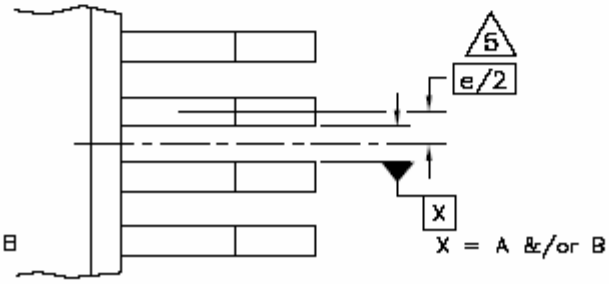




VIEW C



ODD LEAD SIDES
TOPVIEW



EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AA.

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