T-46-13-29

PRELIMINARY

CY7C258
CY7C259

CYPRESS SEMICONDUCTOR

2K x 16 Reprogrammable State Machine PROM

Features

- **High speed: 83-MHz operation**
  - **—t_{CP} = 12 ns**
  - **—t_{CKO} = 9 ns**
  - **—t_{AS} = 3 ns**
- **16-bit-wide state word**
- **Optimum speed/ power**
- **Individually bypassable input and output registers**
- **Individually programmable address/ feedback muxes**
- **Synchronous and asynchronous chip select**
- **Synchronous and asynchronous $\overline{INIT}$ and programmable initialize word**
- **16 outputs (CY7C259)**
- **Software support**
- **CY7C258 available in 28-pin, 300-mil plastic and ceramic DIP, LCC, PLCC**
- **CY7C259 available in 44-pin LCC and PLCC**
- **Reprogrammable in windowed packages**
- **Capable of withstanding greater than 2001V static discharge**

Functional Description

The CY7C258 and CY7C259 are 2K x 16 CMOS PROMS specifically designed for use in state machine applications.

State machines are one of the most common applications for registered PROMs. The CY7C258 and CY7C259 feature internal state feedback and a variety of programmable features to support 83-MHz state machines with as many as 2,048 distinct states.

It is easy to use a PROM as a state machine. Each array location contains output data as well as information fed back to select the next state. Note that a PROM is only limited by the number of array inputs. If a given state machine can be implemented in the number of inputs/feedbacks available (11 on the CY7C258/259), then it will always fit in the device. No software minimization is required.

Among the programmable features of the CY7C258/CY7C259 are individually bypassable input and output registers. The registers run off the same clock for pipeline capability. Each individual register can be programmed to capture data at the rising edge of the clock or to be transparent.

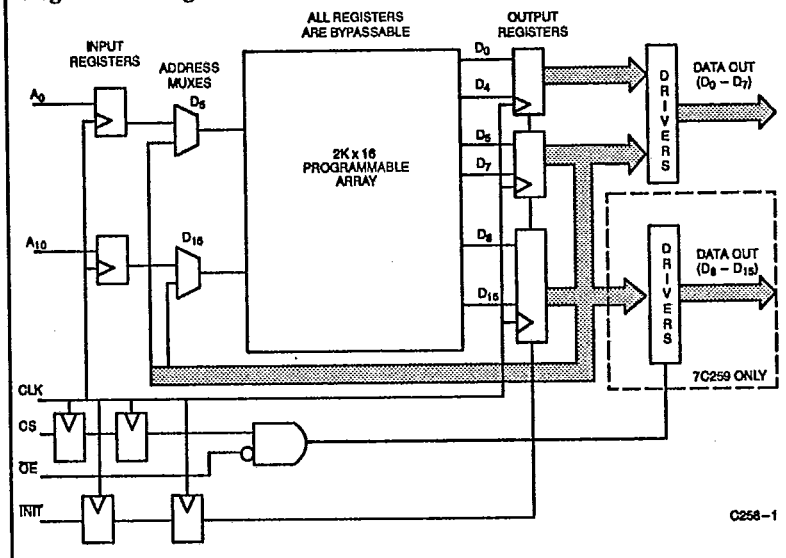
The registers at the inputs are useful for signals that require short set-up times (t_{AS} = 3 ns). The input register does intro- duce a cycle of latency, however. For signals that directly affect the next state of the machine, each input register can be bypassed. Note that the cycle time remains the same (12-ns min.), even if the inputs are bypassed.

Registers at the output are used to hold both state information and output data. These registers are also bypassable for maximum flexibility. Occasionally, an individual output cannot wait for the next clock edge. These outputs are sometimes called Mealy outputs, and can be created by bypassing the appropriate output register.

Since the CY7C258 and CY7C259 contain a 2K array, they each require 11 inputs. Each of these inputs can come from an input pin or from internal output register feedback. Eleven individually programmable address muxes allow the user to select the ratio of pin input and state feedback.

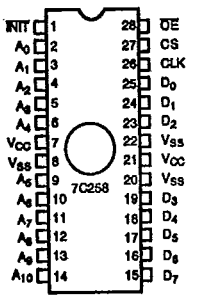
These devices have both an asynchronous output ($\overline{OE}$) and a synchronous chip select (CS). The CS input is polarity

Logic Block Diagram



Pin Configurations

DIP
Top View



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Functional Description (continued)

programmable and registered twice. Each of the CS registers can be bypassed in the same manner as the address input and output registers.

A separately controllable INIT input is included for user resets. If INIT is sampled LOW on the rising edge of CLK, the user programmable initialization word will appear at the outputs after the next CLK cycle. Each of the INIT registers can be bypassed in the same manner as the address input and output registers.

The difference between the CY7C258 and CY7C259 is in the packaging. The CY7C258 has three different types of outputs. $D_4 - D_0$ are dedicated outputs that do not feed back to the input registers. $D_5 - D_7$ appear on the outputs and are fed back to the input muxes. Finally, $D_8 - D_{15}$ are dedicated feedback lines that do not appear at the external outputs. The dedicated feedback allows the CY7C258 to be packaged in 28-pin packages. The CY7C258 is available in 28-pin LCC, PLCC, and slim 300-mil DIP packages.

On the CY7C259, all 16 array outputs are available at the pins. Outputs $D_4 - D_0$ remain as dedicated outputs while $D_5 - D_{15}$ appear at the pins and are also fed back to the input muxes. This organization allows the user maximum flexibility in selecting the ratio of outputs to state feedback. The availability of state information at pins also improves testability. The CY7C259 is packaged in 44-pin LCC and PLCC packages.

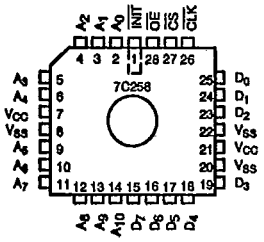
To make it easier to use the CY7C258 and CY7C259, the devices are supported in the Cypress PLD Toolkit, including the waveform simulator. Several third-party programmers also feature support for PROMs as state machines, including Data I/O (ABEL) and ISDATA (LOG/iC).

The CY7C258 and CY7C259 offer the advantage of low power, superior performance, and programming yield. The EPROM cells allow for each memory location to be 100% tested, with each location being written into, erased, and repeatedly exercised prior to encapsulation. Each PROM is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

PROMs

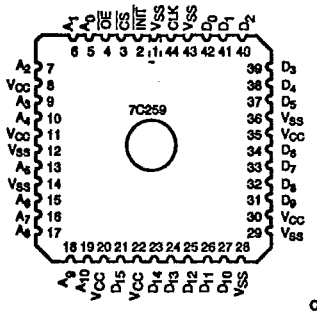
Pin Configurations (continued)

LCC/PLCC(Opaque Only)
Top View



C258-3

PLCC (Opaque Only)
Top View



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Selection Guide

	Commercial			Military			Units
	12 ns	15 ns	18 ns	15 ns	18 ns	25 ns	
Minimum Cycle Time	12	15	18	15	18	25	ns
Registered Input Set-Up/Hold[1]	3/3 or 7/0	4/4 or 8/1	5/5 or 9/2	4/4 or 8/1	5/5 or 9/2	6/6 or 10/3	ns
Bypassed Input Set-Up/Hold	12/0	15/0	18/0	15/0	18/0	25/0	ns
Clock-to-Output	9	11	13	11	13	15	ns
Maximum Operating Current	175	175	175	200	200	200	mA

Shaded area contains advanced information.

Notes:
1. This parameter is programmable.

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Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... – 65°C to +150°C
Ambient Temperature with Power Applied ..... – 55°C to +125°C
Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... – 0.5V to +7.0V
DC Voltage Applied to Outputs in High Z State ..... – 0.5V to +7.0V
DC Input Voltage ..... – 3.0V to +7.0V
DC Program Voltage 13.0V
Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)
Latch-Up Current ..... >200 mA
UV Exposure ..... 7258 Wsec/cm^2

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[2]	– 40°C to +85°C	5V ± 10%
Military[3]	– 55°C to +125°C	5V ± 10%

Electrical Characteristics Over the Operating Range[4, 5, 6]

Parameter	Description	Test Conditions		Min.	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = – 2 mA		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8 mA	Commercial		0.4	V
		V_{CC} = Min., I_{OL} = 6 mA	Military		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs		2.0	6.0	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs		– 3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_{IN} ≤ V_{CC}		– 10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		– 40	+40	µA
I_{OS}	Output Short Circuit Current[7]	V_{CC} = Max., V_{OUT} = GND		– 20	– 90	mA
I_{CC}	Maximum Operating Current	V_{CC} = Max., I_{OUT} = 0 mA	Commercial		175	mA
		V_{CC} = Max., I_{OUT} = 0 mA	Military		200	mA

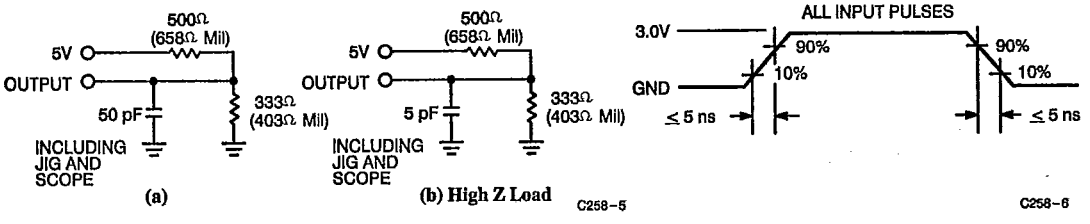
Capacitance[5]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

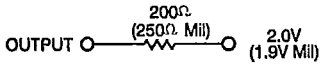
Notes:

2. Contact a Cypress representative for industrial temperature range specification.
3. T_A is the "instant on" case temperature.
4. See the last page of this specification for Group A subgroup testing information.
5. See Introduction to CMOS PROMs in this Data Book for general information on testing.
6. Data for 12-ns Commercial and 15-ns Military is advanced information.
7. For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed 30 seconds.

AC Test Loads and Waveforms[4]



Equivalent to: THEVENIN EQUIVALENT



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Switching Characteristics Over the Operating Range[3,4]

Parameters	Description	Commercial						Military						Units
		12 ns		15 ns		18 ns		15 ns		18 ns		25 ns		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{CP}	Clock Period	12		15		18		15		18		25		ns
t_{CH}	Clock HIGH	5		6.5		8		6.5		8		11.5		ns
t_{CL}	Clock LOW	5		6.5		8		6.5		8		11.5		ns
t_{AS}	Address Set-Up to CLK	3/7		4/8		5/9		4/8		5/9		6/10		ns
t_{AH}	Address hold from CLK	3/0		4/1		5/2		4/1		5/2		6/3		ns
t_{ABS}	Address Set-Up to CLK with Input Bypassed	12		15		18		15		18		25		ns
t_{ABH}	Address Hold from CLK with Input Bypassed	0		0		0		0		0		0		ns
t_{CSS}	Chip Select Set-Up to CLK	3/7		4/8		5/9		4/8		5/9		6/10		ns
t_{CSH}	Chip Select Hold from CLK	3/0		4/1		5/2		4/1		5/2		6/3		ns
t_{CKO}	CLK to Data Valid		9		11		13		11		13		15	ns
t_{DH}	Data Hold From CLK	0		0		0		0		0		0		ns
t_{COV}	CLK to Output Valid[7]		9		11		13		11		13		15	ns
t_{COZ}	CLK to High Z Output[8]		9		11		13		11		13		15	ns
t_{CSV}	CS to Output Valid with Input Bypassed[8]		12		15		18		15		18		21	ns
t_{CSZ}	CS to High Z Output with Input Bypassed [8]		12		15		18		15		18		21	ns
t_{OEV}	$\overline{OE}$ to Output Valid[7]		9		11		13		11		13		15	ns
t_{OEZ}	$\overline{OE}$ to High Z Output[8]		9		11		13		11		13		15	ns
t_{IS}	$\overline{INIT}$ Set-Up to CLK	3/7		4/8		5/9		4/8		5/9		6/10		ns
t_{IH}	$\overline{INIT}$ Hold from CLK	3/0		4/1		5/2		4/1		5/2		6/3		ns
t_{IBS}	$\overline{INIT}$ Set-Up to CLK with Input Bypassed	12		15		18		15		18		25		ns
t_{IBH}	$\overline{INIT}$ Hold from CLK with Input Bypassed	0		0		0		0		0		0		ns
t_{PD}	Propagation Delay with Input and Output Bypassed		18		21		25		21		25		30	ns
t_{ICO}	CLK to Output Valid with Output Bypassed		18		21		25		21		25		30	ns
t_{IW}	Asynchronous $\overline{INIT}$ Pulse Width	12		15		18		15		18		25		ns
t_{IDV}	Asynchronous $\overline{INIT}$ to Data Valid		12		15		18		15		18		25	ns
t_{ICR}	Asynchronous $\overline{INIT}$ Recovery to Clock	12		15		18		15		18		25		ns

Shaded area contains advanced information.

Notes:
8. See Output Waveform—Measurement Level

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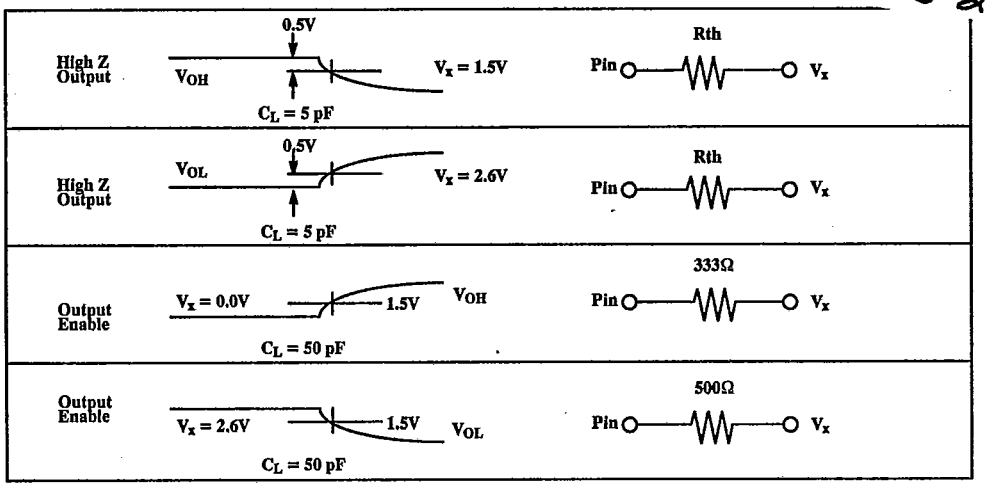
Output Waveform—Measurement Level



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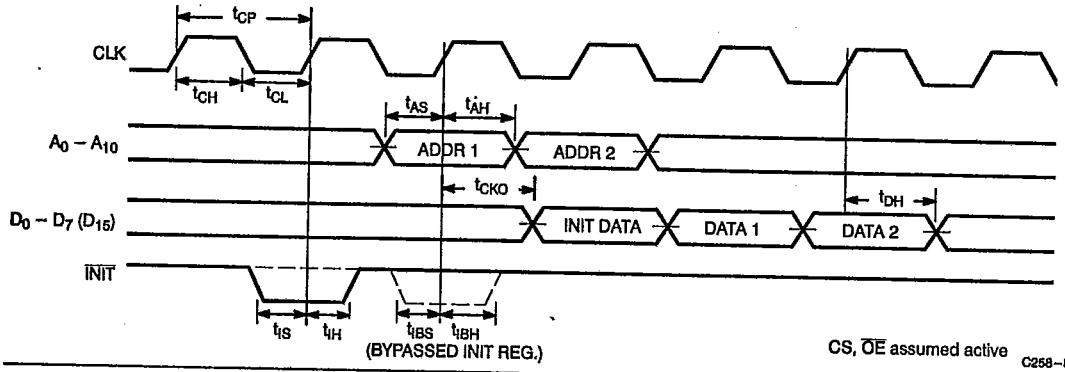
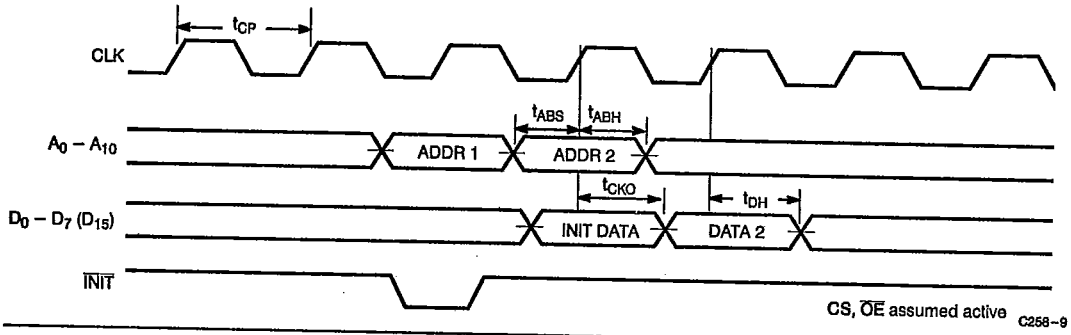
Switching Waveforms

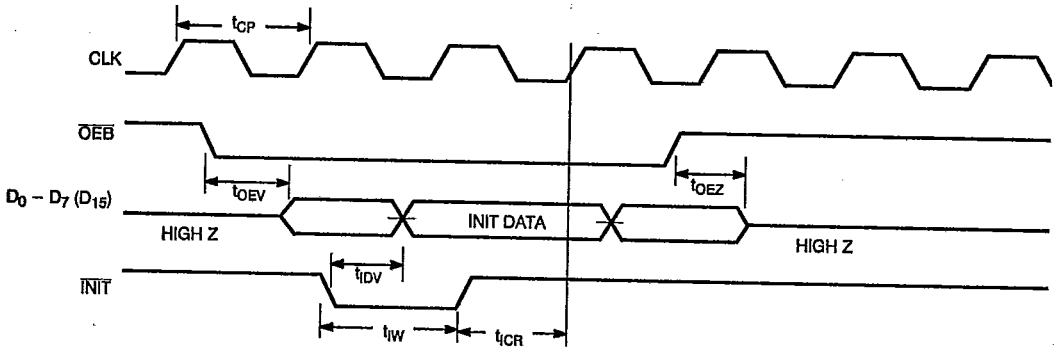
Registered Input and Output (combined with $\overline{INIT}$)



Bypassed Address and $\overline{INIT}$ Registers



Asynchronous $\overline{INIT}$ and $\overline{OE}$



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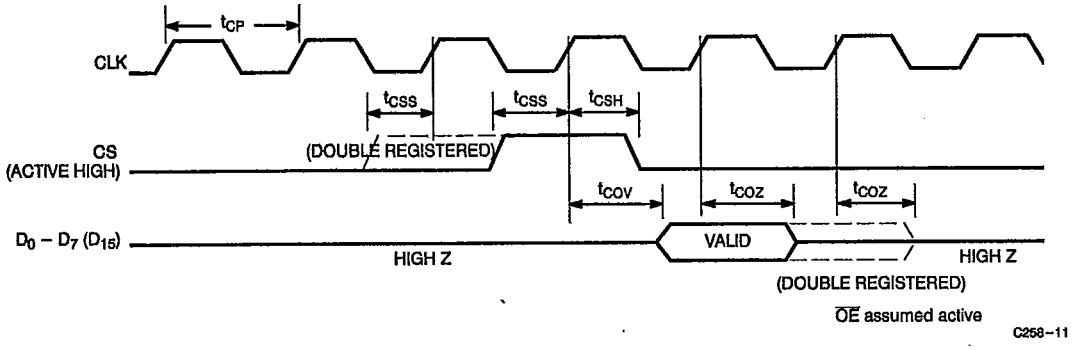
Switching Waveforms

Single- and Double-Registered Chip Select



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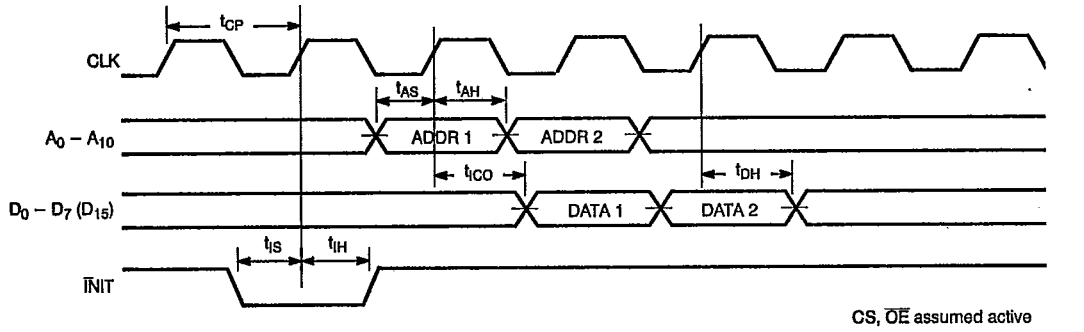
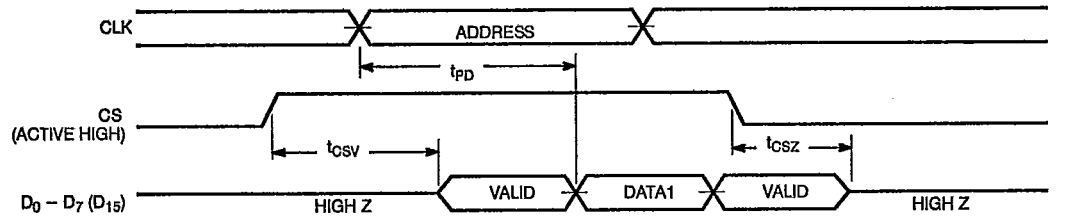
Bypassed Output Register[9]



C258–12

Bypassed Input and Output Register (CS and Address)



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Note:
9. INIT only sets output register even though register is bypassed (for feedback purposes).

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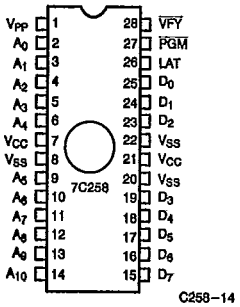
Mode Table

Mode	LAT (7C258–CLK)	$\overline{VPP}$ ($\overline{INIT}$)	$\overline{PGM}$ ($\overline{CS}$)	$\overline{VFY}$ ($\overline{OE}$)	D_0–D_{15} (259) D_0–D_7 (258)
Latch High Byte	V_{IHP}	V_{PP}	V_{IHP}	V_{IHP}	V_{IHP}/V_{ILP}
Program Inhibit	V_{ILP}	V_{PP}	V_{IHP}	V_{IHP}	HI–Z
Program Enable	V_{ILP}	V_{PP}	V_{ILP}	V_{IHP}	V_{IHP}/V_{ILP}
Program Verify	V_{ILP}	V_{PP}	V_{IHP}	V_{ILP}	V_{OHP}/V_{OLP}

PROMs

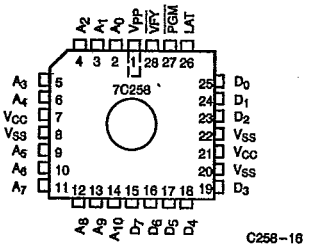
Programming Pinouts

DIP



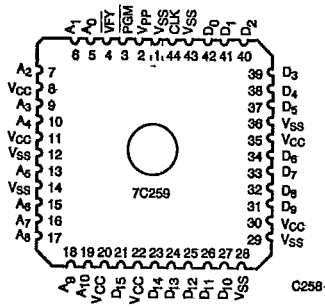
C258–14

LCC/PLCC



C258–16

LCC/PLCC



C258–15

Programming Information

This datasheet provides some but not all the programming information necessary for on-board programming of the CY7C258 and CY7C259. For more information about on-board programming of Cypress PROMs contact your local Cypress Field Sales Engineer or Field Applications Engineer.

7C258 Bitmap[10]

Programmer Address Decimal	Programmer Address Hex	Programmer Memory 7C258	Bit Breakdown D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0	0	Data	Array Data
.	.	.	
.	.	.	
.	.	.	
2047	7FF	Data	
2048	800	Address Register Select (1=Bypassed Register)	A_9 A_8 A_7 A_6 A_5 A_2 A_1 A_0 A_{10} X X X X X A_4 A_3
2049	801	Array Input Select (1= Feedback)	A_9 A_8 A_7 A_6 A_5 A_2 A_1 A_0 A_{10} X X X X X A_4 A_3
2050	802	Output Register Select (1= Bypassed Register)	X X X X X X X X D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2051	803	INIT WORD (1= INIT Bit 1)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2052	804	Architecture	X X X X X X X X SH C_1 C_2 CP IB IA X X

Notes:
10. All configurable bits default to 0.

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7C259 Bitmap[10]

Programmer Address Decimal	Programmer Address Hex	Programmer Memory 7C259	Bit Breakdown D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
0	0	Data	Array Data
.	.	.	
.	.	.	
.	.	.	
2047	7FF	Data	
2048	800	Address Register Select (1 = Bypassed Register)	A_{10} A_9 A_8 A_7 A_6 A_5 X X X X X A_4 A_3 A_2 A_1 A_0
2049	801	Array Input Select (1 = Feedback)	A_{10} A_9 A_8 A_7 A_6 A_5 X X X X X A_4 A_3 A_2 A_1 A_0
2050	802	Output Register Select (1 = Bypassed Register)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2051	803	INIT WORD (1 = INIT Bit 1)	D_{15} D_{14} D_{13} D_{12} D_{11} D_{10} D_9 D_8 D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0
2052	804	Architecture	SH C_1 C_2 CP IB IA X X X X X X X X X X

Architecture Word

Control Option	Control Word			Function
	Bit (258)	Bit (259)	Programmed level	
IA (INIT Async)	D_2	D_{10}	0 = Default 1 = Programmed	Synchronous INIT Asynchronous INIT
IB (INIT Bypass)	D_3	D_{11}	0 = Default 1 = Programmed	INIT Registered Bypass INIT Register
CP (CS Polarity)	D_4	D_{12}	0 = Default 1 = Programmed	CS Active LOW CS Active HIGH
C2 (CS Bypass) (Buried Register)	D_5	D_{13}	0 = Default 1 = Programmed	CS Input Registered Bypass CS Register
C1 (CS Bypass) (Input Register)	D_6	D_{14}	0 = Default 1 = Programmed	CS Input Registered Bypass CS Register
SH (Set-Up/Hold)	D_7	D_{15}	0 = Default 1 = Programmed	Set-Up/Hold = 3/3 ns Set-Up/Hold = 7/0 ns

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Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C258–12DC	D16	Commercial
	CY7C258–12HC	H64	
	CY7C258–12JC	J64	
	CY7C258–12PC	P15	
	CY7C258–12WC	W22	
15	CY7C258–15DC	D16	Commercial
	CY7C258–15HC	H64	
	CY7C258–15JC	J64	
	CY7C258–15PC	P15	
	CY7C258–15WC	W22	
	CY7C258–15HMB	H64	Military
	CY7C258–15LMB	L64	
	CY7C258–15QMB	Q64	
	CY7C258–15WMB	W22	
18	CY7C258–18DC	D16	Commercial
	CY7C258–18HC	H64	
	CY7C258–18JC	J64	
	CY7C258–18PC	P15	
	CY7C258–18WC	W22	
	CY7C258–18HMB	H64	Military
	CY7C258–18LMB	L64	
	CY7C258–18QMB	Q64	
	CY7C258–18WMB	W22	
25	CY7C258–25HMB	H64	Military
	CY7C258–25LMB	L64	
	CY7C258–25QMB	Q64	
	CY7C258–25WMB	W22	

Shaded area contains advanced information.

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C259–12HC	H67	Commercial
	CY7C259–12JC	J67	
15	CY7C259–15HC	H67	Commercial
	CY7C259–15JC	J67	
	CY7C259–15HMB	H67	Military
	CY7C259–15LMB	L67	
	CY7C259–15QMB	Q67	
18	CY7C259–18HC	H67	Commercial
	CY7C259–18JC	J67	
	CY7C259–18HMB	H67	Military
	CY7C259–18LMB	L67	
	CY7C259–18QMB	Q67	
25	CY7C259–25HMB	H67	Military
	CY7C259–25LMB	L67	
	CY7C259–25QMB	Q67	

Shaded area contains advanced information.

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MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3,
V_{OL}	1, 2, 3,
V_{IH}	1, 2, 3,
V_{IL}	1, 2, 3,
I_{IX}	1, 2, 3,
I_{OZ}	1, 2, 3,
I_{CC}	1, 2, 3,
I_{SB}	1, 2, 3,

Switching Characteristics

Parameters	Subgroups
t_{CP}	7, 8, 9, 10, 11
t_{CH}	7, 8, 9, 10, 11
t_{CL}	7, 8, 9, 10, 11
t_{AS}	7, 8, 9, 10, 11
t_{ABS}	7, 8, 9, 10, 11
t_{CSS}	7, 8, 9, 10, 11
t_{CSH}	7, 8, 9, 10, 11
t_{CKO}	7, 8, 9, 10, 11
t_{DH}	7, 8, 9, 10, 11
t_{COV}	7, 8, 9, 10, 11
t_{CSV}	7, 8, 9, 10, 11
t_{CSZ}	7, 8, 9, 10, 11
t_{OEV}	7, 8, 9, 10, 11
t_{OEZ}	7, 8, 9, 10, 11
t_{IS}	7, 8, 9, 10, 11
t_{IH}	7, 8, 9, 10, 11
t_{IBS}	7, 8, 9, 10, 11
t_{IBH}	7, 8, 9, 10, 11
t_{PD}	7, 8, 9, 10, 11
t_{ICO}	7, 8, 9, 10, 11
t_{IW}	7, 8, 9, 10, 11
t_{IDV}	7, 8, 9, 10, 11
t_{ICR}	7, 8, 9, 10, 11

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