UHF power MOS transistor BLF404

FEATURES

- High power gain
- Easy power control
- Gold metallization
- Good thermal stability
- Withstands full load mismatch
- Designed for broadband operation.

APPLICATIONS

- Communication transmitters in the VHF/UHF range with a nominal supply voltage of 12.5 V.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS power transistor in an 8-lead SOT409A SMD package with a ceramic cap.

PINNING

PIN	DESCRIPTION
1, 8	source
2, 3	gate
4, 5	source
6, 7	drain

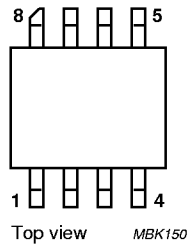


Fig.1 Simplified outline SOT409A.

QUICK REFERENCE DATA

RF performance at $T_{mb} \leq 60$ °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW class-AB	500	12.5	4	≥10	≥50

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A, and SNW-FQ-302B.

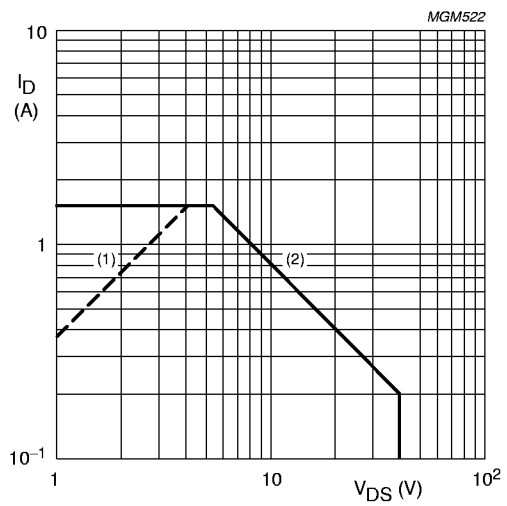
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	40	V
V_{GS}	gate-source voltage		–	±20	V
I_D	DC drain current		–	1.5	A
P_{tot}	total power dissipation	$T_{mb} \leq 85$ °C	–	8.3	W
T_{stg}	storage temperature		−65	150	°C
T_j	junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	$T_{mb} \leq 85$ °C, P_{tot} = 8.3 W	12.1	K/W



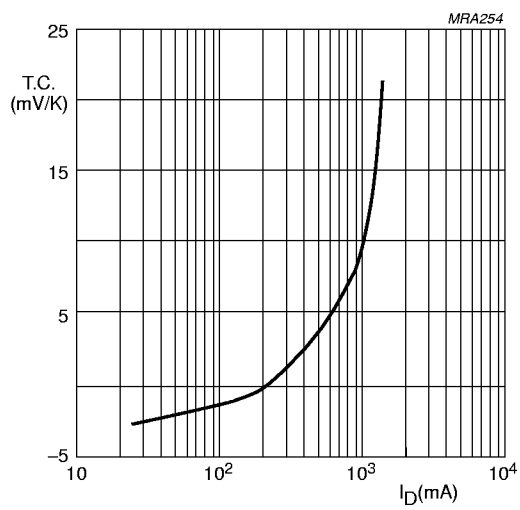
(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 85 °C.

Fig.2 DC SOAR.

CHARACTERISTICS

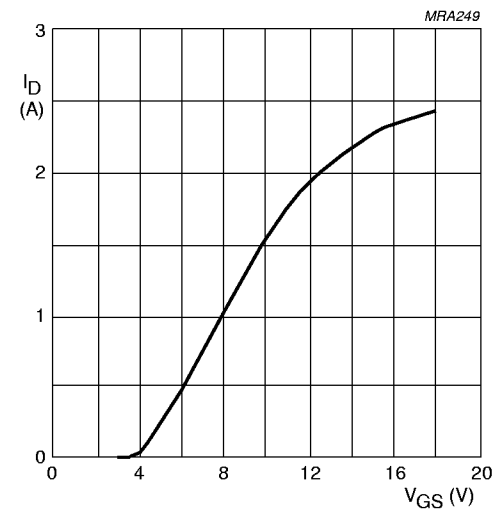
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 5 mA	40	–	–	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 12.5 V	–	–	0.5	mA
I_{GSS}	gate-source leakage current	V_{DS} = 0; V_{GS} = ±20 V	–	–	1	μA
I_{DSX}	on-state drain current	V_{GS} = 15 V; V_{DS} = 10 V	–	2.3	–	A
R_{DSon}	drain-source on-state resistance	I_D = 0.7 A; V_{GS} = 15 V	–	1.8	2.7	Ω
g_{fs}	forward transconductance	I_D = 0.7 A; V_{DS} = 10 V	200	270	–	mS
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	14	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	17	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 12.5 V; f = 1 MHz	–	3	–	pF



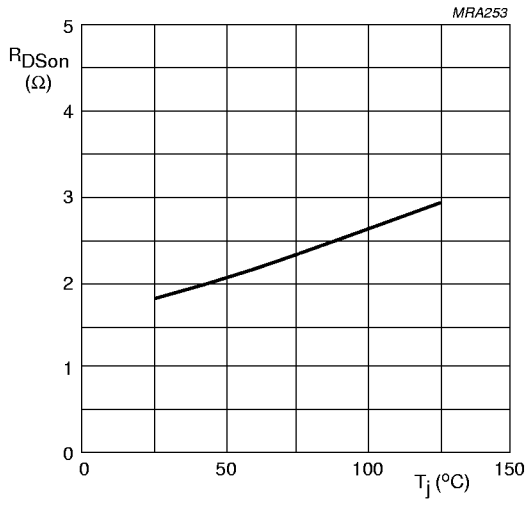
V_{DS} = 10 V.

Fig.3 Temperature coefficient of gate-source voltage as a function of drain current; typical values.



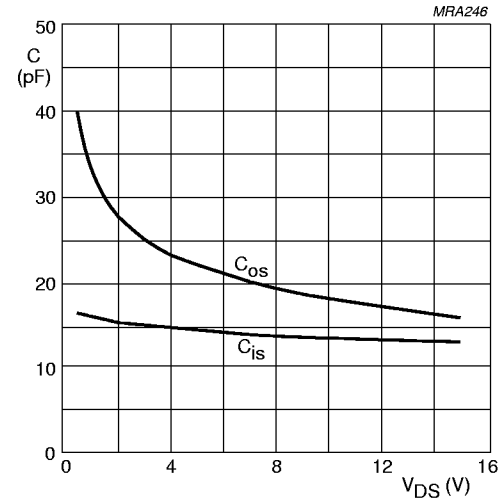
V_{DS} = 10 V; T_j = 25 °C.

Fig.4 Drain current as a function of gate-source voltage; typical values.



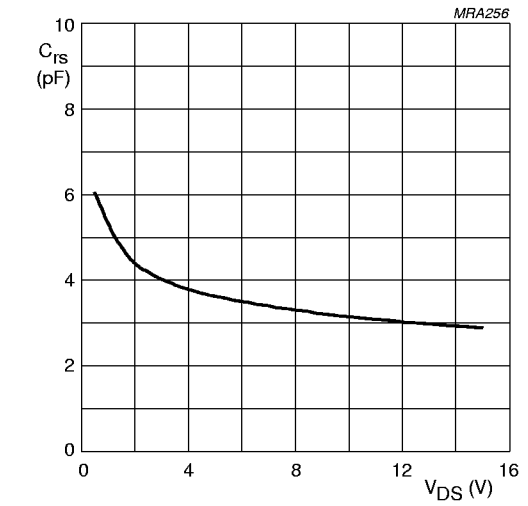
I_D = 0.7 A; V_{GS} = 15 V.

Fig.5 Drain-source on-state resistance as a function of junction temperature; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.6 Input and output capacitance as functions of drain-source voltage; typical values.



V_{GS} = 0; f = 1 MHz; T_j = 25 °C.

Fig.7 Feedback capacitance as a function of drain-source voltage; typical values.

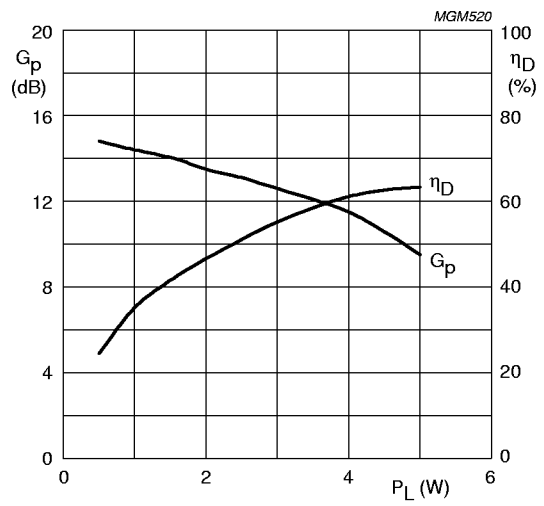
APPLICATION INFORMATION

RF performance at $T_{mb} \leq 60$ °C in a common source test circuit with the device soldered on a printed-circuit board with through metallized holes.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (A)	P_L (W)	G_p (dB)	η_D (%)
CW, class-AB	500	12.5	50	4	≥10 typ. 11.5	≥50 typ. 55

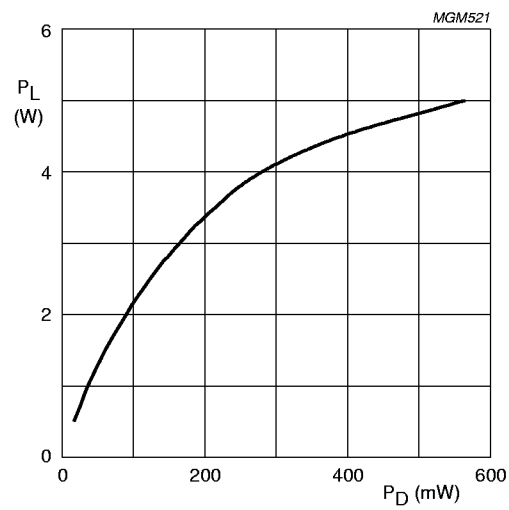
Ruggedness in class-AB operation

The BLF404 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: f = 500 MHz; V_{DS} = 12.5 V; P_L = 4 W; $T_{mb} \leq 60$ °C.



CW, class-AB operation; f = 500 MHz; V_{DS} = 12.5 V; I_{DQ} = 50 mA; $T_{mb} \leq 60$ °C.

Fig.8 Power gain and drain efficiency as functions of load power; typical values.



CW, class-AB operation; f = 500 MHz; V_{DS} = 12.5 V; I_{DQ} = 50 mA; $T_{mb} \leq 60$ °C.

Fig.9 Load power as a function of drive power; typical values.

Test circuit information

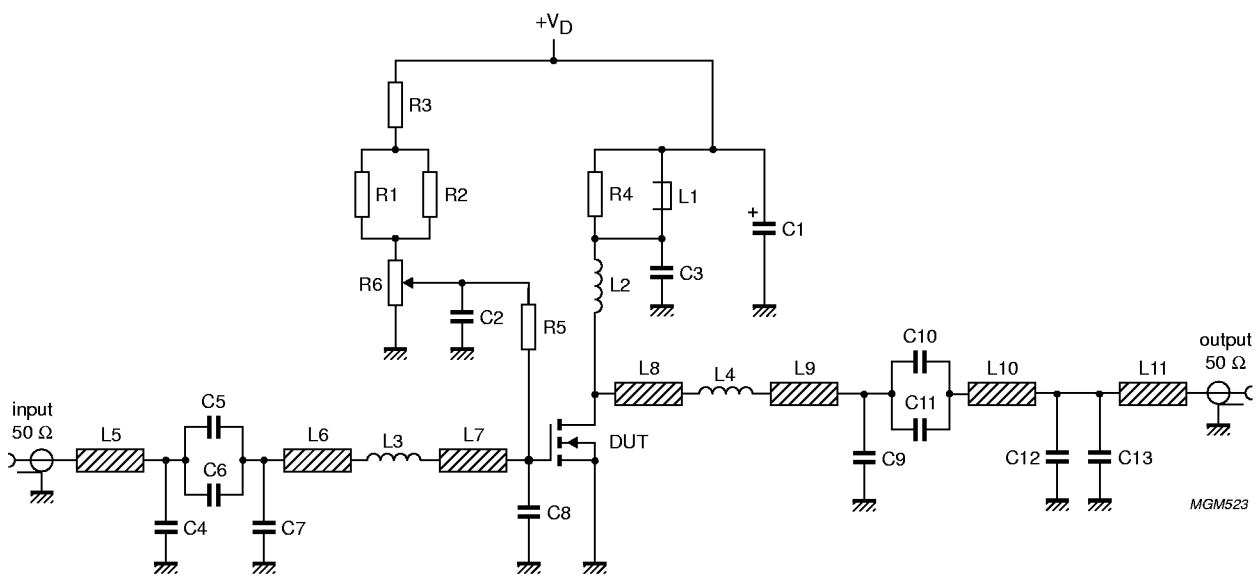


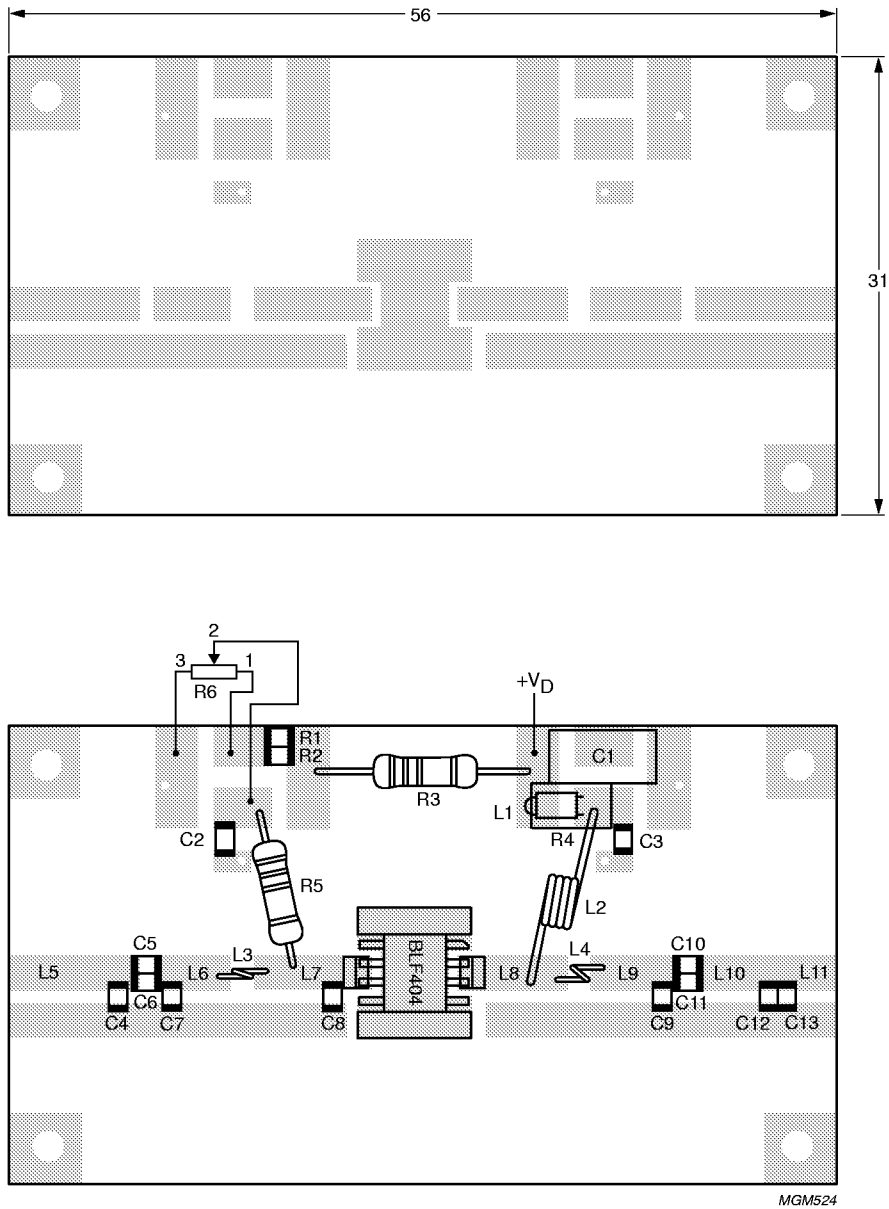
Fig.10 Class-AB common source test circuit at f = 500 MHz.

List of components used in test circuit (see Figs 10 and 11).

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1	electrolytic capacitor	4.7 μF, 10 V		
C2, C3	multilayer ceramic chip capacitor	47 nF		
C4	multilayer ceramic chip capacitor; note 1	18 pF		
C5, C10	multilayer ceramic chip capacitor; note 1	180 pF		
C6, C11	multilayer ceramic chip capacitor; note 1	270 pF		
C7	multilayer ceramic chip capacitor; note 1	22 pF		
C8	multilayer ceramic chip capacitor; note 1	8.2 pF		
C9	multilayer ceramic chip capacitor; note 1	2.7 pF		
C12	multilayer ceramic chip capacitor; note 1	1.2 pF		
C13	multilayer ceramic chip capacitor; note 1	12 pF		
L1	2 turns 1 mm enamelled copper wire on a grade 4B1 Ferroxcube core		ext. dia. = 4.2 mm int. dia. = 2 mm length = 6 mm	
L2	3 turns 1 mm enamelled copper wire		int. dia. = 4.6 mm leads = 2 x 5 mm	
L3	bifilar coil		lead dia. = 0.8 mm	
L4	bifilar coil		lead dia. = 1 mm	
L5	stripline; note 2	50 Ω	8.8 × 2.38 mm	
L6	stripline; note 2	50 Ω	5.8 × 2.38 mm	
L7	stripline; note 2	50 Ω	6.8 × 2.38 mm	
L8	stripline; note 2	50 Ω	3.76 × 2.38 mm	
L9	stripline; note 2	50 Ω	5.8 × 2.38 mm	
L10	stripline; note 2	50 Ω	4.48 × 2.38 mm	
L11	stripline; note 2	50 Ω	3.13 × 2.38 mm	
R1, R2	SMD resistor	3.9 kΩ		
R3	metal film resistor	1 kΩ, 0.25 W		
R4	metal film resistor	22 Ω, 0.25 W		
R5	metal film resistor	10 kΩ, 0.25 W		
R6	potentiometer	10 kΩ		

Notes

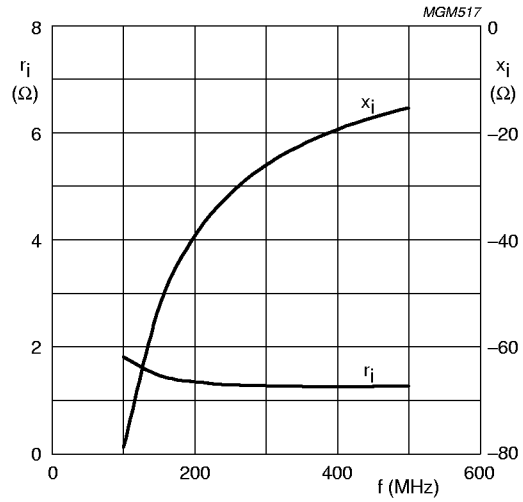
1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad printed circuit board, with DUROID dielectric (ε_r = 2.2); thickness 0.79 mm, thickness of the copper sheet 2 x 35 μm.



Dimensions in mm.

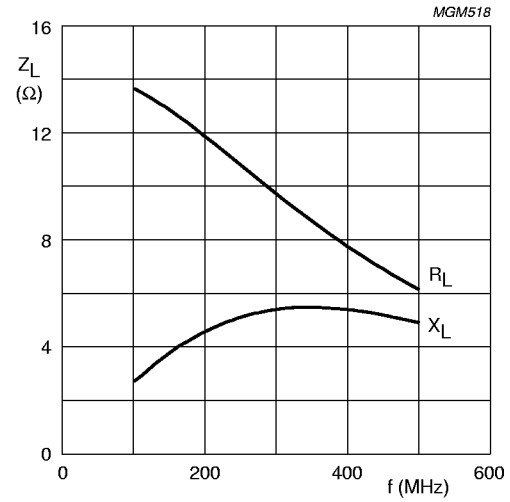
The components are situated on one side of the copper-clad printed-circuit board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.11 Printed-circuit board and component layout for 500 MHz class-AB test circuit in Fig.10.



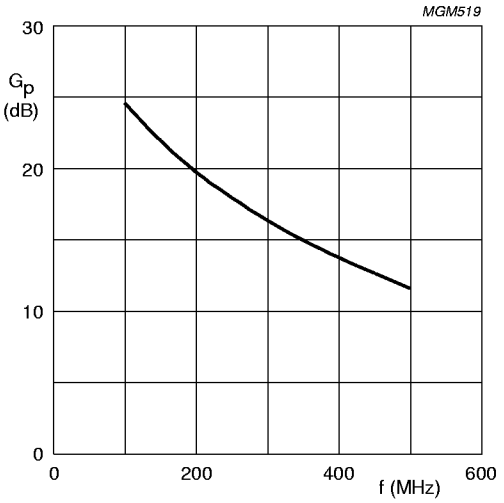
CW, class-AB operation; V_{DS} = 12.5 V; I_D = 50 mA;
P_L = 4 W; $T_{mb} \leq$ 60 °C.

Fig.12 Input impedance as a function of frequency (series components); typical values.



CW, class-AB operation; V_{DS} = 12.5 V; I_D = 50 mA;
P_L = 4 W; $T_{mb} \leq$ 60 °C.

Fig.13 Load impedance as a function of frequency (series components); typical values.

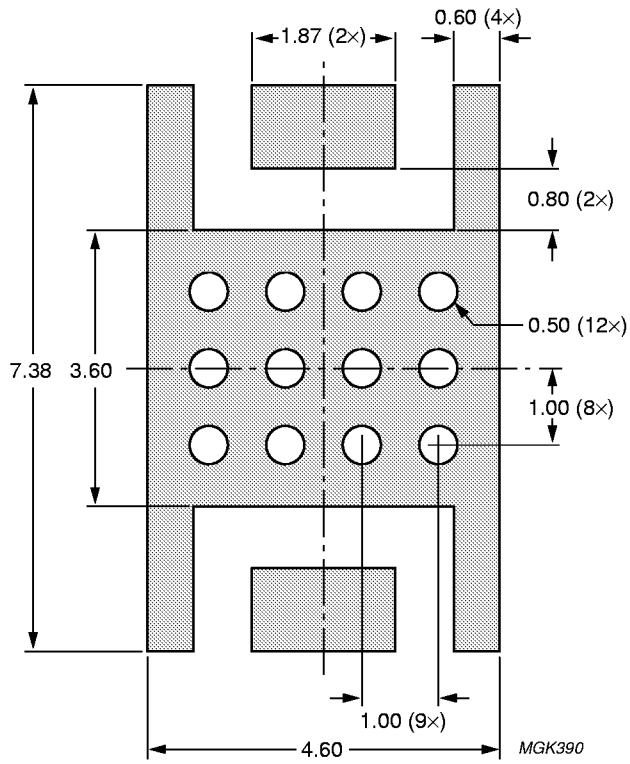


CW, class-AB operation; V_{DS} = 12.5 V; I_{DQ} = 50 mA;
P_L = 4 W; $T_{mb} \leq$ 60 °C.

Fig.14 Power gain as a function of frequency (series components); typical values.

MOUNTING RECOMMENDATIONS

Both the metallized groundplate and leads contribute to the heatflow. It is recommended that the transistor is mounted on a grounded metallized area of a maximum thickness of 0.8 mm on the printed-circuit board, equipped with at least 12 (0.5 mm diameter) through metallized holes filled with solder.
A thermal resistance $R_{th(mb-h)}$ of 5 K/W can be achieved if heatsink compound is applied when the transistor is mounted on the printed-circuit board.

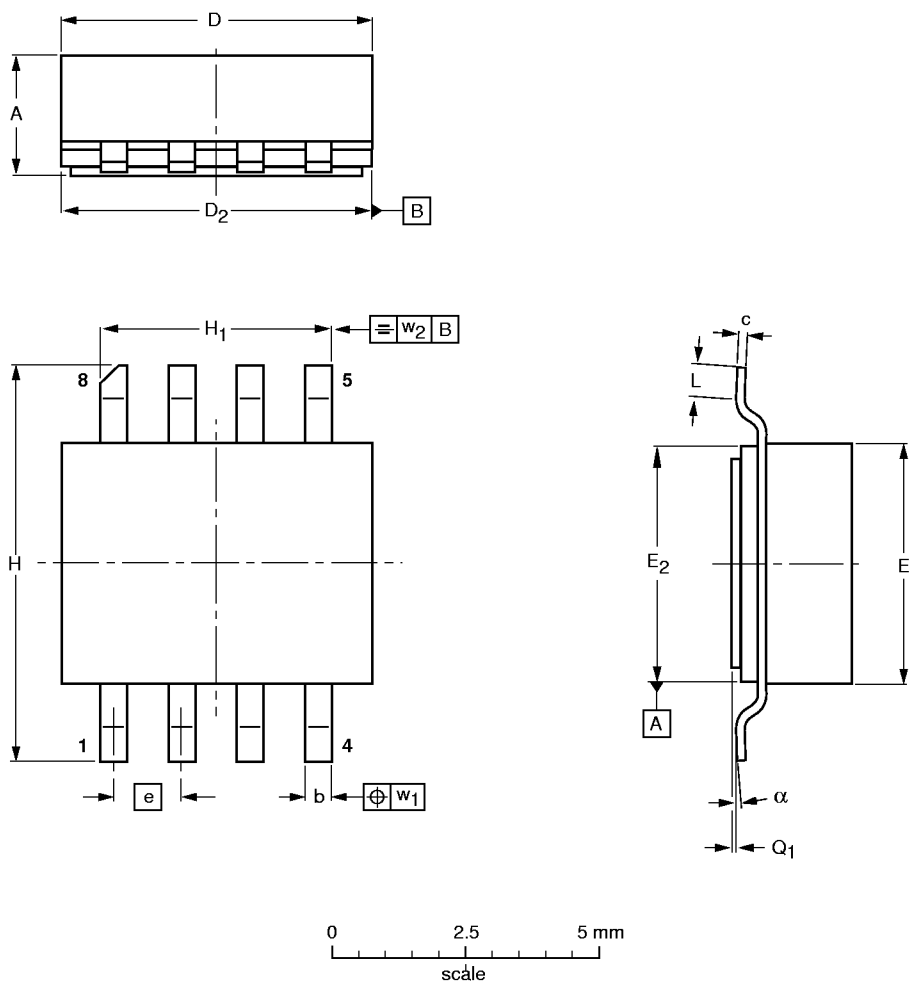


Dimensions in mm.

Fig.15 Reflow soldering footprint for SOT409A.

PACKAGE OUTLINE

Ceramic surface mounted package; 8 leads **SOT409A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_2	E	E_2	e	H	H_1	L	Q_1	w_1	w_2	α
mm	2.36 2.06	0.58 0.43	0.23 0.18	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	1.02 0.51	0.10 0.00	0.25	0.25	7° 0°
inches	0.093 0.081	0.023 0.017	0.009 0.007	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.040 0.020	0.004 0.000	0.010	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409A						98-01-27