REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
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SHEET	15																			

REV STATUS OF SHEETS	REV															
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
97-02-10

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, VARIABLE LENGTH SHIFT REGISTER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-96793

SHEET 1 OF 15

DESC FORM 193
JUL 94

5962-E081-97

DISTRIBUTION STATEMENT A. Approved for public release: distribution is unlimited.

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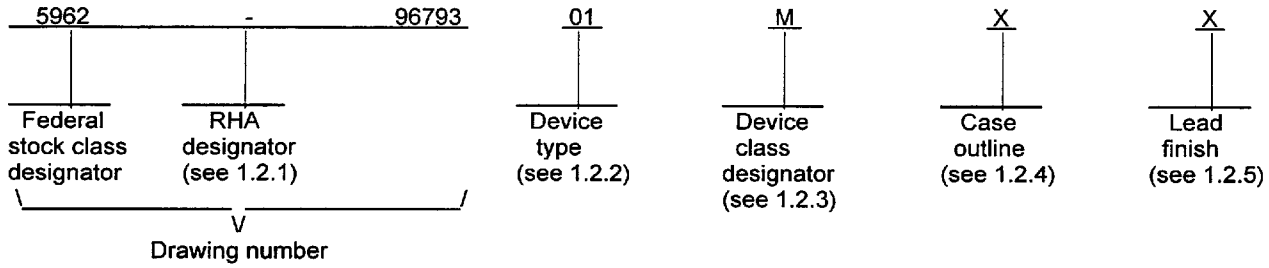
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Frequency
01	L10c11	4/8-bit variable length shift register	30 ns
02	L10c11	4/8-bit variable length shift register	25 ns
03	L10c11	4/8-bit variable length shift register	20 ns
04	L21c11	8-bit variable length shift register	30 ns
05	L21c11	8-bit variable length shift register	25 ns
06	L21c11	8-bit variable length shift register	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
L	GDIP3-T24	24	dual-in-line package
3	CQCC1-N28	28	leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

Storage Temperature	-65°C to +125°C
Supply voltage with respect to ground (V_{CC})	-0.5 V to +7.0 v
Input signal with respect to ground	-3.0 V to +7.0 V
Signal applied to high impedance output	-3.0 V to +7.0 V
Output current into low outputs	25 mA
Latchup current	> 400 mA
Thermal resitance Junction-to-case (Θ_{JC})	See MIL-STD-1835
Lead temperature (soldering, 10 seconds)	+275°C
Power dissipation (P_D)	250 mW
Maximum junction temperature	175°C

1.4 Recommended operating conditions.

Operating ambient temperature	-55°C to +125°C
Supply voltage range	4.5 V ≤ V_{CC} ≤ 5.5 V

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Control encoding. The control encoding table shall be as specified on figure 2.

3.2.4 Block diagram. The blockdiagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = Min, I_{OH} = 12 mA	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = Min, I_{OL} = 24 mA	1, 2, 3	All		0.5	V
Input high voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC}	V
Input low voltage	V_{IL}	2/	1, 2, 3	All	0	0.8	V
Input current	I_{CC}	$GND \le V_{IN} \le V_{CC}$ 3/	1, 2, 3	All	-20	+20	μA
Supply Current dynamic	I_{CC1}	4/, 5/	4, 5, 6	All		20	mA
Supply current quiescent	I_{CC2}	6/	1, 2, 3	All		1.0	mA
Input Capacitance	C_{IN}	See 4.4.1c	4	All			pF
Functional test		See 4.4.1b	7, 8	All			
Output delay	t_{PD}	7/, 8/	9, 10, 11	01,04 02,05 03,06		30 25 20	ns
Clock pulse width	t_{PW}	V_{CC} = 4.5 V See figure 3 7/, 8/	9, 10, 11	01,04 02,05 03,06	15 12 12		ns
Data setup time	t_{SD}	V_{CC} = 4.5 V See figure 3 7/, 8/	9, 10, 11	01,04 02,05 03,06	25 10 10		ns
Data hold time	t_{HD}	V_{CC} = 4.5 V See figure 3 7/, 8/	9, 10, 11	01,04 02,05 03,06	2 2 0		ns
L3-0, mode setup time	t_{SL}	V_{CC} = 4.5 V See figure 3 7/, 8/	9, 10, 11	01 02,03	25 10		ns
Length code setup time	t_{SL}	V_{CC} = 4.5 V See figure 3 7/, 8/	9, 10, 11	04 05,06	25 10		ns
L3-0, mode hold time	t_{HL}	V_{CC} = 4.5 V See figure 3 7/, 8/	9, 10, 11	01,02 03	2 0		ns
Length code hold time	t_{HL}	V_{CC} = 4.5 V See figure 3 7/, 8/	9, 10, 11	04,05 06	2 0		ns

See footnotes at end of table.

1/ All testing to be performed using worst case test conditions unless otherwise specified.

2/ This devices provides hard clamping of transient undershoot and overshoot. Input levels below ground or above V_{CC} will be clamped beginning at -0.6 V and V_{CC} +0.6 V. The devices can withstand indefinite operation with inputs in the range of -0.5 V to +7.0V. Devices operation will not be adversely affected, however, input current levels will be well in excess of 100 mA.

3/ These parameters are only tested at the high temperature extreme, which is the worst case for leakage current.

4/ Supply current for a given application can be accurately approximated by:

$$\frac{NCV^2F}{4}$$

where

N = total number of device outputs
C = capacitive load per output
V = supply voltage
F = clock frequency

5/ Tested with all outputs changing every cycle and no load, at a 5 MHz clock rate.

6/ Tested with all inputs within 0.1 V of V_{CC} or Ground, no load.

7/ AC specification are tested with input transition times less than 3 ns, output reference levels of 1.5 V (except t_{ENA}/t_{DIS} test), and input levels of nominally 0 to 3.0 V. Output loading may be a resistive divider which provides for specified I_{OH} and I_{OL} at an output voltage of V_{OH} min and V_{OL} max respectively. Alternatively, a diode bridge with upper and lower current source of I_{OH} and I_{OL} respectively, and a balancing voltage of 1.5 V may be used. Parasitic capacitance is 30 pF minimum, and may be distributed. For

t_{ENABLE} and $t_{DISABLE}$ measurements, the load current is increased to 10 mA to reduce the RC delay component of the measurement.

This device has high speed output capable of large instantaneous current pulses and fast turn-on/turn-off times. As a result,care must be exercised in the testing of the devices. The following measures are recommended:

a. A 0.1 μF ceramic capacitor should be installed between V_{CC} and Ground leads as close to the Devices Under Test (DUT) as possible. Similar capacitors should be installed between devices V_{CC} and the tester common, and device ground and tester common.

b. Ground and V_{CC} supply planes must be brought directly to the DUT socket or fingers.

c. Input voltages should be adjusted to compensate for inductive ground and V_{CC} noise to maintain request DUT input levels relative to the DUT ground pin.

8/ Each parameter is shown as a minimum or maximum value. Input requirements are specified from the point of view of the external system driving the chip. Setup time, for example, is specified as a minimum since the external system must supply at least that much time to meet the worst-case requirements of all parts. Responses from the internal circuitry are specified from the point of view of the device. Output delay, for example, is specified as a maximum since worst-case operation of any device always provides data within that time.

Device 01-03							
Case L							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D_0	7	V_{CC}	13	Y_7	19	L_3
2	D_1	8	CLK	14	Y_6	20	L_2
3	D_2	9	D_4	15	Y_5	21	Y_3
4	D_3	10	D_5	16	Y_4	22	Y_2
5	L_0	11	D_6	17	MODE	23	Y_1
6	L_1	12	D_7	18	GND	24	Y_0

Devices 04-06							
Case L							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	D_0	7	V_{CC}	13	Y_7	19	L_3
2	D_1	8	CLK	14	Y_6	20	L_2
3	D_2	9	D_4	15	Y_5	21	Y_3
4	D_3	10	D_5	16	Y_4	22	Y_2
5	L_0	11	D_6	17	GND	23	Y_1
6	L_1	12	D_7	18	GND	24	Y_0

Figure 1. Terminal connections.

Device 01-03							
Case 3							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Y_0	8	V_{CC}	15	Y_7	22	GND
2	D_0	9	CLK	16	Y_6	23	L_3
3	D_1	10	D_4	17	Y_5	24	L_2
4	D_2	11	NC	18	Y_4	25	NC
5	D_3	12	D_5	19	NC	26	Y_3
6	L_0	13	D_6	20	MODE	27	Y_2
7	L_1	14	D_7	21	GND	28	Y_1

Devices 04-06							
Case 3							
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	Y_0	8	V_{CC}	15	Y_7	22	GND
2	D_0	9	CLK	16	Y_6	23	L_3
3	D_1	10	D_4	17	Y_5	24	L_2
4	D_2	11	NC	18	Y_4	25	NC
5	D_3	12	D_5	19	NC	26	Y_3
6	L_0	13	D_6	20	GND	27	Y_2
7	L_1	14	D_7	21	GND	28	Y_1

FIGURE 1. Terminal connections. - Continued

Device type 01, 02, 03								Device type 04,05,06				
Length Code				Mode = 0 Delay		Mode = 1 Delay		Length Code				Delay
L3	L2	L1	LO	Y_{3-0}	Y_{7-4}	Y_{3-0}	Y_{7-4}	L3	L2	L1	L0	Y_{7-0}
0	0	0	0	3	3	3	18	0	0	0	0	1
0	0	0	1	4	4	4	18	0	0	0	1	2
0	0	1	0	5	5	5	18	0	0	1	0	3
0	0	1	1	6	6	6	18	0	0	1	1	4
0	1	0	0	7	7	7	18	0	1	0	0	5
0	1	0	1	8	8	8	18	0	1	0	1	6
0	1	1	0	9	9	9	18	0	1	1	0	7
0	1	1	1	10	10	10	18	0	1	1	1	8
1	0	0	0	11	11	11	18	1	0	0	0	9
1	0	0	1	12	12	12	18	1	0	0	1	10
1	0	1	0	13	13	13	18	1	0	1	0	11
1	0	1	1	14	14	14	18	1	0	1	1	12
1	1	0	0	15	15	15	18	1	1	0	0	13
1	1	0	1	16	16	16	18	1	1	0	1	14
1	1	1	0	17	17	17	18	1	1	1	0	15
1	1	1	1	18	18	18	18	1	1	1	1	16

Figure 2. Control encoding

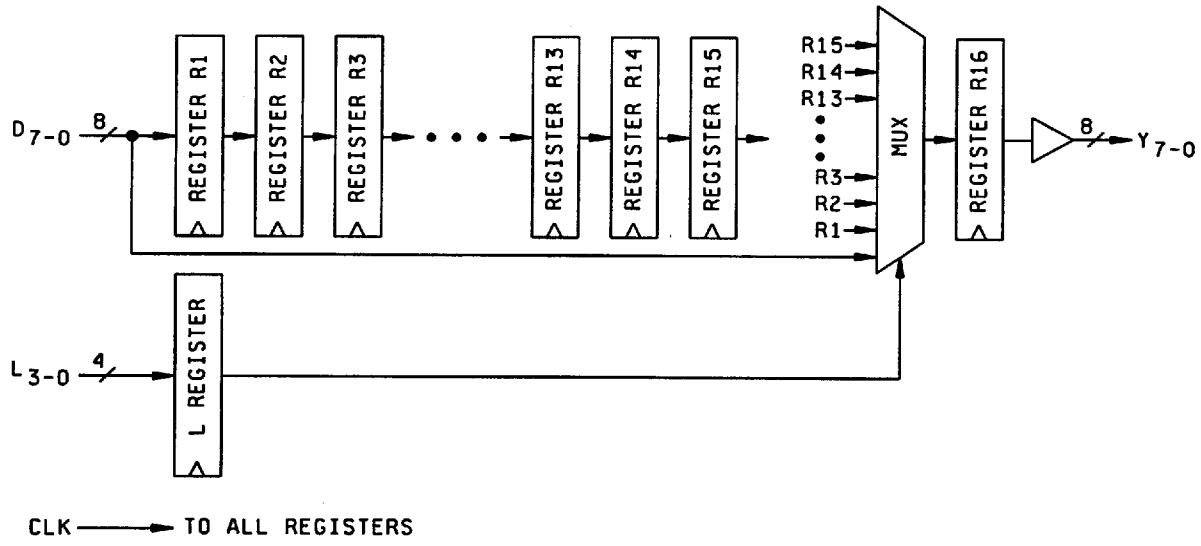


FIGURE 4. Block diagram.

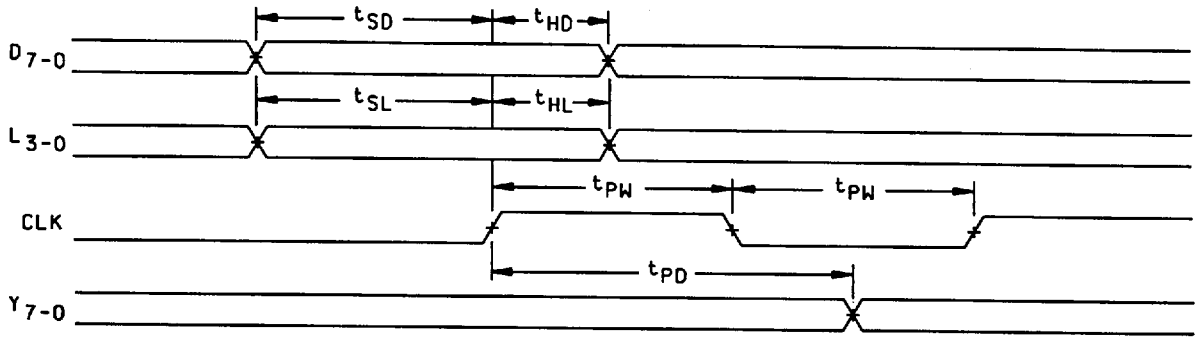


FIGURE 6. Timing waveforms.

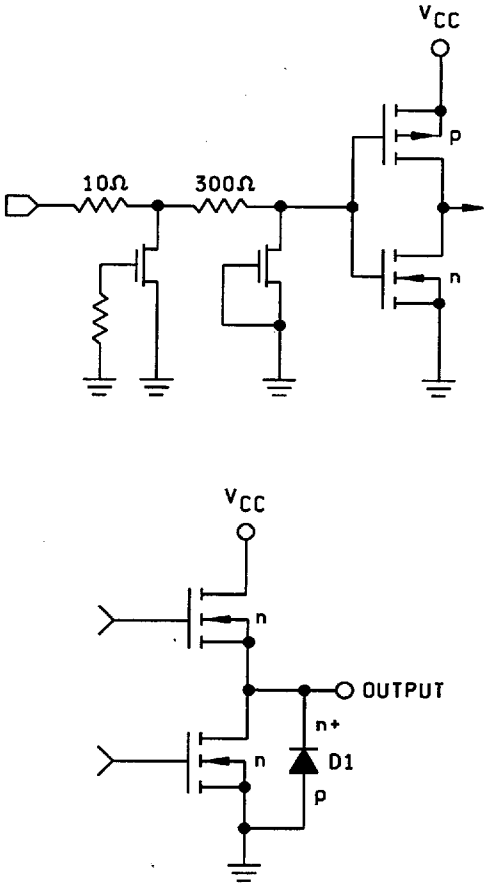


FIGURE 7. Switching waveforms and test circuit.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 040 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A . The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Sample size is five devices with zero rejects.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply CenterColumbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-02-10

Approved sources of supply for SMD 5962-96793 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9679301MLA	65896	L10C11CMB30
5962-9679301M3A	65896	L10C11KMB30
5962-9679301M3C	65896	L10C11KMB30
5962-9679302MLA	65896	L10C11CMB25
5962-9679302M3A	65896	L10C11KMB25
5962-9679302M3C	65896	L10C11KMB25
5962-9679303MLA	65896	L10C11CMB20
5962-9679303M3A	65896	L10C11KMB20
5962-9679303M3C	65896	L10C11KMB20
5962-9679304MLA	65896	L21C11CMB30
5962-9679304M3A	65896	L21C11KMB30
5962-9679304M3C	65896	L21C11KMB30
5962-9679305MLA	65896	L21C11CMB25
5962-9679305M3A	65896	L21C11KMB25
5962-9679305M3C	65896	L21C11KMB25
5962-9679306MLA	65896	L21C11CMB20
5962-9679306M3A	65896	L21C11KMB20
5962-9679306M3C	65896	L21C11KMB20

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65896	Logic Device Incorporated 628 E. Evelyn Ave Sunnyvale, CA. 94086

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.