REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R270-92.	92-08-07	M. L. Poelking
B	Redrawn with changes. Added device type 02. Editorial changes throughout.	94-02-22	M. L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

CURRENT CAGE CODE 67268

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REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	A	A	A	A	B	B	
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	

PMIC N/A	PREPARED BY Marcia B. Kelleher	DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444
STANDARDIZED MILITARY DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Thomas J. Ricciuti	MICROCIRCUITS, DIGITAL, CMOS, QUAD BILATERAL SWITCH, MONOLITHIC SILICON
	APPROVED BY Michael A. Frye	
	DRAWING APPROVAL DATE 90-10-15	SIZE **A** CAGE CODE **14933** **5962-90640**
	REVISION LEVEL B	SHEET 1 OF 13

DESC FORM 193
JUL 91

5962-E428-93

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1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

5962-90640	01	C	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	4016B	Quad bilateral switch
02	14016B	Quad bilateral switch

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings.

Supply voltage range (V_{DD}):	
Device type 01	-0.5 V dc to +20 V dc
Device type 02	-0.5 V dc to +18 V dc
Input voltage range (V_{IN})	-0.5 V dc to V_{DD} + 0.5 V dc
DC input current	±10 mA
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D) 1/	500 mW dc
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}):	
Device type 01	+3.0 V dc to +18 V dc
Device type 02	+3.0 V dc to +15 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ For T_C = +100 to +125°C, derate linearly at 12 mW/°C to 200 mW.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Intergrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.2.4 Logic diagram(s). The logic diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits Min	Limits Max	Unit
Quiescent supply current	I_{DD}	$V_{DD} = 5$ V 1/ $V_{IN} = 0.0$ V or V_{DD}		All	1, 3		0.25	µA
					2		7.5	
		$V_{DD} = 10$ V 1/ $V_{IN} = 0.0$ V or V_{DD}		All	1, 3		0.5	
					2		15	
		$V_{DD} = 15$ V 1/ $V_{IN} = 0.0$ V or V_{DD}		All	1, 3		1	
					2		30	
		$V_{DD} = 20$ V $V_{IN} = 0.0$ V or V_{DD} 2/		01	1, 3		5	
					2		150	
Low level output voltage	V_{OL}	$V_{IN} = 0.0$ V or V_{DD} $\lvert I_O \rvert < 1$ µA	$V_{CC} = 5$ V 1/	02	1, 2, 3		0.05	V
			$V_{CC} = 10$ V 1/		1, 2, 3		0.05	
			$V_{CC} = 15$ V		1, 2, 3		0.05	
High level output voltage	V_{OH}	$V_{IN} = 0.0$ V or V_{DD} $\lvert I_O \rvert < 1$ µA	$V_{CC} = 5$ V 1/	02	1, 2, 3	4.95		
			$V_{CC} = 10$ V 1/		1, 2, 3	9.95		
			$V_{CC} = 15$ V		1, 2, 3	14.95		
Low level input voltage, control inputs	V_{IL}	$V_{DD} = 5$ V $\lvert I_{IL} \rvert < 10$ µA	$V_{IN} = GND$, $V_{OUT} = V_{DD}$, and $V_{IN} = V_{DD}$ $V_{OUT} = GND$	01	1 2 3		0.7 0.4 0.9	
				02	1, 2, 3		0.9	
		$V_{DD} = 10$ V $\lvert I_{IL} \rvert < 10$ µA 1/	$V_{IN} = GND$, $V_{OUT} = V_{DD}$, and $V_{IN} = V_{DD}$ $V_{OUT} = GND$	01	1 2 3		0.7 0.4 0.9	
				02	1, 2, 3		0.9	
		$V_{DD} = 15$ V $\lvert I_{IL} \rvert < 10$ µA	$V_{IN} = GND$, $V_{OUT} = V_{DD}$, and $V_{IN} = V_{DD}$ $V_{OUT} = GND$	01	1 2 3		0.7 0.4 0.9	
				02	1, 2, 3		0.9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
High level input voltage, control	V_{IH}	V_{DD} = 5 V	01	1, 2, 3	3.5		V
			02		3.0		
		V_{DD} = 10 V 1/	01	1, 2, 3	7.0		
			02		8.0		
		V_{DD} = 15 V	01	1, 2, 3	11.0		
			02		13.0		
Low level output current	I_{OL}	V_{DD} = 5 V 3/ V_{OUT} = 0.4 V V_{IN} = 0.0 V or V_{DD}	02	1	0.51		mA
				2	0.36		
				3	0.64		
		V_{DD} = 10 V 1/ V_{OUT} = 0.5 V V_{IN} = 0.0 V or V_{DD}	02	1	1.3		
				2	0.9		
				3	1.6		
		V_{DD} = 15 V 1/ V_{OUT} = 1.5 V V_{IN} = 0.0 V or V_{DD}	02	1	3.4		
				2	2.4		
				3	4.2		
High level output current	I_{OH}	V_{DD} = 5 V 3/ V_{OUT} = 4.6 V V_{IN} = 0.0 V or V_{DD}	02	1	-0.51		mA
				2	-0.36		
				3	-0.64		
		V_{DD} = 5 V 3/ V_{OUT} = 2.5 V V_{IN} = 0.0 V or V_{DD}	02	1	-1.6		
				2	-1.15		
				3	-2.0		
		V_{DD} = 10 V 1/ V_{OUT} = 9.5 V V_{IN} = 0.0 V or V_{DD}	02	1	-1.3		
				2	-0.9		
				3	-1.60		
		V_{DD} = 15 V 1/ V_{OUT} = 13.5 V V_{IN} = 0.0 V or V_{DD}	02	1	-3.4		
				2	-2.4		
				3	-4.2		
Input current	I_{IN}	V_{DD} = 20 V 2/ V_{IN} = 0.0 V or V_{DD}	01	1,3		±0.1	µA
				2		±1.0	
		V_{DD} = 15 V V_{IN} = 0.0 V or V_{DD}	02	1, 3		±0.1	µA
				2		±1.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Input capacitance	C_{IN}	V_{DD} = GND See 4.3.1c		All	4		7.5	pF
Functional test		See 4.3.1d		All	7, 8			
Propagation delay time, input to output	t_{PHL}, t_{PLH}	R_L = 200 kΩ (01) R_L = 10 kΩ (02) C_L = 50 pF $t_r = t_f$ = 20 ns $V_{CONTROL} = V_{DD}$ $V_{IN} = V_{DD}$ (square wave centered on $V_{DD}/2$) See figure 4	V_{DD} = 5 V	All	9	1.5 4/	100	ns
					10, 11	1.5 4/	160	
			V_{DD} = 10 V 1/		9	1.5 4/	40	
					10, 11	1.5 4/	64	
			V_{DD} = 15 V 1/		9	1.5 4/	30	
					10, 11	1.5 4/	48	
Propagation delay time, control input to switch output (turn on)	t_{PHZ}, t_{PLZ}, t_{PZH}, t_{PZL}	R_L = 1 kΩ C_L = 50 pF $t_r = t_f$ = 20 ns See figure 5	V_{DD} = 5 V	All	9	1.5 4/	70	
					10, 11	1.5 4/	112	
			V_{DD} = 10 V 1/		9	1.5 4/	40	
					10, 11	1.5 4/	64	
			V_{DD} = 15 V 1/		9	1.5 4/	30	
					10, 11	1.5 4/	48	
On-state resistance	R_{ON}	$V_{CONTROL} = V_{DD}$ R_L = 10 kΩ returned to V_{DD} - GND/2	V_{DD} = 10 V $V_{IN} = V_{DD}$ or GND	All	1 2 3		660 960 600	Ω
			V_{DD} = 10 V V_{IN} = 4.75 V to 5.75 V		1 2 3		2000 2600 1870	
			V_{DD} = 15 V $V_{IN} = V_{DD}$ or GND		1 2 3		400 600 360	
			V_{DD} = 15 V V_{IN} = 7.25 V to 7.75 V		1 2 3		850 1230 775	
Delta on-state resistance between any two switches	delta R_{ON}	$V_{CONTROL} = V_{DD}$ R_L = 10 kΩ 1/ V_{SS} = 0.0 V	V_{DD} = 5 V	01	1		15	Ω
			V_{DD} = 10 V	01	1		15	
				02	1		15	
			V_{DD} = 15 V	01	1		10	
				02	1		10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Input/output leakage current	I_{IS}	$V_{CONTROL} = 0$ V $V_{IN} = 18$ V $V_{OUT} = 0$ V	All	1, 3		±0.1	µA
				2		±1.0	
(Switch off)		$V_{CONTROL} = 0$ V $V_{IN} = 0$ V $V_{OUT} = 18$ V	All	1, 3		±0.1	µA
				2		±1.0	

1/ This parameter is guaranteed, if not tested, to the specified limits in table I for device 01 only.

2/ At -55°C test is performed with V_{DD} at 18 volts.

3/ The I_{OL} and I_{OH} tests are tested 100 percent at $T_C = +25°C$, and are guaranteed, if not tested, for $T_C = -55°C$ and $T_C = +125°C$.

4/ The minimum limit for device type 01 only = 1.5 ns.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) $T_A = +125°C$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

Device type	01 and 02
Case outline	C
Terminal number	Terminal symbol
1	INPUT/OUTPUT SIG A
2	OUTPUT/INPUT SIG A
3	OUTPUT/INPUT SIG B
4	INPUT/OUTPUT SIG B
5	CONTROL B
6	CONTROL C
7	GND
8	INPUT/OUTPUT SIG C
9	OUTPUT/INPUT SIG C
10	OUTPUT/INPUT SIG D
11	INPUT/OUTPUT SIG D
12	CONTROL D
13	CONTROL A
14	V_{CC}

FIGURE 1. Terminal connections.

Truth table each switch		
Input		Output
$V_{CONTROL}$	V_{IN}	V_{OUT}
H	L	L
H	H	H
L	L	OPEN
L	H	OPEN

H = High voltage level
L = Low voltage level

Positive logic: Switch on $V_{CONTROL}$ = High
Switch off $V_{CONTROL}$ = Low

FIGURE 2. Truth table.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90640
		REVISION LEVEL A	SHEET 8

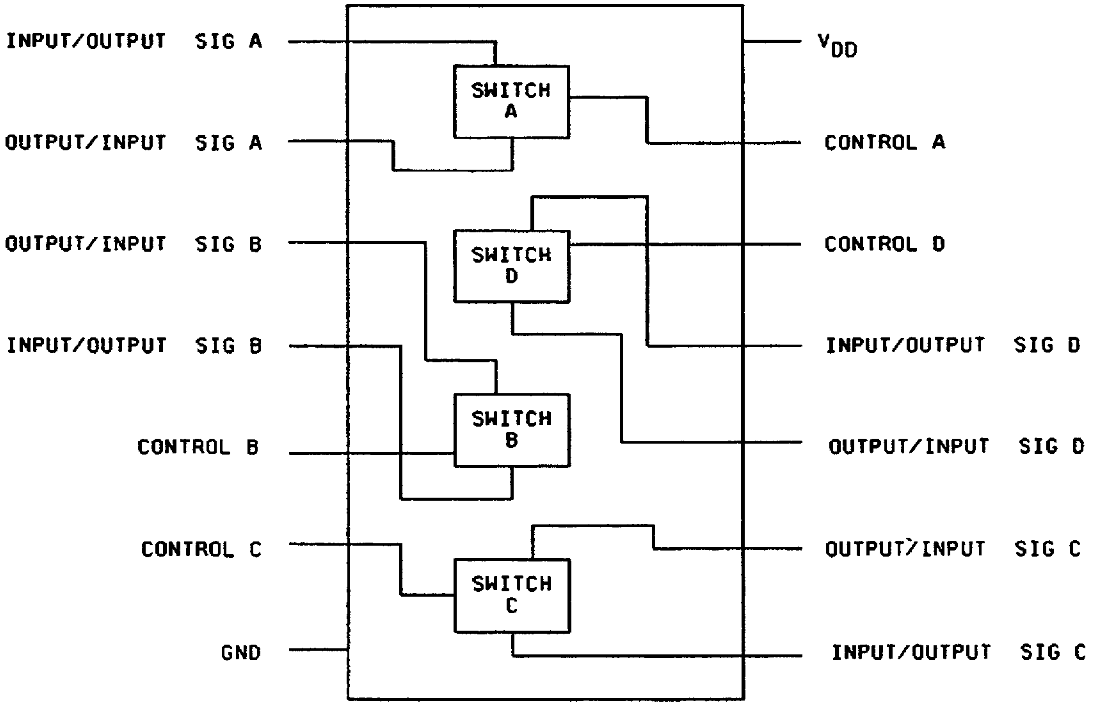
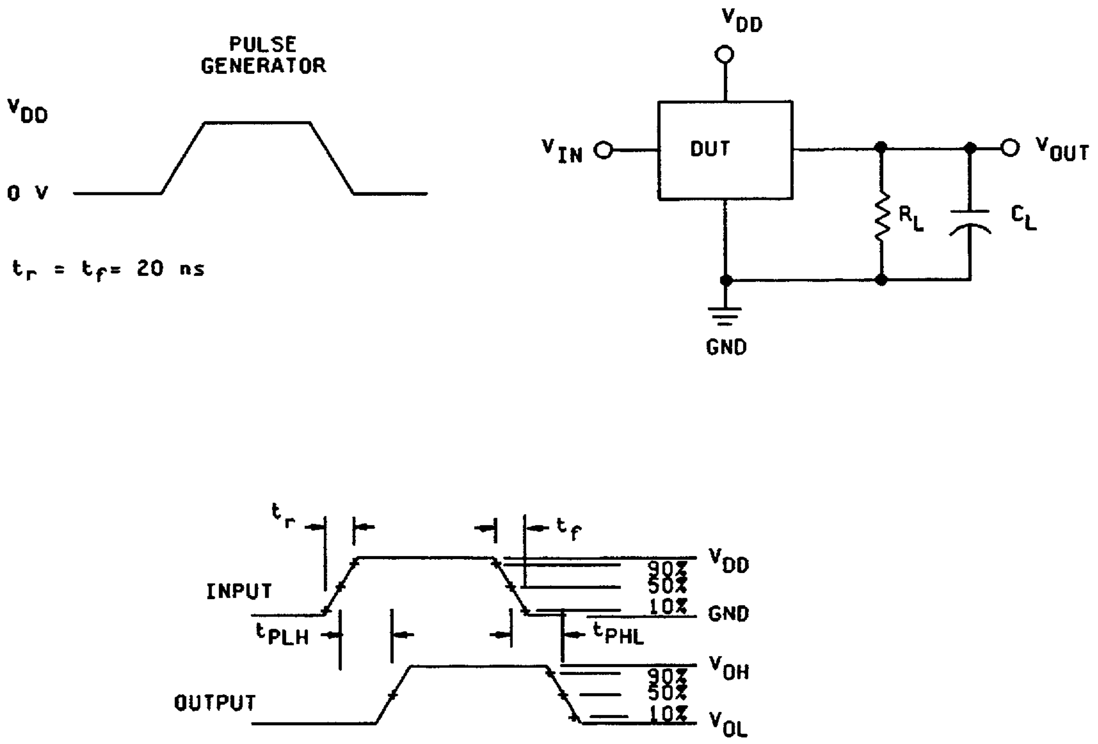


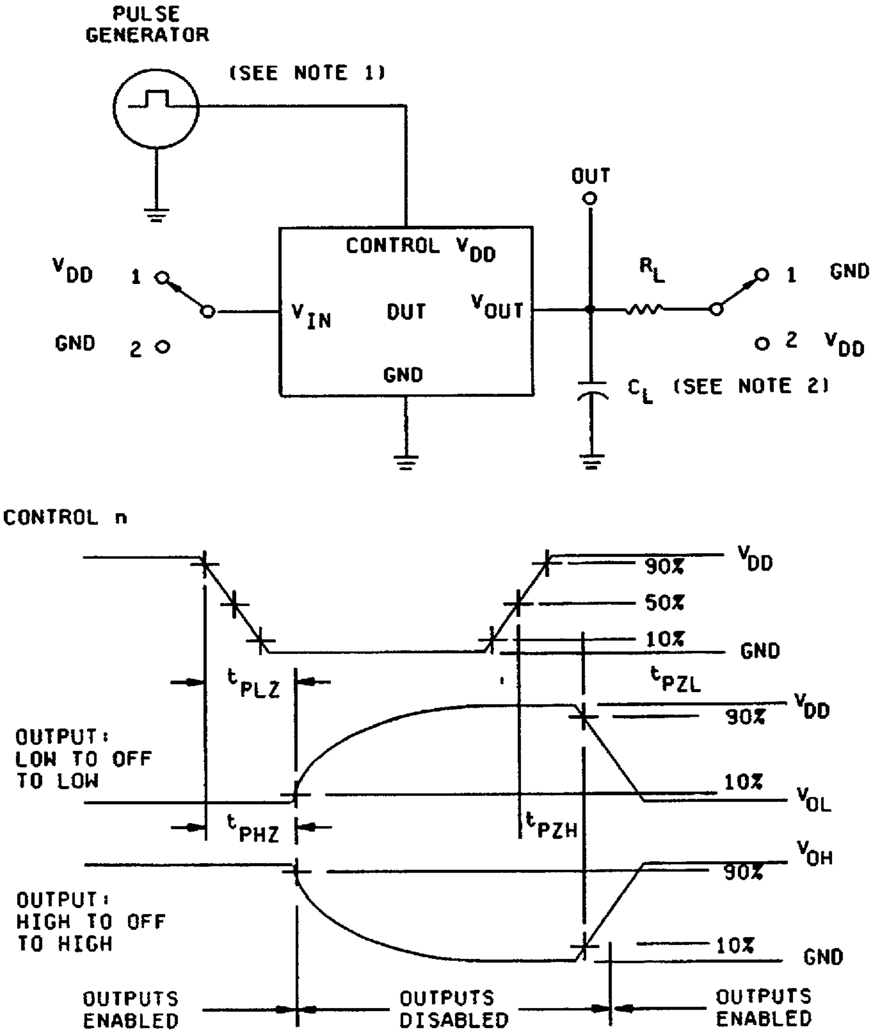
FIGURE 3. Logic diagram.



NOTES:

1. Pulse generator conditions: $V_{GEN} = V_{DD}$ ±1 percent, duty cycle - 50 percent, t_r and t_f = 20 ns ±2.0 ns.
2. C_L = 50 pF, R_L = 200 kΩ, includes probe and jig capacitance.
3. Identical switching measurements are obtained from switch A, switch B, switch C, and switch D.

FIGURE 4. Switching test circuit and waveforms, switch input to switch output.



NOTES:

1. Pulse generator characteristics: $V_{GEN} = V_{DD}$ ±1 percent; duty cycle = 50 percent; t_r, t_f = 20 ns and $Z_{OUT} = 50\Omega$.
2. C_L = 50 pF, R_L = 1 kΩ, includes probe and jig capacitance.
3. Identical switching measurements are obtained from switch A, switch B, switch C, and switch D.
4. Switch position 1 for t_{PZH} and t_{PHZ} tests; switch position 2 for t_{PLZ} and t_{PZL} tests.

FIGURE 5. Switching test circuit and waveforms, switch control input to switch output.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 9
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10**, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.
** Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. Capacitance shall be measured between the designated terminal and GND or at a frequency of 1 MHz . Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 shall include verification of the truth table as specified on figure 2 herein.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistic purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using Form DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.