REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. Add case outline M. Add V_{IL2} and V_{IH2} to table I. Add block diagram for device types 03 and 04. Editorial changes throughout.	92-07-09	Monica L. Poelking
B	Add new programming configuration to Figure 7. Changes to table I. Editorial changes throughout.	93-04-19	Monica L. Poelking
C	Add device types 05 and 06. Editorial changes throughout.	94-09-14	Monica L. Poelking

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED

REV																			
SHEET																			
REV	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27						

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Jeffery Tunstall

CHECKED BY Thomas Hess

APPROVED BY Monica Poelking

DRAWING APPROVAL DATE 91-20-11

REVISION LEVEL C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, CHMOS, SINGLE-CHIP, 8-BIT MICROCONTROLLER WITH 16K BYTES OF EPROM PROGRAM MEMORY, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-90564
A	67268	

SHEET 1 OF 27

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	87C51FB-12	High performance CHMOS single-chip 8-bit microcontroller
02	87C51FB-16	High performance CHMOS single-chip 8-bit microcontroller
03	87C654	High performance CHMOS single-chip 8-bit microcontroller
04	87C654-16	High performance CHMOS single-chip 8-bit microcontroller
05	87C654	High performance CHMOS single chip 8-bit microcontroller with 16K bytes of one time programable EPROM memory (3.5 to 12 MHz
06	87C654-16	High performance CHMOS single-chip 8-bit microcontroller with 16K bytes of one time programable EPROM memory (3.5 to 16 MHz

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
M	GQCC1-J44 or CQCC2-J44	44	ceramic chip carrier "J" leaded package 1/
T	See figure 1	44	ceramic chip carrier, "J" leaded package) 1/
U	CQCCQ-N44	44	square chip carrier package 1/
X	GDIP1-T40 or CDIP2-T40	40	dual-in-line package 1/
Z	See figure 2	44	ceramic chip carrier, gull wing leaded package 1/

1.2.3 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein). Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ For device types 01, 02, 03, and 04, lid shall be transparent to permit ultraviolet light erasure.

1.3 Absolute maximum ratings.

Storage temperature range	-65°C to +150°C
Voltage on EA/V_{PP} pin to V_{SS} range	0 V to +13.0 V
Voltage on any other pin to V_{SS} range	-0.5 V to +6.5 V
Maximum I_{OL} per I/O pin	15 mA
Power dissipation (P_D)	1.5 W 2/
Lead temperature (soldering, 10 seconds)	+265°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases M, U and X	See MIL-STD-1835
Cases T and Z	14°C/W
Data retention	10 years

1.4 Recommended operating conditions.

Case operating temperature range (T_C)	-55°C to +125°C 3/
Supply voltage (V_{CC})	5.0 V ±10 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and bulletin. Unless otherwise specified, the following specification, standards, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

2/ Based on package heat transfer limitations, not device power consumption.
3/ Case temperatures are "instant on".

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-I-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-I-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-I-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein anf figures 1 and 2.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.3 Block diagram(s). The block diagram(s) shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.9.1 Processing EPROMS. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.9.2 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.4.

3.9.3 Programmability of EPROMS. When specified, devices shall be programmed to the specified pattern using the procedures and characteristics specified in 4.5 and table III.

3.9.4 Verification of erasure of programmability of EPROMS. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10%; V_{SS} = 0 V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}	1/	1, 2, 3	All	2/ -0.5	$0.2 V_{CC} - 0.1$	V
Input low voltage $\overline{EA}$	V_{IL1}	1/	1, 2, 3	03,04, 05,06	2/ 0	$0.2 V_{CC} - 0.45$	V
Input low voltage to P1.6/SCL, P1.7/SDA	V_{IL2}	1/	1, 2, 3	03,04, 05,06	-0.5	$0.3 V_{CC}$	V
Input high voltage (except XTAL1, RST)	V_{IH}	1/	1, 2, 3	All	$0.2 V_{CC} + .9$	$V_{CC} + 0.5$ 2/	V
Input high voltage (XTAL1, RST)	V_{IH1}	1/	1, 2, 3	All	$0.7 V_{CC}$	$V_{CC} + 0.5$ 2/	V
Input high voltage to P1.6/SCL, P1.7/SDA	V_{IH2}	1/	1, 2, 3	03,04, 05,06	$0.7 V_{CC}$	6.0	V
Output low voltage (ports 1, 2, and 3) 3/	V_{OL}	I_{OL} = 100 µA V_{CC} = 4.5 V I_{OL} = 1.6 mA I_{OL} = 3.5 mA 4/	1, 2, 3	All		0.3 0.45 1.0	V
Output low voltage (port 0, ALE, PSEN) 3/	V_{OL1}	I_{OL} = 200 µA V_{CC} = 4.5 V I_{OL} = 3.2 mA I_{OL} = 7.0 mA 4/	1, 2, 3	All		0.3 0.45 1.0	V
Output high voltage (Ports 1, 2, and 3) (except P1.6 and P1.7) 3/	V_{OH}	I_{OH} = -10 µA V_{CC} = 4.5 V I_{OH} = -30 µA I_{OH} = -60 µA	1, 2, 3	All	$V_{CC}-0.3$ $V_{CC}-0.7$ $V_{CC}-1.5$		V
Output high voltage (Port 0 in external bus mode, ALE, PSEN)	V_{OH1}	I_{OH} = -200 µA V_{CC} = 4.5 V I_{OH} = -3.2 mA 5/ I_{OH} = -7.0 mA	1, 2, 3	All	$V_{CC}-0.3$ $V_{CC}-0.7$ $V_{CC}-1.5$		V
Logical 0 input current (ports 1, 2, and 3)	I_{IL}	V_{IN} = 0.45 V	1, 2, 3	All		-75	µA
Input leakage current (port 0)	I_{LI}	$0.45 < V_{IN} < V_{CC}$	1, 2, 3	All	-10	+10	µA
Logical 1-to-0 transition current (ports 1, 2, and 3)	I_{TL}	V_{IN} = 2.0 V	1, 2, 3	All		-750	µA
RST pulldown resistor	R_{RST}		1, 2, 3	All	40	225	kΩ

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$; $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Pin capacitance 2/	C_{IN}	At 1 MHz, +25°C, see 4.3.1c	4	All		10	pF
Power supply current:	I_{CC}	6/ 7/	1, 2, 3				
Running at 16 MHz				All		45	mA
Idle mode 16 MHz				All		15	mA
Power down mode				01,02		130	µA
Power down mode				03,04, 05,06		200	µA
Functional tests		See 4.3.1e	7, 8				
ALE pulse width	t_{LHLL}	Load capacitance for port 0, ALE/PROG and PSEN = 100 pF, load capacitance for all other outputs = 80 pF See figure 5 1/ 8/	9, 10, 11	01,02	$2t_{CLCL-40}$		ns
				03,04, 05,06	$2t_{CLCL-55}$		
Address valid to ALE low	t_{AVLL}		9, 10, 11	All	$t_{CLCL-40}$		ns
Address hold after ALE low	t_{LLAX}		9, 10, 11	01,02	$t_{CLCL-30}$		ns
				03,04, 05,06	$t_{CLCL-50}$		
ALE low to valid instruction in	t_{LLIV}		9, 10, 11	01-02		$4t_{CLCL-100}$	ns
				03-06		$4t_{CLCL-110}$	
ALE low to $\overline{PSEN}$ low	t_{LLPL}		9, 10, 11	01,02	$t_{CLCL-30}$		ns
				03,04, 05,06	$t_{CLCL-55}$		
$\overline{PSEN}$ pulse width	t_{PLPH}		9, 10, 11	01,02	$3t_{CLCL-45}$		ns
				03,04, 05,06	$3t_{CLCL-50}$		
$\overline{PSEN}$ low to valid instruction in	t_{PLIV}		9, 10, 11	All		$3t_{CLCL-105}$	ns
Input instruction hold after PSEN	t_{PXIX}		9, 10, 11	All	0		ns
Input instruction float after PSEN	t_{PXIZ}		9, 10, 11	All		$t_{CLCL-25}$	ns
Address to valid instruction in	t_{AVIV}		9, 10, 11	01,02		$5t_{CLCL-105}$	ns
				03,04, 05,06		$5t_{CLCL-140}$	
$\overline{PSEN}$ low to address float	t_{PLAZ}		9, 10, 11	All		20	ns
$\overline{RD}$ pulse width	t_{RLRH}		9, 10, 11	All	$6t_{CLCL-100}$		ns
$\overline{WR}$ pulse width	t_{WLWH}		9, 10, 11	All	$6t_{CLCL-100}$		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$; $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RD}$ low to valid data in	t_{RLDV}	Load capacitance for port 0, ALE/PROG and PSEN = 100 pF, load capacitance for all other outputs = 80 pF See figure 5 1/	9, 10, 11	01,02		$5t_{CLCL}-165$	ns
				03,04 05,06		$5t_{CLCL}-175$	
Data hold after $\overline{RD}$	t_{RHDX}		9, 10, 11	All	0		ns
Data float after $\overline{RD}$	t_{RHDZ}		9, 10, 11	01,02		$2t_{CLCL}-60$	ns
				03,04 05,06		$2t_{CLCL}-85$	
ALE low to valid data in	t_{LLDV}		9, 10, 11	01,02		$8t_{CLCL}-150$	ns
				03,04 05,06		$8t_{CLCL}-170$	
Address to valid data in	t_{AVDV}		9, 10, 11	01,02		$9t_{CLCL}-185$	ns
				03,04 05,06		$9t_{CLCL}-185$	
ALE low to $\overline{RD}$ or $\overline{WR}$ low	t_{LLWL}		9, 10, 11	All	$3t_{CLCL}-50$	$3t_{CLCL}+50$	ns
Address valid to $\overline{WR}$ low	t_{AVWL}		9, 10, 11	All	$4t_{CLCL}-130$		ns
Data valid before $\overline{WR}$	t_{QVWX}		9, 10, 11	All	$t_{CLCL}-50$		ns
Data hold after $\overline{WR}$	t_{WHQX}		9, 10, 11	All	$t_{CLCL}-50$		ns
Data valid to $\overline{WR}$ high	t_{QVWH}		9, 10, 11	All	$7t_{CLCL}-150$		ns
$\overline{RD}$ low to address float	t_{RLAZ}		9, 10, 11	All		0	ns
$\overline{RD}$ or $\overline{WR}$ high to ALE high	t_{WHLH}		9, 10, 11	All	$t_{CLCL}-40$	$t_{CLCL}+40$	ns
Serial port clock cycle time	t_{XLXL}	Serial port timing - shift register mode load capacitance = 80 pF See figure 5	9, 10, 11	All	$12t_{CLCL}$		ns
Output data setup to clock rising edge	t_{QVXH}		9, 10, 11	All	$10t_{CLCL}-133$		ns
Output data hold after clock rising edge	t_{XHQX}		9, 10, 11	All	$2t_{CLCL}-117$		ns
Input data hold after clock rising edge	t_{XHDX}		9, 10, 11	All	0		ns
Clock rising edge to input data valid	t_{XHDV}		9, 10, 11	All		$10t_{CLCL}-133$	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5.0\ V \pm 10\%$; $V_{SS} = 0\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Oscillator frequency	1/ $1/t_{CLCL}$	External clock drive	9, 10, 11	01,03, 05	3.5	12	MHz
		See figure 5		02,04, 06	3.5	16	
High time	t_{CHCX}		9, 10, 11	All	20		ns
Low time	t_{CLCX}		9, 10, 11	All	20		ns
Rise time 2/	t_{CLCH}		9, 10, 11	All		20	ns
Fall time 2/	t_{CHCL}		9, 10, 11	All		20	ns

1/ Timings tested at 16 MHz only but guaranteed across the specified operating frequency range. Devices not meeting the limits of the 16 MHz devices may be retested to be supplied at the slower 12 MHz speed grade.
2/ Guaranteed to the limits specified in table I, if not tested.
3/ Under steady-state (nontransient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA.
Maximum I_{OL} per 8-bit port: Port 0: 26 mA.
Ports 1, 2, and 3: 15 mA.
Maximum total I_{OL} for all output pins: 71 mA.
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
4/ Capacitive loading on ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and ports 1 and 3. The noise is due to external bus capacitance discharging into the port 0 and port 2 pins when these pins make 1 to 0 transitions during bus operations. In applications where capacitance loading exceeds 100 pF, the noise pulse on the ALE signal may exceed 0.8 V. In these cases, it may be desirable to qualify ALE with Schmitt Trigger, or use an Address Latch with a Schmitt Trigger Strobe input.
5/ Capacitive loading on ports 0 and 2 cause the V_{OH} on ALE and PSEN to drop below the $.9V_{CC}$ specification when the address lines are stabilizing.
6/ Minimum V_{CC} for power down is 2 V.
7/ I_{CC} is measured with all output pins and XTAL2 disconnected; XTAL1 driven with t_{CLCH}. t_{CHCL} = 5 ns, $V_{IL} = V_{SS} + 0.5\ V$, $V_{IH} = V_{CC} - 0.5\ V$ measured with EA and RST connected to V_{CC}. "Idle" and "power down" currents measured with EA and RST connected to V_{SS}. "Power down" currents measured with XTAL1 connected to V_{SS}.
8/ Due to test equipment limitations, actual tested values may differ from those specified, but specified limits are guaranteed.

Case T

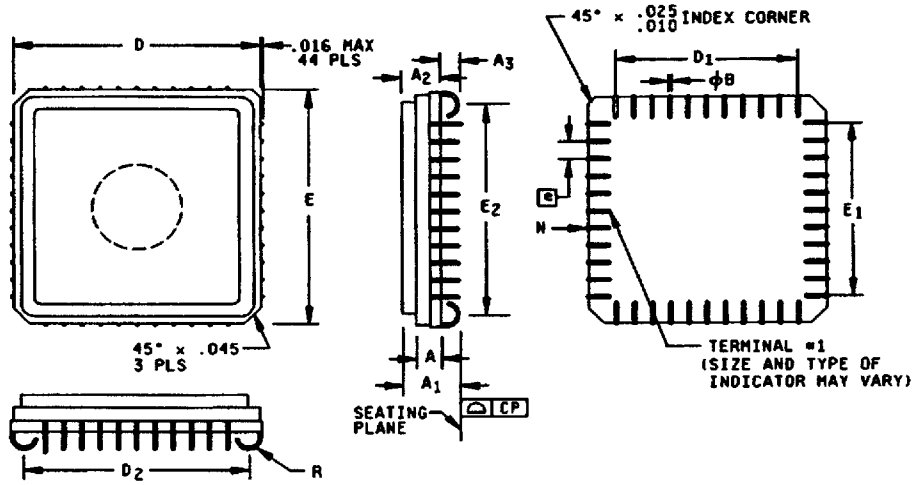

FIGURE 1. Ceramic chip carrier, "J" leaded package.

Family: Ceramic leadless chip carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.52	2.23		.060	.088	
A_1	3.25	4.55		.128	.170	
A_1	3.99	5.08	EPROM lid	.157	.200	EPROM lid
A_2	1.85	2.59		.073	.102	
A_2	2.59	3.40	EPROM lid	.102	.134	EPROM lid
A_3	1.40	1.65		.055	.065	
B	0.35	0.46		.014	.018	
CP	0.00	0.10		.000	.004	
D	16.25	17.02		.640	.670	
D_1	12.70		Reference	.500		Reference
D_2	15.24			.600		
E	16.25	17.02		.640	.670	
E_1	12.70		Reference	.500		Reference
E_2	15.24			.600		
|e|	1.12	1.42		.044	.056	
N	44			44		
R	0.69	0.84		.027	.033	

FIGURE 1. Ceramic chip carrier, "J" leaded package - Continued.

Case Z

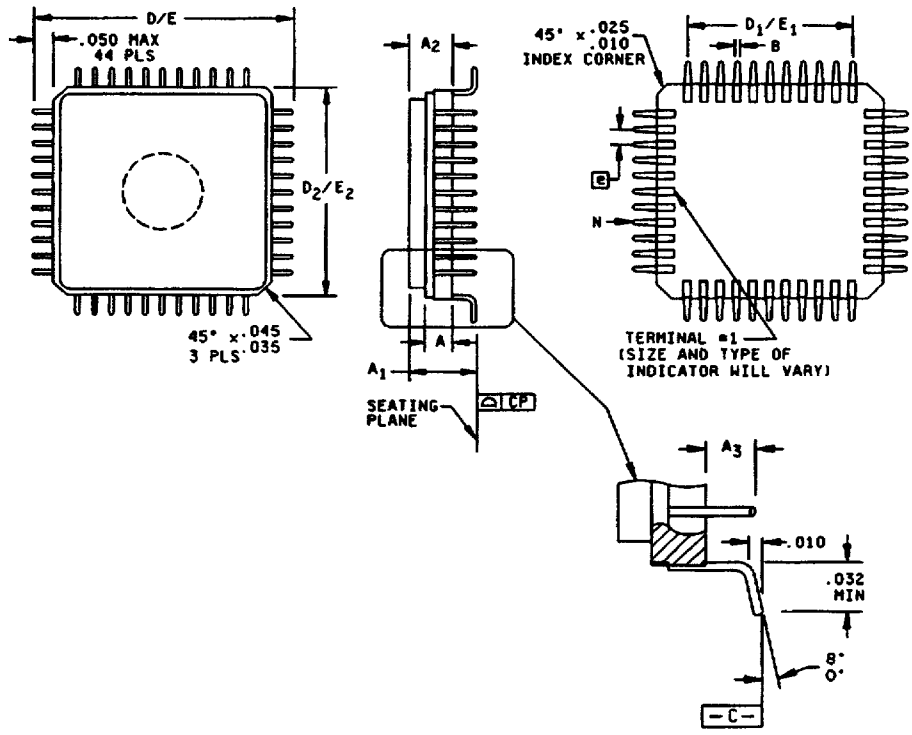

FIGURE 2. Ceramic chip carrier, gull wing leaded package.

Family: Ceramic leadless chip carrier						
Symbol	Millimeters			Inches		
	Min	Max	Notes	Min	Max	Notes
A	1.52	2.29		.060	.090	
A_1	3.25	4.32		.128	.170	
A_1	3.99	5.08	EPROM lid	.157	.200	EPROM lid
A_2	1.85	2.59		.073	.102	Solid lid
A_2	2.59	3.40	EPROM lid	.102	.134	EPROM lid
A_3	1.40	1.65		.055	.065	
B	0.35	0.46		.014	.018	
CP	0.00	0.10		.000	.004	
D	18.19	19.00		.716	.748	
D_1	12.70		Reference	.500		Reference
D_2	16.25	16.76		.640	.660	Solid lid
E	18.19	19.00		.716	.748	
E_1	12.70		Reference	.500		Reference
E_2	16.25	16.76		.640	.660	
|e|	1.12	1.42		.044	.056	
N	44			44		

FIGURE 2. Ceramic chip carrier, gull wing leaded package - Continued.

Case X

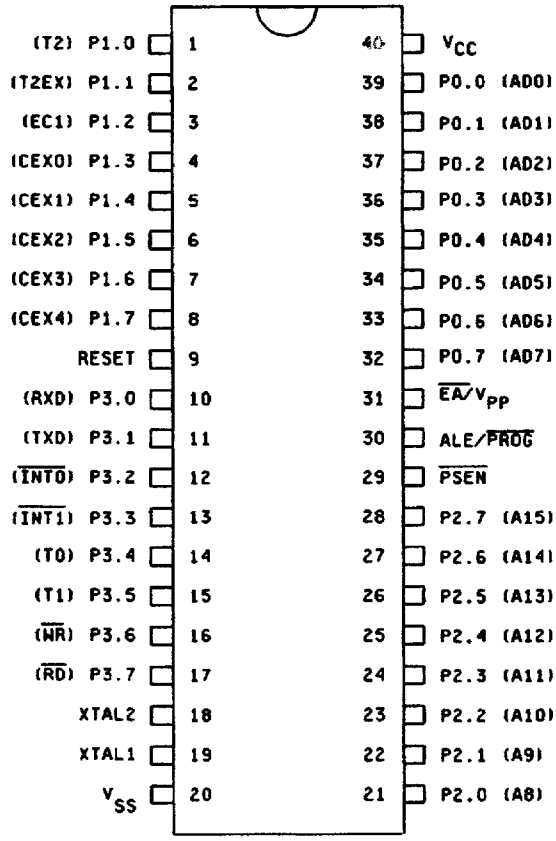

FIGURE 3. Terminal connections.

Cases M, T, U, and Z

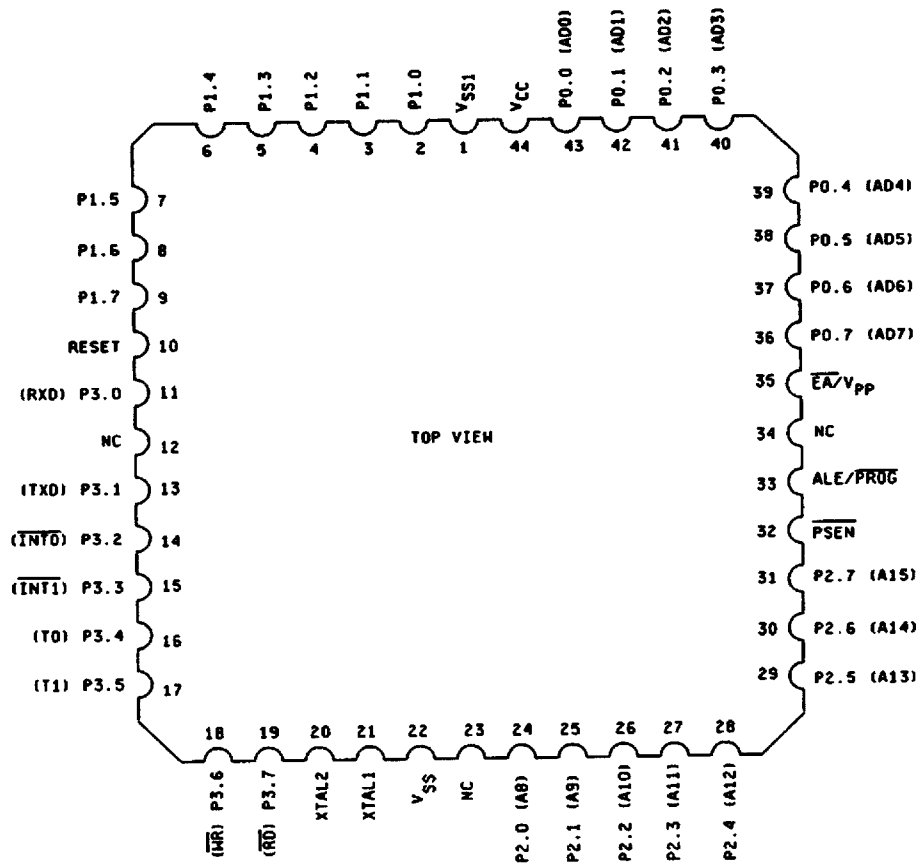

FIGURE 3. Terminal connections - Continued.

Device types 01 and 02

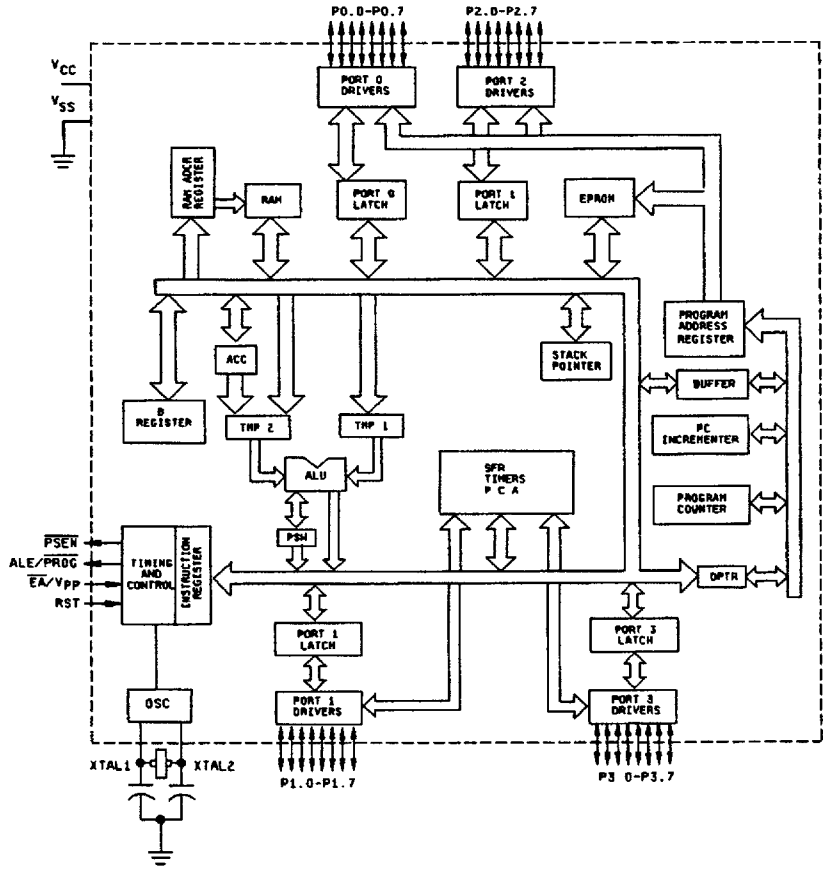

FIGURE 4. Block diagram.

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		REVISION LEVEL C	SHEET 15

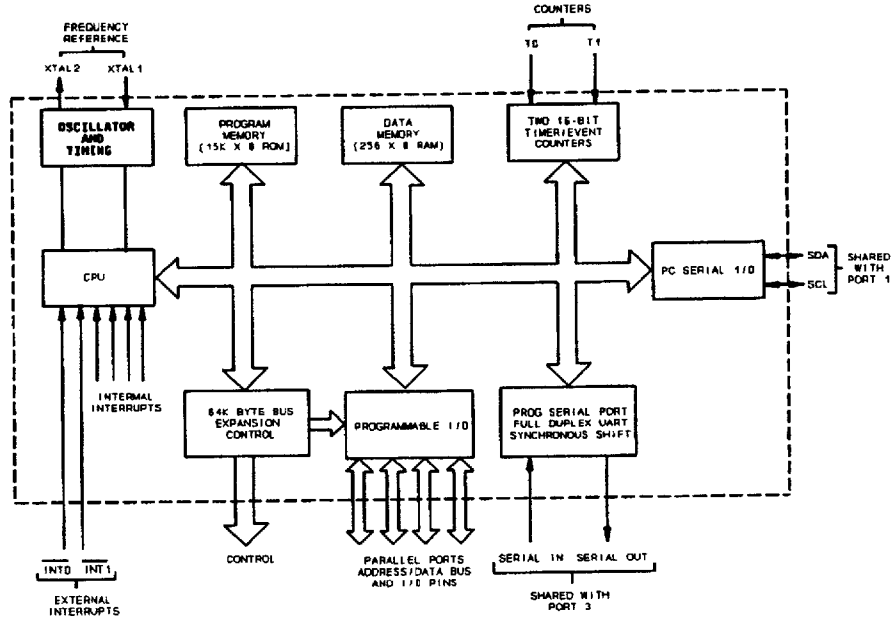
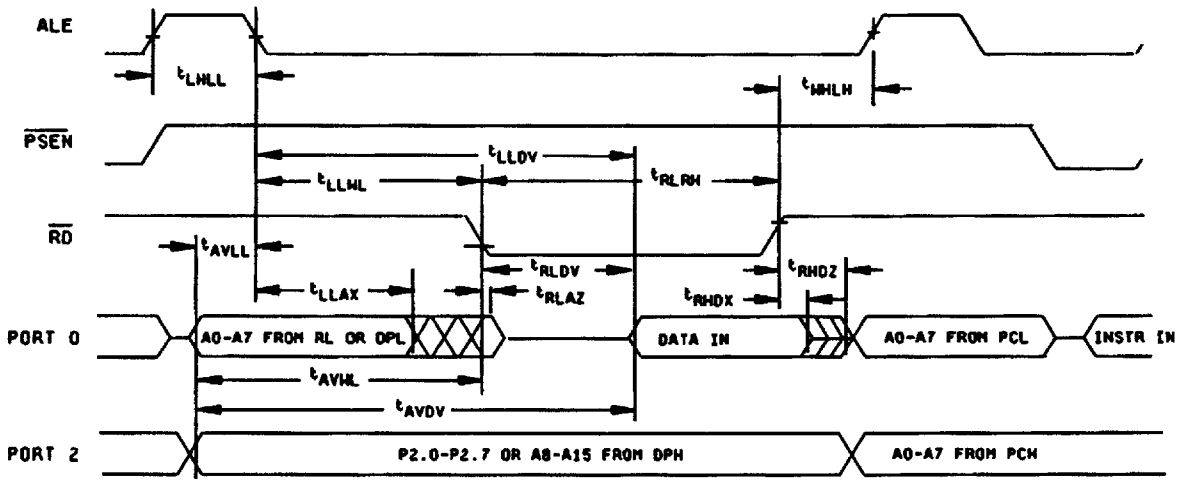


FIGURE 4. Block diagram - continued

External program memory read cycle



External program memory read cycle

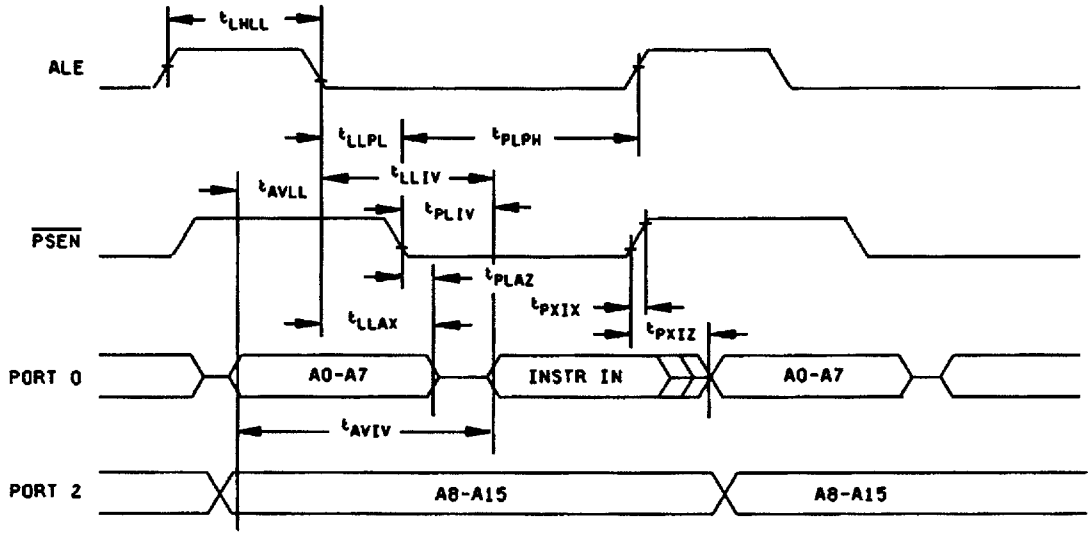
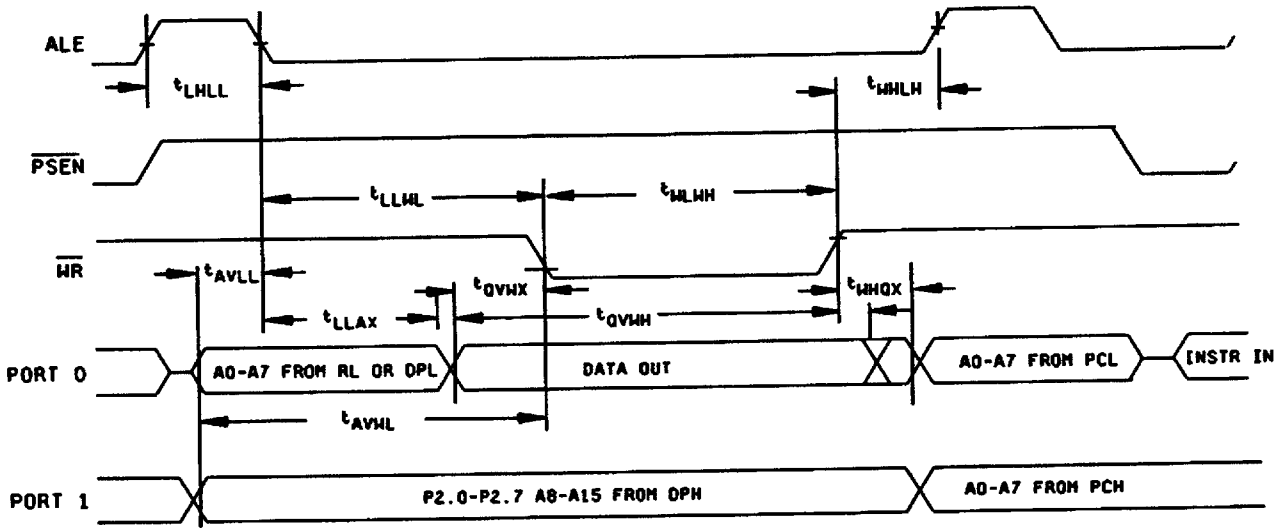


FIGURE 5. Timing waveform and test circuit.

External data memory write cycle



External clock drive waveform

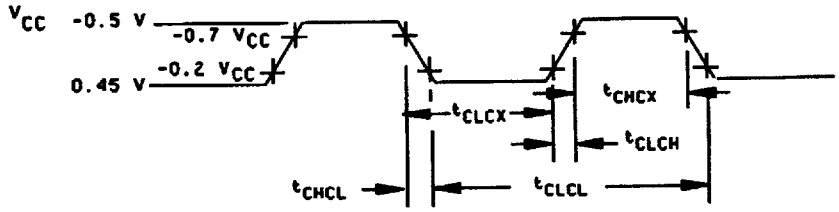
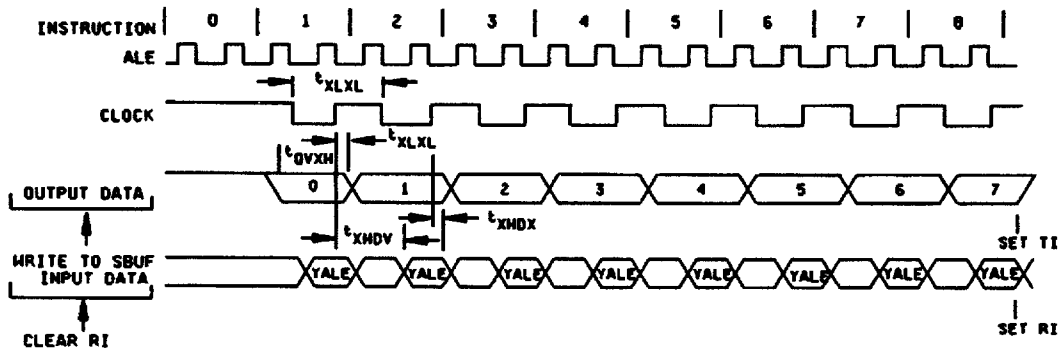


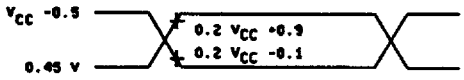
FIGURE 5. Timing waveform and test circuit - continued

Shift register mode timing waveforms

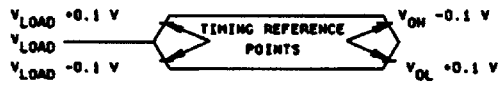


AC testing input

INPUT, OUTPUT WAVEFORMS



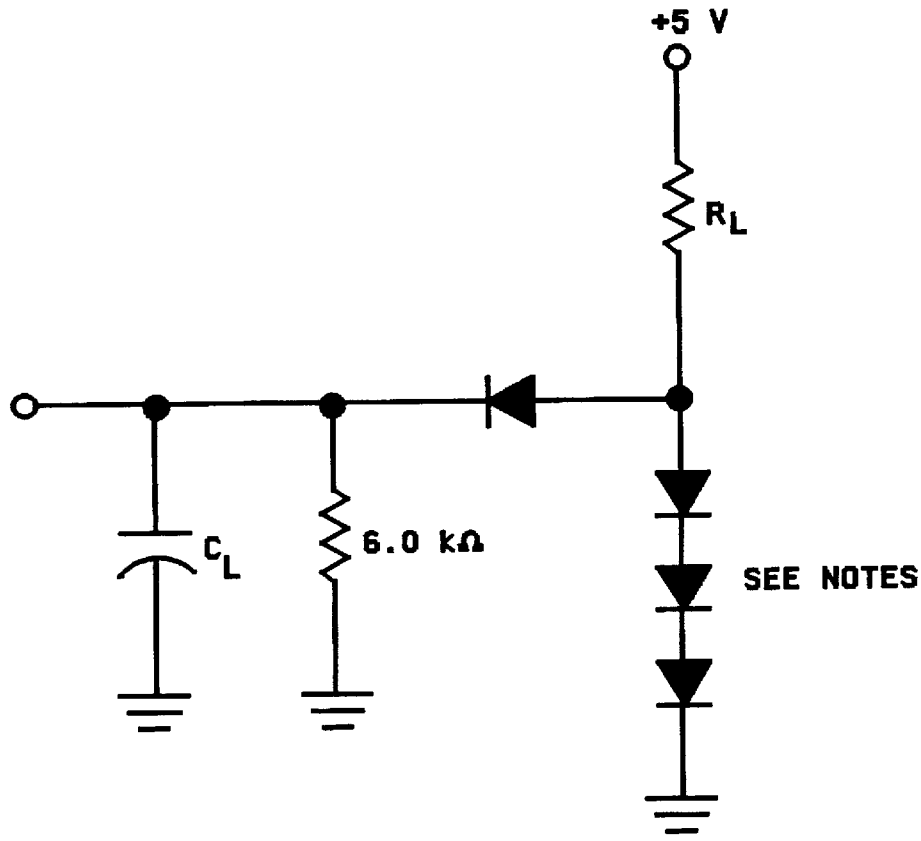
FLOAT WAVEFORMS



AC inputs during testing are driven at V_{CC} -0.5 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at V_{IH} minimum for a logic "1" and V_{IL} maximum for a logic "0".

For timing purposes a port pin is no longer floating when a 100 mV change from load voltage occurs, and begins to float when a 100 mV change from the loaded V_{OH}/V_{OL} level occurs. $I_{OL}/I_{OH} \geq \pm 20$ mA.

FIGURE 5. Timing waveforms and test circuit - continued



Output	R_L	C_L
Port 0, ALE, PSEN	1.2 kΩ	100 pF
All other outputs	2.4 kΩ	80 pF

NOTES:
1. All diodes are 1N914 or equivalent.
2. C_L includes tester and fixture capacitance.

FIGURE 5. Timing waveforms and test circuit - continued

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A. B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9, 10, 11
Group A test requirements (method 5005)	1,2,3,4,7,8 9,10,11
Groups C and D end-point electrical parameters (method 5005)	2, 8 (hot), 10

* PDA applies to subgroup 1.

Margin test method A.

(1) Program greater than 95 percent of the bit locations, including the slowest programming cell (see 3.9.2). The remaining cells shall provide a worst case speed pattern.

(2) Bake, unbiased, for 72 hours at +140°C to screen for data retention lifetime.

(3) Perform a margin test using V_m = +5.9 V at +25°C using loose timing (i.e., T_{ACC} > 1 µs).

(4) Perform dynamic burn-in (see 4.2a).

(5) Margin at V_m = 5.9 V.

(6) Perform electrical tests (see 4.2).

(7) Erase (see 3.9.2), except devices submitted for groups A, B, C, and D testing.

(8) Verify erasure (see 3.9.4)

Margin test method B.

(1) Program at +25°C, 100 percent of the bits.

(2) Bake, unbiased, for 24 hours at +250°C.

(3) Perform margin test at V_m = 5.2 V.

(4) Erase (see 3.9.2).

(5) Perform interim electrical tests in accordance with table II.

(6) For device types 01 to 04, Program 100 percent of the bits and verify (see 3.9.3).

(7) Perform burn-in (see 4.2a).

(8) One-hundred percent test at +25°C (group A, subgroups 1 and 7). V_m = 5.2 V with loose timing, apply PDA, for device types 05 and 06, the virgin state of the device must be verified.

(9) Perform remaining final electrical subgroups and group A testing.

(10) For device types 01, 02, 03, and 04, erase, devices may be submitted for groups B, C, and D at this time.

(11) For device types 01, 02, 03, and 04, verify erasure (see 3.9.4). Steps 1 through 4 are performed at wafer level.

(12) Steps 1 through 4 are performed at wafer level.

TABLE III. Programming characteristics.

Parameter	Symbol	Conditions	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Programming supply voltage	V_{PP}	EPROM programming and verification characteristics T_A = +21°C to +27°C V_{CC} = 5 V ±0.5 V V_{SS} = 0 V See figures 6, 7		All	12.5	13.0	V
Programming supply current	I_{PP}			All		75	mA
Oscillator frequency	$1/t_{CLCL}$			All	4	6	MHz
Address setup to $\overline{PROG}$ low 1/	t_{AVGL}			All	$48t_{CLCL}$		µs
Address hold after $\overline{PROG}$ 1/	t_{GHAX}			All	$48t_{CLCL}$		
Data setup to $\overline{PROG}$ low 1/	t_{DVGL}			All	$48t_{CLCL}$		
Data hold after $\overline{PROG}$ 1/	t_{GHDX}			All	$48t_{CLCL}$		
P2.7 (enable) high to V_{PP} 1/	t_{EHSH}			All	$48t_{CLCL}$		
V_{PP} setup to $\overline{PROG}$ low 1/	t_{SHGL}			All	10		
V_{PP} hold after $\overline{PROG}$ 1/	t_{GHGH}			All	10		µs
$\overline{PROG}$ width	t_{GLGH}			All	90	110	
Address to data valid 1/	t_{AVQV}			All		$48t_{CLCL}$	
Enable low to data valid 1/	t_{ELQV}			All		$48t_{CLCL}$	
Data float after enable 1/	t_{EHQZ}			All	0	$48t_{CLCL}$	
$\overline{PROG}$ high to $\overline{PROG}$ low 1/	t_{GHGL}			All	10		µs

1/ Guaranteed to the limits specified in table III, if not tested.

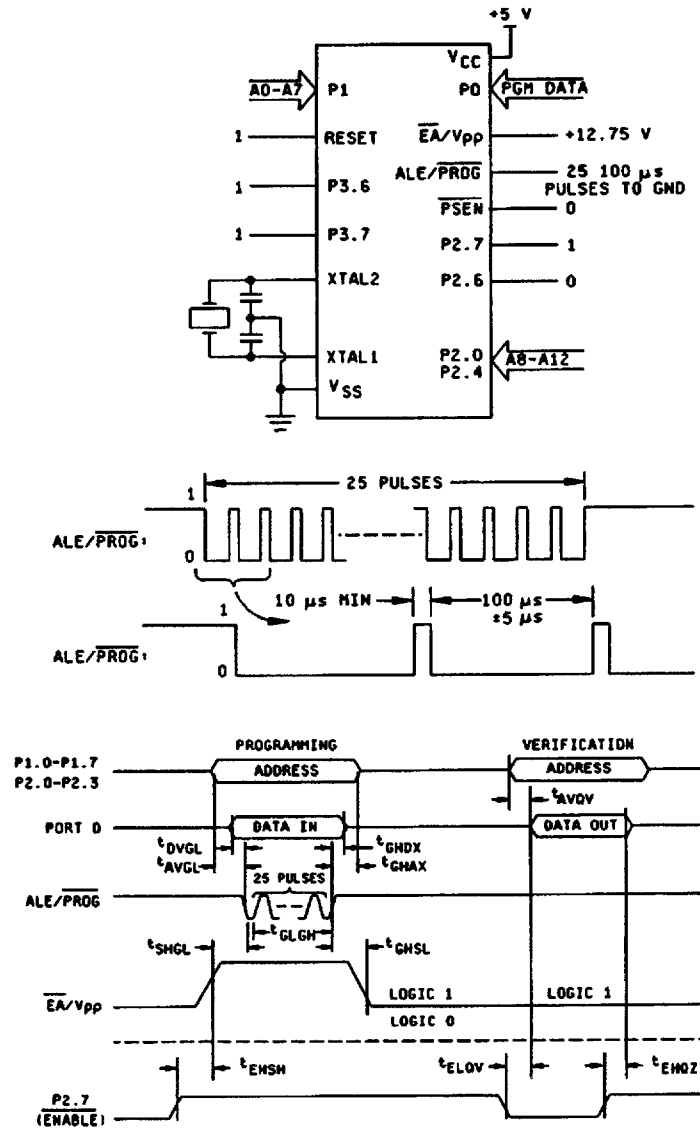


FIGURE 6. EPROM programming and verification waveform.

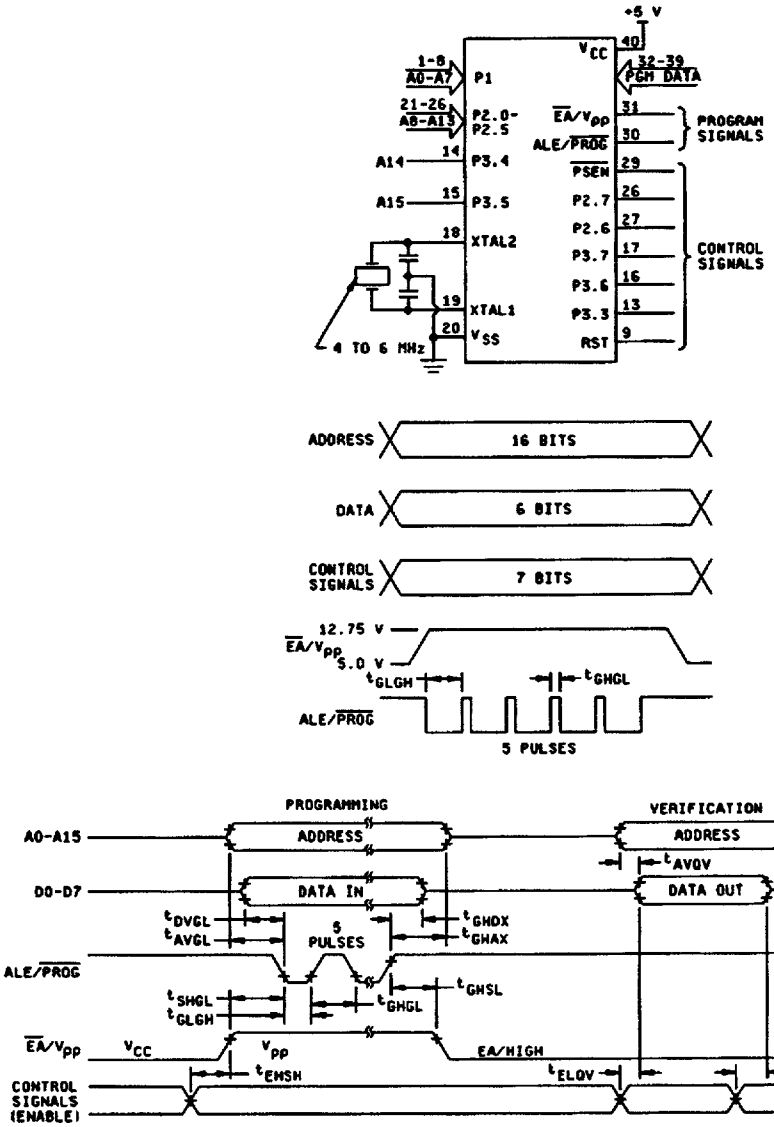


FIGURE 7. Eprom programming and verification waveforms. - Continued

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance. A minmum sample size of five devices with zero rejects shall be required.

d. All devices selected for testing shall have the EPROM programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified (except devices submitted forgroups C and D testing.

e. Subgroups 7 and 8 shall consist of verifying the EPROM pattern specified and the instruction set. The instruction set forms a part of the vendor's test tape and shall be maintained and available from the approved source of supply.

f. The device types 05 and 06 shall be tested for programmability and AC performance compliance to the requirements of group A, subgroups 9, 10, 11. Either of the two techniques is acceptable.

(1) Testing the entire lot using additional built in test circuitry which allows the manufacturer to verify programmability and AC performance without programming user array. If this is done, the resulting test patterns shall be verified on all devices during subgroups 9, 10, 11, group A testing per the sampling plan specified in MIL-STD-883, method 5005.

(2) If such compliance cannot be tested on an unprogramed device, a sample shall be selected to satify programmability requirements prior to performing subgroups 9, 10, and 11. Twelve devices shall be submitted to programming. If more than 2 devices fail to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 24 total devices with no more than 4 total device failures allowable. (Ten devices from the programmmability sample shall be submitted to the requirements of group A, subgroups 9, 10, 11. If more than 2 total devices fail, the lot shall be rejected. At the manufacurer's option, the sample may be increased to 20 total devices with no more than 4 total device failures allowable.)

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) For device types 01, 02, 03, and 04, all devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified.

(5) For device types 05 and 06, the programmability shall be verified per 4.3.1F herein.

4.4 Erasing procedure. The recommended erasure procedure is exposure to ultraviolet light (at 2537 Angstroms) to an integrated dose of at least 15 W-s/cm^2. Exposing the EPROM to an ultraviolet lamp of 12,000 µW/cm^2 rating for 20 to 30 minutes, at a distance of about 1 inch, should be sufficient.

4.5 Programming procedures. The programming characteristics in table III and the following procedures shall be used for programming the device:

a. Devices 01, 02, with an inspection lot date code prior to and including 9104 and devices 03, 04 shall be connected in the electrical configuration that appears in figure 6. Devices 01, 02 with an inspection lot date code 9105 and after shall be connected in the electrical configuration that appears in figure 7. **In addition devices 01, 02 with an inspection lot date code of 9103 and an additional marked number of M121002B, M1490068 or M211001B shall also be programmed utilizing the electrical configuration that appears in figure 7.** The programming characteristics of Table III shall apply.

b. Initially and after each erasure, all bits are in the high "H" state. Information is introduced by selectively programming "L" into the desired bit locations. A programmed "L" can be changed to an "H" by ultraviolet light erasure (see 4.4.).

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein).

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal .

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-8525.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.