REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Change supply voltage tolerance. Change drawing CAGE code. Editorial changes throughout.	1988-NOV-23	M. A. Frye

CURRENT CAGE CODE 67268

REV																								
SHEET																								
REV																								
SHEET																								
REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18					

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Todd Cook

CHECKED BY
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APPROVED BY
M. A. Frye

DRAWING APPROVAL DATE
25 JUNE 1986

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, NMOS, BUS CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	14933	5962-85149

SHEET 1 OF 18

DESC FORM 193-1
SEP 87

* U.S. GOVERNMENT PRINTING OFFICE: 1987 — 748-129/60912

5962-E1069

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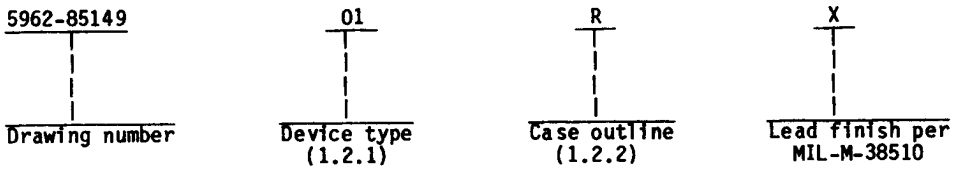
1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	82288-6	6 MHz	Bus controller
02	82288-8	8 MHz	Bus controller

1.2.2 Case outline. The case outline shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
R	D-8 (20-lead, 1.060" x .310" x .200") dual-in-line package

1.3 Absolute maximum ratings.

Supply voltage with respect to ground (V_{CC})	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1 W
Lead temperature (soldering, 10 seconds)	+300°C
Junction temperature (T_J)	+175°C
Thermal resistance, junction to case (θ_{JC})	See MIL-M-38510, appendix C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.75 V dc to +5.25 V dc
Minimum high level input voltage (V_{IH}):	
Clock inputs	+3.8 V dc to V_{CC} +0.5 V dc
All other inputs	+2.0 V dc to V_{CC} +0.5 V dc
Maximum low level input voltage (V_{IL}):	
Clock inputs	-0.5 V dc to +0.6 V dc
All other inputs	-0.5 V dc to +0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

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2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Functional block diagram. The block diagram shall be as specified on figure 2.

3.2.3 Case outline. The case outline shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.5 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.5. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Input low voltage	V_{IL}		1,2,3	All	-0.5	0.8	V
Input high voltage	V_{IH}		1,2,3	All	2.0	V_{CC} +0.5	V
CLK input low voltage	V_{ILC}		1,2,3	All	-0.5	0.6	V
CLK input high voltage	V_{IHC}		1,2,3	All	3.8	V_{CC} +0.5	V
Output low voltage 1/ command outputs	V_{OL}	I_{OL} = 32 mA	1,2,3	All		0.45	V
Output low voltage 2/ control outputs		I_{OL} = 16 mA	1,2,3	All		0.45	V
Output high voltage 1/ command outputs	V_{OH}	I_{OH} = -5 mA	1,2,3	All	2.4		V
Output high voltage 2/ control outputs		I_{OH} = -1 mA	1,2,3	All	2.4		V
Input current ($\overline{SO}$ and $\overline{SI}$ inputs)	I_{IF}	Vf = 0.45 V	1,2,3	All		-0.5	mA
Input leakage current (all other inputs)	I_{IL}	$0\ V \le V_{IN} \le V_{CC}$	1,2,3	All		±10	µA
Output leakage current	I_{LO}	$0.45\ V \le V_{OUT} \le V_{CC}$	1,2,3	All		±10	µA
Power supply current	I_{CC}		1,2,3	All		140	mA
CLK input capacitance	C_{CLK}	FC = 1 MHz See 4.3.1c	4	All		12	pF
Input capacitance	C_{IN}	FC = 1 MHz See 4.3.1c	4	All		10	pF
Input/output capacitance	C_O	FC = 1 MHz See 4.3.1c	4	All		20	pF

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 3/	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
CLK period	1		9,10,11	01	83	250	ns
				02	62	250	
CLK high time	2	at 3.6 V	9,10,11	01	25	230	ns
				02	20	235	
CLK low time	3	at 1.0 V	9,10,11	01	20	225	ns
				02	15	230	
CLK rise time 4/	4	1.0 V to 3.6 V	9,10,11	All		10	ns
CLK fall time 4/	5	3.6 V to 1.0 V	9,10,11	All		10	ns
M/$\overline{IO}$ and status setup time	6		9,10,11	01	28		ns
				02	22		
M/$\overline{IO}$ and status hold time	7		9,10,11	All	1		ns
CENL setup time	8		9,10,11	01	30		ns
				02	20		
CENL hold time	9		9,10,11	All	1		ns
$\overline{READY}$ setup time	10		9,10,11	01	50		ns
				02	38		
$\overline{READY}$ hold time	11		9,10,11	01	35		ns
				02	25		
CMDLY setup time	12		9,10,11	01	25		ns
				02	20		
CMDLY hold time	13		9,10,11	All	1		ns
$\overline{AEN}$ setup time 5/	14		9,10,11	01	25		ns
				02	20		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 3/	Conditions $-55°C \le T_C \le +125°C$ $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
$\overline{AEN}$ hold time 5/	15		9,10,11	All	0		ns
ALE, MCE inactive delay from CLK	16	6/	9,10,11	01	3	25	ns
				02	3	20	
ALE, MCE inactive delay from CLK	17		9,10,11	01		35	ns
				02		25	
DEN (write) inactive from CENL	18		9,10,11	All		35	ns
DT/$\overline{R}$ low from CLK	19		9,10,11	01		40	ns
				02		25	
DEN (READ) active from DT/$\overline{R}$	20		9,10,11	01	5	50	ns
				02	5	35	
DEN (READ) inactive delay from CLK	21		9,10,11	01	3	40	ns
				02	3	35	
DT/$\overline{R}$ high from DEN inactive	22		9,10,11	01	5	45	ns
				02	5	35	
DEN (WRITE) active delay from CLK	23		9,10,11	01		35	ns
				02		30	
DEN (WRITE) inactive delay from CLK	24		9,10,11	01	3	35	ns
				02	3	30	
DEN inactive from CEN	25		9,10,11	01		40	ns
				02		30	
DEN active from CEN	26		9,10,11	01		35	ns
				02		30	
DT/$\overline{R}$ high from CLK (when CEN = LOW)	27		9,10,11	01		50	ns
				02		35	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol 3/	Conditions $-55°C \le T_C \le +125°C$, $V_{CC} = 5\ V \pm 5\%$ unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
DEN active from $\overline{AEN}$	28	6/	9,10,11	01		35	ns
				02		30	
$\overline{CMD}$ active delay from CLK	29	7/	9,10,11	01	3	40	ns
				02	3	25	
$\overline{CMD}$ inactive from CEN	30		9,10,11	01		35	ns
				02		25	
$\overline{CMD}$ inactive from CEN	31		9,10,11	01		35	ns
				02		25	
$\overline{CMD}$ active from CEN	32		9,10,11	01		45	ns
				02		25	
$\overline{CMD}$ inactive enable from $\overline{AEN}$	33		9,10,11	All		40	ns
$\overline{CMD}$ float delay from $\overline{AEN}$	34	8/	9,10,11	All		40	ns
MB setup time	35		9,10,11	01	25		ns
				02	20		
MB hold time	36		9,10,11	All	0		ns
Command inactive enable from MB	37	7/	9,10,11	All		40	ns
Command float time from MB	38	8/	9,10,11	All		40	ns
DEN inactive from MB	39	6/	9,10,11	01		40	ns
				02		30	
DEN active from MB	40		9,10,11	01		35	ns
				02		30	

See footnotes on next page.

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1/ Command outputs are $\overline{\text{INTA}}$, $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$, $\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$.

2/ Control outputs are DT/$\overline{\text{R}}$, $\overline{\text{DEN}}$, ALE and MCE.

3/ The waveform reference number refers to the position where the parameter appears on figure 3.

4/ Guaranteed to the limit specified herein, if not tested.

5/ $\overline{\text{AEN}}$ is an asynchronous input. This specification is for testing purposes only, to assure recognition at specific CLK edge.

6/ Control output load: C1 = 100 pF.

7/ Control output load: C1 = 150 pF.

8/ Float condition occurs when output current is less than I_{LO} in magnitude.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

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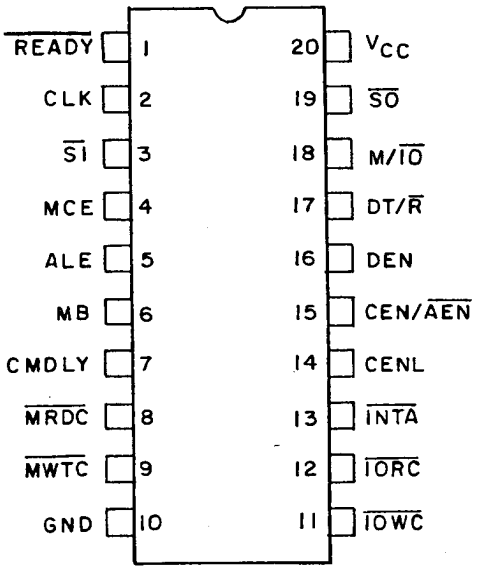

FIGURE 1. Terminal connections.

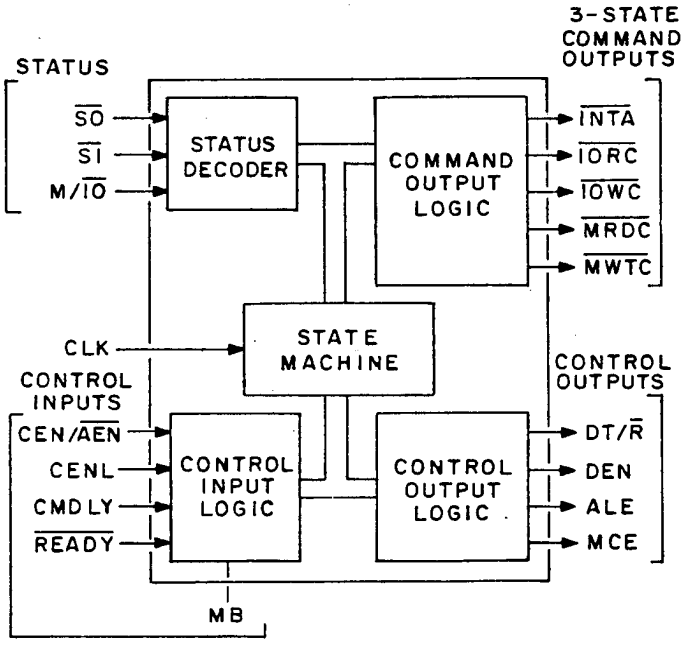

FIGURE 2. Functional block diagram.

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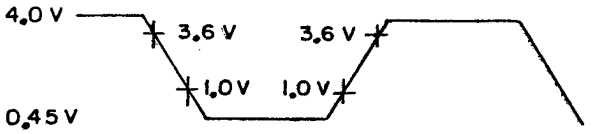
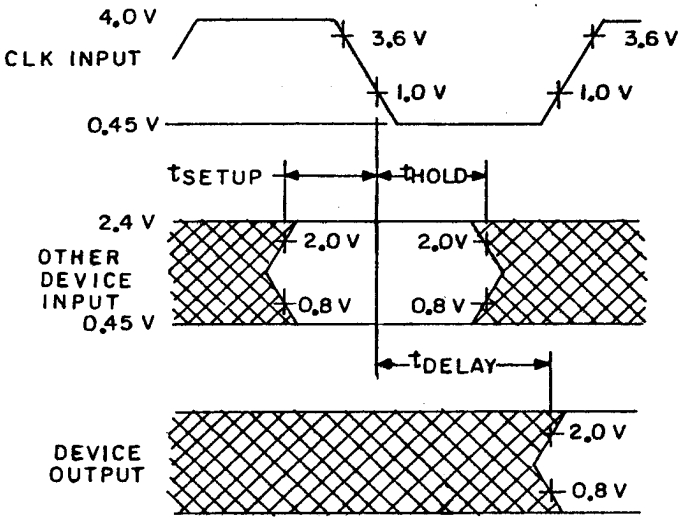
AC DRIVE AND MEASUREMENT POINTS - CLK INPUT



AC SETUP, HOLD AND DELAY TIME MEASUREMENT - GENERAL



AC TEST LOADING ON OUTPUTS

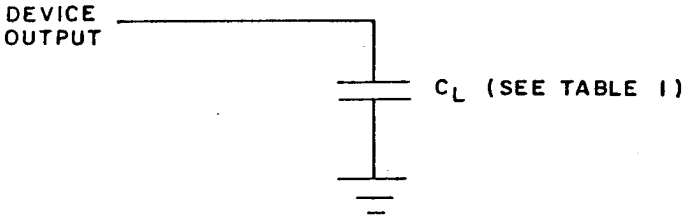


FIGURE 3. Waveforms.

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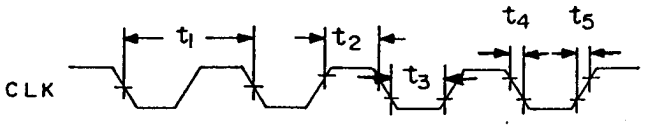
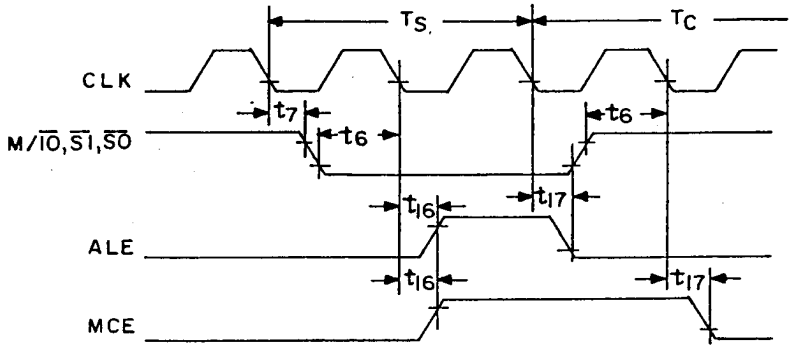
CLK CHARACTERISTICS



STATUS, ALE, MCE, CHARACTERISTICS



CENL, CMDLY, DEN CHARACTERISTICS WITH MB = 0 and CEN = 1 DURING WRITE CYCLE

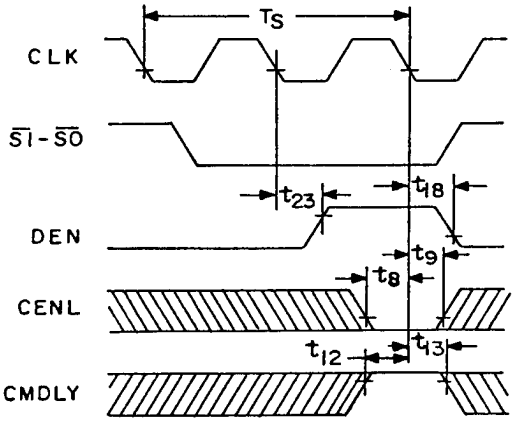


FIGURE 3. Waveforms - Continued.

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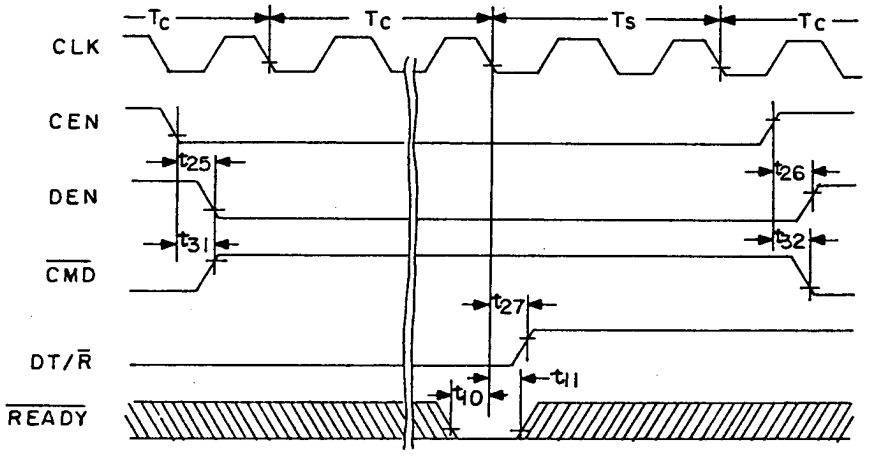
CEN CHARACTERISTICS WITH MB = 0



AEN CHARACTERISTICS WITH MB = 1

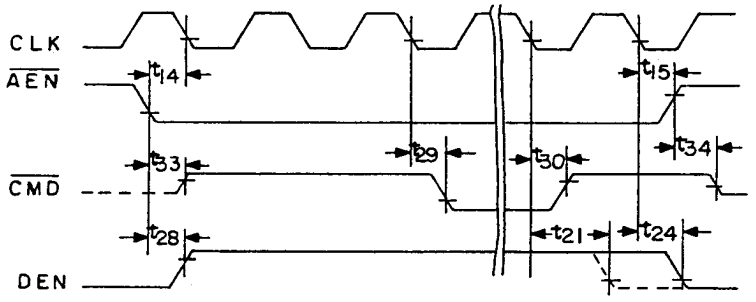


FIGURE 3. Waveforms - Continued.

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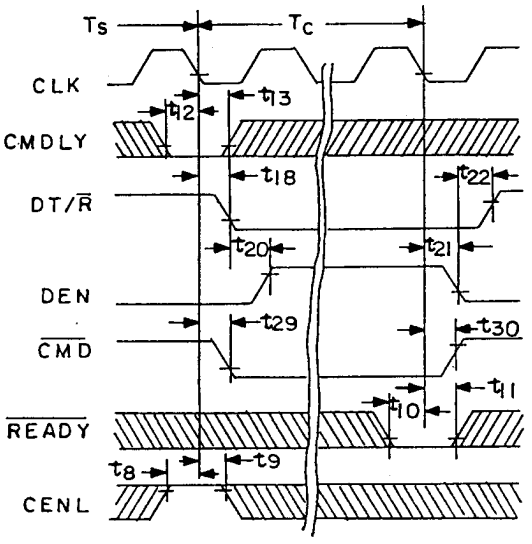
READ CYCLE CHARACTERISTICS WITH MB = 0 AND CEN = 1



WRITE CYCLE CHARACTERISTICS WITH MB = 0 and CEN = 1

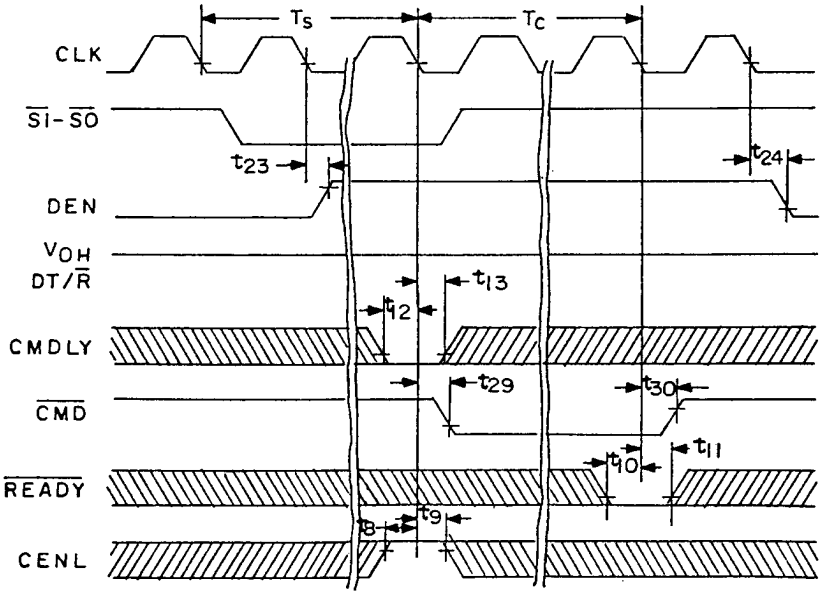


FIGURE 3. Waveforms - Continued.

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4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN}, C_{CLK}, and C_O measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8,9 10,11
Group A test requirements (method 5005)	1,2,3,7,8,9 10,11
Groups C and D end-point electrical parameters (method 5005)	2,8, (+125°C), 10

*PDA applies to subgroups 1 and 7.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Functional description. The following pin function descriptions for this device shall be as follows:

<table>
<tr><th>Symbol</th><th>Type</th><th>Name and function</th></tr>
<tr><td>CLK</td><td>1</td><td>System clock provides the basic timing control for the microsystem. Its frequency is twice the internal processor clock frequency. The falling edge of this input signal establishes when inputs are sampled and command and control outputs change.</td></tr>
<tr><td>$\overline{SO}$, $\overline{SI}$</td><td>1</td><td>Bus cycle status starts a bus cycle and, along with M/$\overline{IO}$, defines the type of bus cycle. These inputs are active LOW. A bus cycle is started when either $\overline{SI}$ or $\overline{SO}$ is sampled LOW at falling edge of CLK. These inputs have pullups sufficient to hold them HIGH when nothing drives them. Setup and hold times must be met for proper operation.
<table>
<tr><th colspan="4">Bus cycle status definition</th></tr>
<tr><th>M/$\overline{IO}$</th><th>$\overline{SI}$</th><th>$\overline{SO}$</th><th>Type of bus cycle</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Interrupt acknowledge</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>I/O read</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>I/O write</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>None; idle</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>Halt or shutdown</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>Memory read</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Memory write</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>None; idle</td></tr>
</table></td></tr>
<tr><td>M/$\overline{IO}$</td><td>1</td><td>Memory or I/O select determines whether the current bus cycle is in the memory space or I/O space. When LOW, the current bus cycle is in the I/O space. Setup and hold times must be met for proper operation.</td></tr>
</table>

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6.4 Functional description - (Continued).

Symbol	Type	Name and function
MB	1	Multibus mode select determines timing of the command and control outputs. When HIGH, the bus controller operates with multibus-compatible timings. When LOW, the bus controller optimizes the command and control output timing for short bus cycles. The function of the CEN/$\overline{\text{AEN}}$ input pin is selected by this signal. This input is intended to be a strapping option and not dynamically changed. This input may be connected to V_{CC} or GND.
CENL	1	Command enable latched is a bus controller select signal which enables the bus controller to respond to the current bus cycle being initiated. CENL is an active HIGH input latched internally at the start of each bus cycle. CENL is used to select the appropriate bus controller for each bus cycle in a system where the CPU has more than one bus it can use. This input may be connected to V_{CC} to select this device for all transfers. No control inputs affect CENL. Setup and hold times must be met for proper operation.
CMDLY	1	Command delay allows delaying the start of a command. CMDLY is an active HIGH input. If sampled HIGH, the command output is not activated and CMDLY is again sampled at the next CLK cycle. When sampled LOW the selected command is enabled. If $\overline{\text{READY}}$ is detected LOW before the command output is activated, the device will terminate the bus cycle, even if no command was issued. Setup and hold times must be satisfied for proper operation. This input may be connected to GND if no delays are required before starting a command.
$\overline{\text{READY}}$	1	$\overline{\text{READY}}$ indicates the end of the current bus cycle. $\overline{\text{READY}}$ is an active LOW input. Multibus mode requires at least one wait state to allow the command outputs to become active. $\overline{\text{READY}}$ must be LOW during reset, to force the device into the idle state. Setup and hold times must be met for proper operation.
CEN/$\overline{\text{AEN}}$	1	Command enable/Address enable controls the command and DEN outputs of the bus controller. CEN/$\overline{\text{AEN}}$ inputs may be asynchronous to CLK. Setup and hold times are given to assure a guaranteed response to synchronous inputs. This input may be connected to V_{CC} or GND. When MB is HIGH this pin has the $\overline{\text{AEN}}$ function. $\overline{\text{AEN}}$ is an active LOW input which indicates that the CPU has been granted use of a shared bus and the bus controller command outputs may exit 3-state OFF and become inactive (HIGH). $\overline{\text{AEN}}$ HIGH indicates that the CPU does not have control of the shared bus and forces the command outputs into 3-state OFF and DEN inactive (LOW). $\overline{\text{AEN}}$ would normally be controlled by a bus arbiter which activates $\overline{\text{AEN}}$ when that arbiter owns the bus to which the bus controller is attached. When MB is LOW this pin has the CEN function. CEN is an unlatched active HIGH input which allows the bus controller to activate its command and DEN outputs. With MB LOW, CEN LOW forces the command and DEN outputs inactive but does not 3-state them.

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6.4 Functional description - (Continued).

Symbol	Type	Name and function
ALE	O	Address latch enable controls the address latches used to hold an address stable during a bus cycle. This control output is active HIGH. ALE will not be issued for the halt bus cycle and is not affected by any of the control inputs.
MCE	O	Master cascade enable signals that a cascade address from a master interrupt controller may be placed onto the CPU address bus for latching by the address latches under ALE control. The CPU's address bus may then be used to broadcast the cascade address to slave interrupt controllers so only one of them will respond to the interrupt acknowledge cycle. This control output is active HIGH. MCE is only active during interrupt acknowledge cycles and is not affected by any control input. Using MCE to enable cascade address drivers requires latches which save the cascade address on the falling edge of ALE.
DEN	O	Data enable controls when data transceivers connected to the local data bus should be enabled. DEN is an active HIGH control output. DEN is delayed for write cycles in the multibus mode.
DT/$\overline{R}$	O	Data transmit/Receive establishes the direction of data flow to or from the local data bus. When HIGH, this control output indicates that a write bus cycle is being performed. A LOW indicates a read bus cycle. DEN is always inactive when DT/$\overline{R}$ changes states. This output is HIGH when no bus cycle is active. DT/$\overline{R}$ is not affected by any of the control inputs.
$\overline{IOWC}$	O	I/O write command instructs an I/O device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{IORC}$		I/O read command instructs an I/O device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{MWTC}$	O	Memory write command instructs a memory device to read the data on the data bus. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{MRDC}$	O	Memory read command instructs the memory device to place data onto the data bus. This command output is active LOW. The MB and CMDLY inputs control this output becomes active. $\overline{READY}$ controls when it becomes inactive.
$\overline{INTA}$	O	Interrupt acknowledge tells an interrupting device that its interrupt request is being acknowledged. This command output is active LOW. The MB and CMDLY inputs control when this output becomes active. $\overline{READY}$ controls when it becomes inactive.
V_{CC}		System power: +5 V power supply
GND		System ground: 0 volts

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6.5 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8514901RX	34649	MD82288-6/B
5962-8514902RX	34649	MD82288-8/B

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34649	Intel Corporation 5000 W. Williams Field Road Chandler, AZ 85224

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