



Binary Counter

**ELECTRICALLY TESTED PER:
MPG 10578**

The 10578 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function. Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

- 505 mW Max/Pkg (No Load)
- $f_{toggle} = 150 \text{ MHz (typ)}$
- $t_r, t_f = 2.7 \text{ ns typ (20\% - 80\%)}$

PIN ASSIGNMENTS

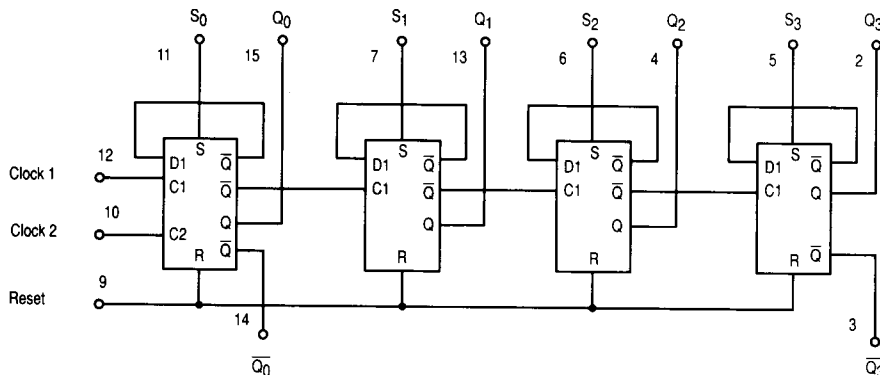
FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_3	2	6	3	51Ω to V_{TT}
$\bar{Q}_3$	3	7	4	51Ω to V_{TT}
Q_2	4	8	5	51Ω to V_{TT}
S_3	5	9	7	GND
S_2	6	10	8	GND
S_1	7	11	9	GND
V_{EE}	8	12	10	V_{EE}
Reset	9	13	12	OPEN
Clock 2	10	14	13	OPEN
S_0	11	15	14	GND
Clock 1	12	16	15	OPEN
Q_1	13	1	17	51Ω to V_{TT}
$\bar{Q}_0$	14	2	18	51Ω to V_{TT}
Q_0	15	3	19	51Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:

$V_{TT} = -2.2 \text{ V MIN} / -2.0 \text{ V MAX}$

$V_{EE} = -5.7 \text{ V MAX} / -5.2 \text{ V MIN}$

LOGIC DIAGRAM



Military 10578

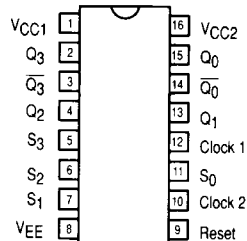


AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: 10578/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

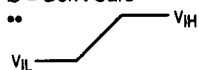
The letter "M" appears before the slash on LCC.



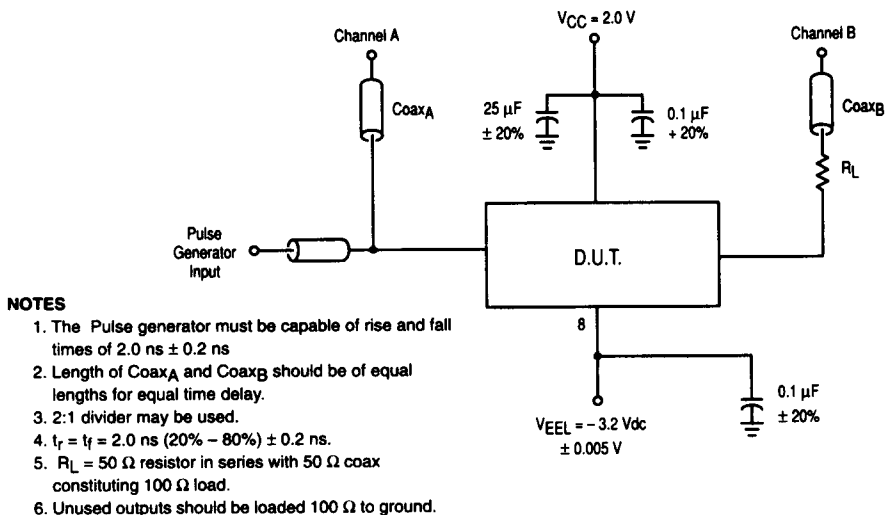
10578

INPUTS							OUTOUTS			
R	S ₀	S ₁	S ₂	S ₃	C ₁	C ₂	Q ₀	Q ₁	Q ₂	Q ₃
H	L	L	L	L	φ	φ	L	L	L	L
L	H	H	H	H	φ	φ	H	H	H	H
L	L	L	L	L	H	φ	No Count			
L	L	L	L	L	φ	H				
L	L	L	L	L	..	..	L	L	L	L
L	L	L	L	L	..	..	H	L	L	L
L	L	L	L	L	..	..	L	H	L	L
L	L	L	L	L	..	..	H	H	L	L
L	L	L	L	L	..	..	L	L	H	L
L	L	L	L	L	..	..	H	L	H	L
L	L	L	L	L	..	..	L	H	H	L
L	L	L	L	L	..	..	H	H	H	L
L	L	L	L	L	..	..	L	L	L	H
L	L	L	L	L	..	..	H	L	L	H
L	L	L	L	L	..	..	L	H	L	H
L	L	L	L	L	..	..	H	H	L	H
L	L	L	L	L	..	..	L	L	H	H
L	L	L	L	L	..	..	H	L	H	H
L	L	L	L	L	..	..	L	H	H	H
L	L	L	L	L	..	..	H	H	H	H

Ø = Don't Care



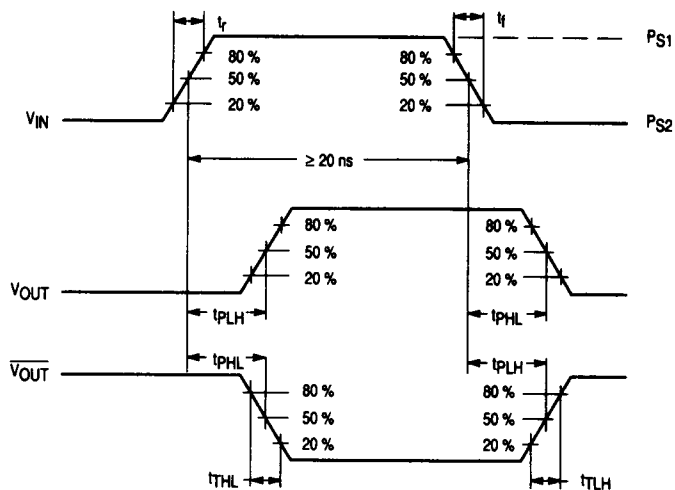
Clock transition from V_{IL} to V_{IH} may be applied to C_1 or C_2 or both for same effect.



NOTES

1. The Pulse generator must be capable of rise and fall times of $2.0\text{ ns} \pm 0.2\text{ ns}$
2. Length of CoaxA and CoaxB should be of equal lengths for equal time delay.
3. 2:1 divider may be used.
4. $t_r = t_f = 2.0\text{ ns}$ (20% - 80%) $\pm 0.2\text{ ns}$.
5. $R_L = 50\text{ }\Omega$ resistor in series with $50\text{ }\Omega$ coax constituting $100\text{ }\Omega$ load.
6. Unused outputs should be loaded $100\text{ }\Omega$ to ground.

Figure 1. Switching Test Circuit

**NOTES**

1. V_{IN} waveform has the following characteristics:

- Pulse width ≥ 20 ns.
- frequency = 1.0 MHz.
- t_r and $t_f = 2.0$ ns $\pm$ 0.2 ns.

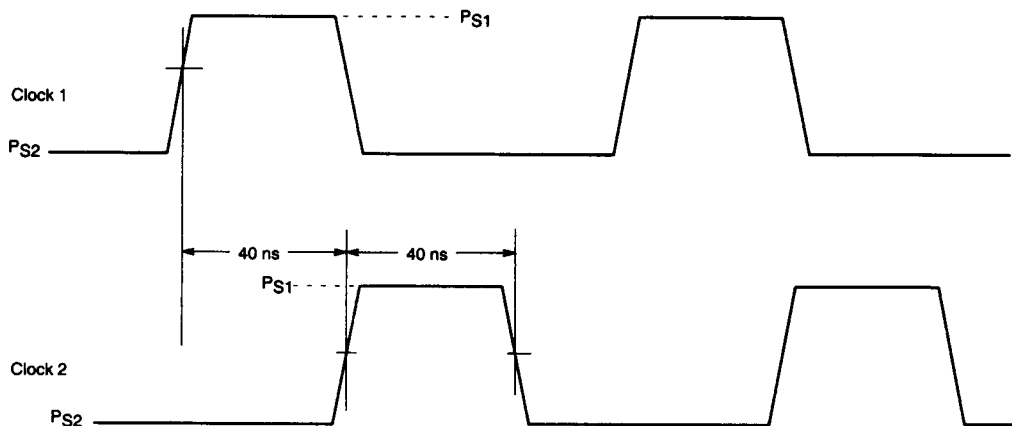


Figure 2. Switching Test Circuit Waveforms

10578 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to -2.0 volts.

Test Temperature	Test Voltage Values (Volts)						
	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	PS1	PS2	VEEL
T _A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2
T _A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2
T _A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW						
	Functional Parameters:	+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V _{CC} = 0 V, Output Load = 100 Ω to - 2.0 V						
		Subgroup 1		Subgroup 2		Subgroup 3									
		Min	Max	Min	Max	Min	Max								
V _{OH}	High Output Voltage	- 0.93	- 0.78	- 0.825	- 0.63	- 1.08	- 0.88	V	5 - 7, 9, 11	V _{IH}	V _{IL}	P ₁ , 2, 3	V _{EE}	V _{CC}	P. U. T.
V _{OL}	Low Output Voltage	- 1.85	- 1.62	- 1.82	- 1.545	- 1.92	- 1.655	V	5 - 7, 9, 11				8	1, 16	2, 3, 4, 13, 14
V _{OL1}	Low Output Voltage	- 1.85	- 1.60	- 1.82	- 1.525	- 1.92	- 1.635	V		5 - 7, 9 - 12	5 - 7, 9 - 12		8	1, 16	2, 3, 4, 13, 14
V _{OH1}	High Output Voltage	- 0.95	- 0.78	- 0.845	- 0.63	- 1.10	- 0.88	V		5 - 7, 9 - 12			8	1, 16	2, 3, 4, 13 - 15
I _{IH}	Input Current High		245		415		415	μA	10, 12				8	1, 16	10, 12
I _{IH1}	Input Current High		220		375		375	μA	5 - 7, 11				8	1, 16	5 - 7, 11
I _{IH2}	Input Current High		410		700		700	μA	9				8	1, 16	9
I _{IL}	Input Current Low	0.5		0.3		0.5		μA			5 - 7, 9 - 12		8	1, 16	5 - 7, 9 - 12
I _{EE}	Power Supply Drain Current	- 88	- 10	- 97	- 10	- 97	- 10	mA					8	1, 16	8

NOTES



10578 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10K series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to 0.0 volts.

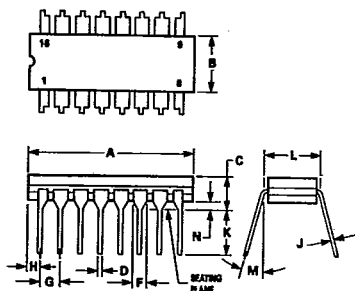
Test Temperature	Test Voltage Values (Volts)							
	V _{IH}	V _{IL}	V _{IH1}	V _{IL1}	PS1	PS2	VEE	VEEL
T _A = 25 °C	-0.78	-1.85	-1.105	-1.475	+1.11	+0.31	-5.2	-3.2
T _A = 125 °C	-0.63	-1.82	-1.000	-1.400	+1.24	+0.36	-5.2	-3.2
T _A = -55 °C	-0.88	-1.92	-1.255	-1.510	+1.01	+0.28	-5.2	-3.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW																																																																																																																																														
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND																																																																																																																																														
																			Subgroup 9		Subgroup 10		Subgroup 11		Min	Max	Min	Max	Min	Max	VIN	VOUT	PS1	PS2	fmax	VCC	VEEL	P. U. T.	tTLH	Rise Time	1.1	4.5	1.1	5.3	1.1	4.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15	tTHL	Fall Time	1.1	4.5	1.1	5.3	1.1	4.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15	t _{pd}	Propagation Delay Clock to Q ₀ , Q ₁	1.5	4.8	1.5	5.6	1.4	5.0	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15	t _{pd}	Propagation Delay Clock to Q ₁	2.0	9.2	2.0	10.8	1.9	9.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15	t _{pd}	Propagation Delay Clock to Q ₂	3.0	12	3.0	14	2.9	13	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15	t _{pd}	Propagation Delay Clock to Q ₃ , Q ₃	4.0	14.5	4.0	17	3.9	16	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15	t _{sel/ reset}	Set/Rest Input	1.5	5.0	1.5	6.1	1.4	5.6	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15	t _{tog}
		Subgroup 9		Subgroup 10		Subgroup 11																																																																																																																																																	
Min	Max	Min	Max	Min	Max	VIN	VOUT	PS1	PS2	fmax	VCC	VEEL	P. U. T.																																																																																																																																										
tTLH	Rise Time	1.1	4.5	1.1	5.3	1.1	4.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15																																																																																																																																								
tTHL	Fall Time	1.1	4.5	1.1	5.3	1.1	4.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15																																																																																																																																								
t _{pd}	Propagation Delay Clock to Q ₀ , Q ₁	1.5	4.8	1.5	5.6	1.4	5.0	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15																																																																																																																																								
t _{pd}	Propagation Delay Clock to Q ₁	2.0	9.2	2.0	10.8	1.9	9.9	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15																																																																																																																																								
t _{pd}	Propagation Delay Clock to Q ₂	3.0	12	3.0	14	2.9	13	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15																																																																																																																																								
t _{pd}	Propagation Delay Clock to Q ₃ , Q ₃	4.0	14.5	4.0	17	3.9	16	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15																																																																																																																																								
t _{sel/ reset}	Set/Rest Input	1.5	5.0	1.5	6.1	1.4	5.6	ns	5 - 7, 9, 11	2 - 4, 13 - 15	6, 7, 11		1, 16	8	2 - 4, 13 - 15																																																																																																																																								
t _{tog}	Toggle Frequency	125		125		125		MHz		14, 15		6, 7, 9, 11	10, 12	1, 16	8	14, 15																																																																																																																																							

PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

**L SUFFIX
CERAMIC PACKAGE
CASE 620-09**



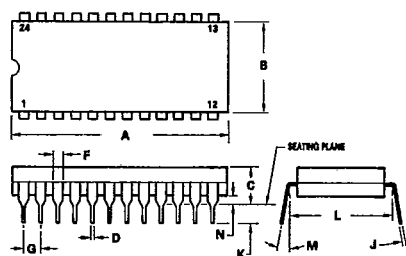
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.32	6.59	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	2.27	2.87	0.090	0.110
M	10°		10°	
N	0.51	1.02	0.020	0.040

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- PACKAGE INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT.
- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

**L SUFFIX
CERAMIC PACKAGE
CASE 623-05**

(LW SUFFIX
FOR
MC10H181
ONLY)

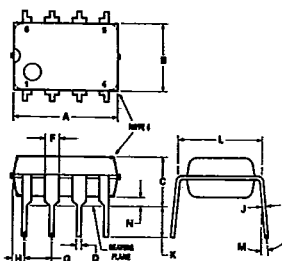


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.77	1.230	1.290
B	12.70	15.49	0.500	0.610
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	0° 15°		0° 15°	
N	0.51	1.27	0.020	0.050

NOTES:

- DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION (WHEN FORMED PARALLEL).

**P SUFFIX
PLASTIC PACKAGE
CASE 626-04**

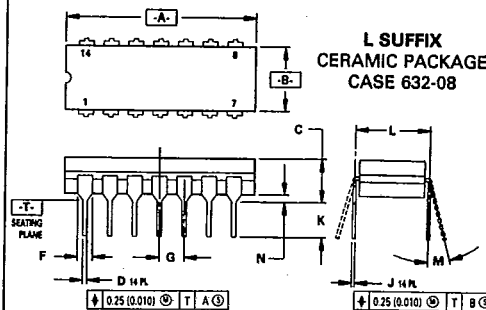


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.54	4.45	0.135	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.87	3.43	0.115	0.135
L	2.87 BSC		0.300 BSC	
M	10°		10°	
N	0.51	0.76	0.020	0.030

NOTES:

- LEAD POSITIONAL TOLERANCE:
 $\phi 0.13 (0.005) \text{ T A } \phi \text{ B } \phi$
- DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
- PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS).
- DIMENSIONS A AND B ARE DATUMS.
- DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.

**L SUFFIX
CERAMIC PACKAGE
CASE 632-08**



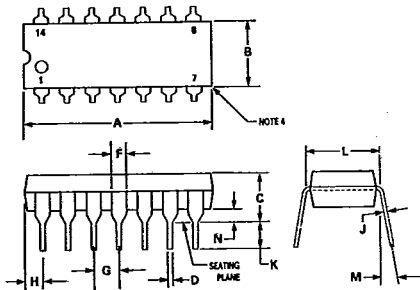
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.94	0.750	0.785
B	6.23	7.11	0.245	0.280
C	3.94	5.08	0.155	0.200
D	0.39	0.50	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	3.18	4.31	0.125	0.170
L	7.62 BSC		0.300 BSC	
M	0° 15°		0° 15°	
N	0.51	1.01	0.020	0.040

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
- DIM F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

PACKAGE OUTLINE DIMENSIONS (continued)

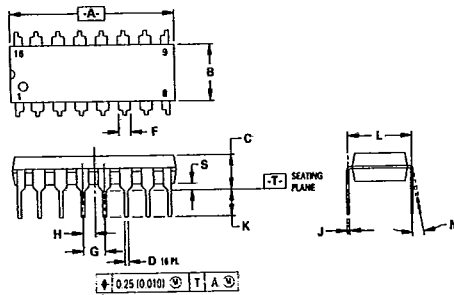
T-90-20

P SUFFIX
PLASTIC PACKAGE
CASE 646-06

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	19.56	0.715	0.770
B	6.10	6.60	0.240	0.260
C	3.69	4.69	0.145	0.185
D	0.38	0.53	0.015	0.021
E	1.02	1.78	0.040	0.070
F	2.54 BSC		0.100 BSC	
G	1.32	2.41	0.052	0.095
H	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	10°	0°	10°
N	0.29	1.01	0.015	0.039

NOTES:

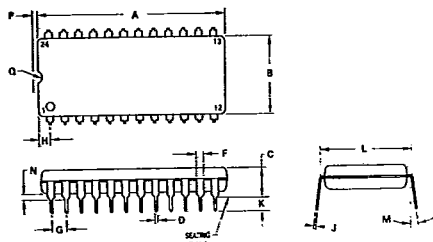
- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

P SUFFIX
PLASTIC PACKAGE
CASE 648-08

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.80	19.55	0.740	0.770
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.39	0.53	0.015	0.021
E	1.02	1.77	0.040	0.070
F	2.54 BSC		0.100 BSC	
G	1.27 BSC		0.050 BSC	
H	0.21	0.38	0.008	0.015
K	2.80	3.30	0.110	0.130
L	7.50	7.74	0.295	0.305
M	0°	10°	0°	10°
N	0.51	1.01	0.020	0.040

NOTES:

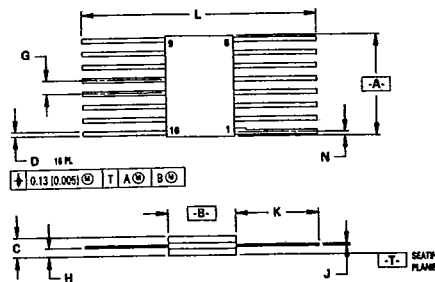
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
- DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
- ROUNDED CORNERS OPTIONAL.

P SUFFIX
PLASTIC PACKAGE
CASE 649-03(PW SUFFIX
FOR MC10H181
ONLY)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
E	1.02	1.52	0.040	0.060
F	2.54 BSC		0.100 BSC	
G	1.65	2.16	0.065	0.085
H	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	—	10°	—	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:

- LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
- DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

F SUFFIX
CERAMIC PACKAGE
CASE 650-05

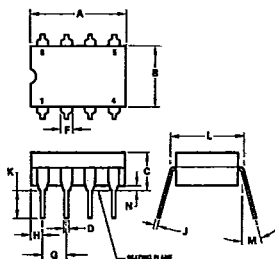
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	9.90	0.370	0.390
B	6.23	6.60	0.245	0.260
C	1.53	2.15	0.060	0.085
D	0.38	0.48	0.014	0.019
E	1.27 BSC		0.050 BSC	
F	0.64	0.01	0.025	0.040
G	0.11	0.17	0.004	0.007
K	6.35	9.39	0.250	0.370
L	18.93	—	0.745	—
N	—	0.50	—	0.020

NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- DIMENSION "A" AND "B" ALLOW FOR LID MISMATCH, AND GLASS MENISCUS.
- DIMENSION "H" SHALL BE MEASURED AT THE POINT OF EXIT OF THE LEAD FROM THE BODY.
- LEAD NUMBER 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
- DIMENSION "J" INCLUDES SOLDER LEAD FINISH.
- LEAD NUMBERS SHOWN FOR REFERENCE ONLY.

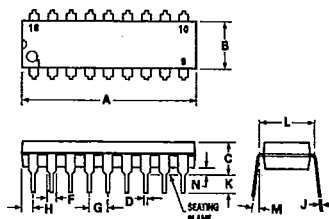
PACKAGE OUTLINE DIMENSIONS (continued)

T-90-20

L SUFFIX
CERAMIC PACKAGE
CASE 693-02


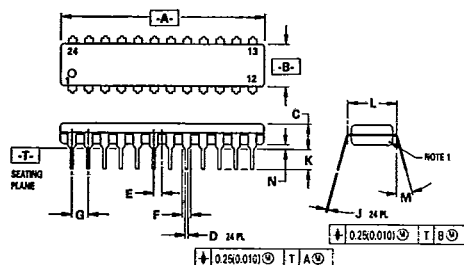
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.91	10.92	0.390	0.430
B	6.22	6.99	0.245	0.275
C	4.32	5.08	0.170	0.200
D	0.41	0.51	0.016	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	1.14	1.65	0.045	0.065
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	— 15°		— 15°	
N	0.51	1.02	0.020	0.040

- NOTES:
- LEADS WITHIN 0.13 mm (0.005) RAD OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
 - DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

P SUFFIX
PLASTIC PACKAGE
CASE 707-02


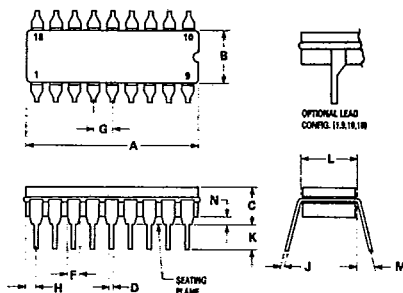
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
E	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

- NOTES:
- POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25mm(0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
 - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIMENSION B DOES NOT INCLUDE MOLD FLASH.

P SUFFIX
PLASTIC PACKAGE
CASE 724-03


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.25	32.13	1.230	1.265
B	6.35	6.85	0.250	0.270
C	3.69	4.44	0.145	0.175
D	0.38	0.51	0.015	0.020
E	1.27 BSC		0.050 BSC	
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.18	0.30	0.007	0.012
I	2.80	3.55	0.110	0.140
J	7.62 BSC		0.300 BSC	
K	0°	15°	0°	15°
L	0.51	1.01	0.020	0.040

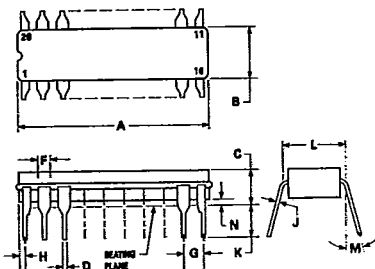
- NOTES:
- CHAMFERED CONTOUR OPTIONAL.
 - DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.

L SUFFIX
CERAMIC PACKAGE
CASE 726-04


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	22.35	23.11	0.880	0.910
B	6.10	7.49	0.240	0.295
C	—	5.08	—	0.200
D	0.38	0.53	0.015	0.021
E	1.40	1.78	0.055	0.070
F	2.54 BSC		0.100 BSC	
G	0.51	1.14	0.020	0.045
H	0.20	0.30	0.008	0.012
I	3.18	4.32	0.125	0.170
J	7.62 BSC		0.300 BSC	
K	0°	15°	0°	15°
L	0.51	1.02	0.020	0.040

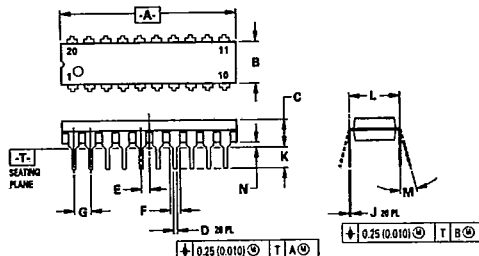
- NOTES:
- LEADS, TRUE POSITIONED WITHIN 0.25 mm (0.010) DIA. AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 - DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIM "A" & "B" INCLUDES MENISCUS.
 - "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 9, 10, AND 18.

PACKAGE OUTLINE DIMENSIONS (continued)

L SUFFIX
CERAMIC PACKAGE
CASE 732-03

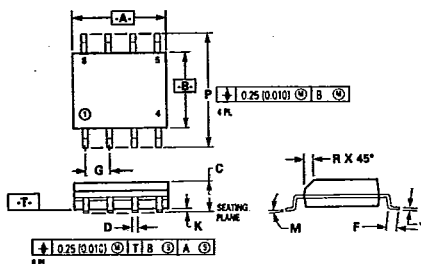
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.43	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
E	1.40	1.65	0.055	0.065
F	2.54 BSC		0.100 BSC	
G	0.51	1.27	0.020	0.050
H	0.20	0.30	0.008	0.012
J	3.18	4.06	0.125	0.160
K	7.62 BSC		0.300 BSC	
L	0°	15°	0°	15°
M	0.25	1.02	0.010	0.040

- NOTES:
- LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
 - DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIM A AND B INCLUDES MENISCUS.

P SUFFIX
PLASTIC PACKAGE
CASE 738-03

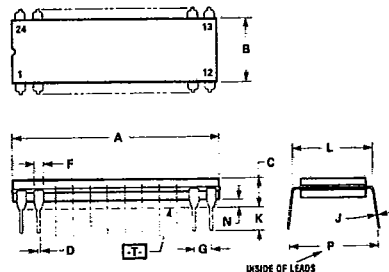
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	25.56	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

- NOTES:
- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIMENSION: INCH.
 - DIMENSION 'L' TO CENTER OF LEAD WHEN FORMED PARALLEL.
 - DIMENSION 'B' DOES NOT INCLUDE MOLD FLASH.

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-03

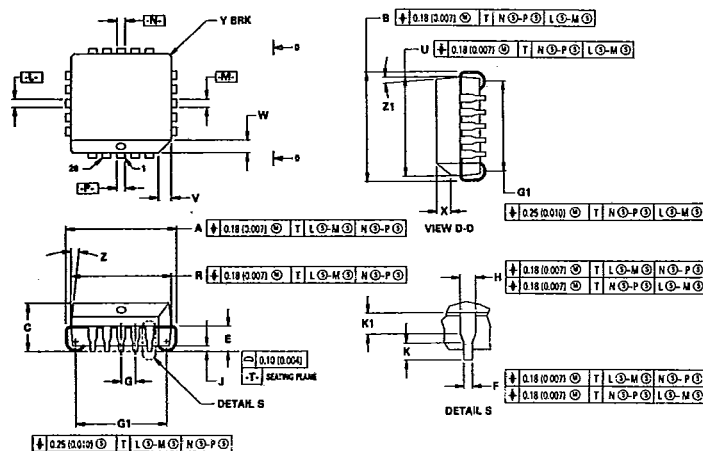
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.18	0.25	0.007	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- NOTES:
- DIMENSIONS "A" AND "B" ARE DATUMS AND "T" IS A DATUM SURFACE.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 - CONTROLLING DIM: MILLIMETER.
 - DIMENSION "A" AND "B" DO NOT INCLUDE MOLD PROTRUSION.
 - MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

L SUFFIX
CERAMIC PACKAGE
CASE 758-01

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.64	1.240	1.285
B	7.24	7.75	0.285	0.305
C	3.68	4.44	0.145	0.175
D	0.38	0.53	0.015	0.021
F	1.14	1.57	0.045	0.062
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.19	0.100	0.165
L	7.62	7.87	0.300	0.310
N	0.51	1.27	0.020	0.050
a	9.14	10.16	0.360	0.400

- NOTES:
- DIMENSION A IS DATUM.
 - POSITIONAL TOLERANCE FOR LEADS: 24 PLACES $\pm 0.25 (0.010) \text{ TIA } \text{B}$
 - "T" IS SEATING PLANE.
 - DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
 - DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

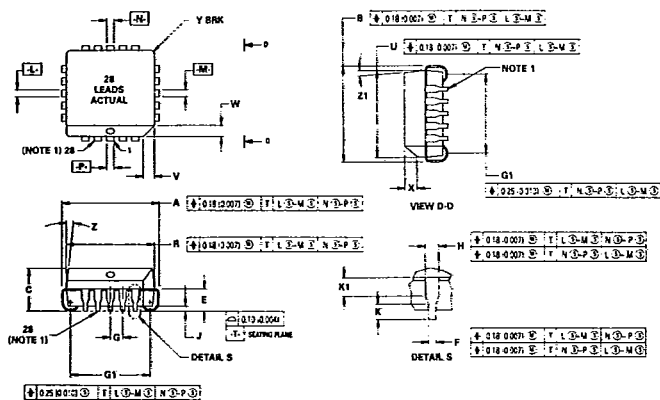


FN SUFFIX
PLASTIC PACKAGE
CASE 775-02

NOTES:

1. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
2. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
3. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.78	10.03	0.385	0.395
B	9.78	10.03	0.385	0.395
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51		0.020	
K	0.64		0.025	
R	8.83	9.04	0.350	0.356
U	8.83	9.04	0.350	0.356
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y		0.50		0.020
Z	2°	10°	2°	10°
G1	7.88	8.38	0.310	0.330
K1	1.02		0.040	
Z1	2°	10°	2°	10°



FN SUFFIX
PLASTIC PACKAGE
CASE 776-02

NOTES:

1. DUE TO SPACE LIMITATION, CASE 776-02 SHALL BE REPRESENTED BY A GENERAL (SMALLER) CASE OUTLINE DRAWING RATHER THAN SHOWING ALL 28 LEADS.
2. DATUMS -L-, -M-, -N-, AND -P- DETERMINED WHERE TOP OF LEAD SHOULDER EXIT PLASTIC BODY AT MOLD PARTING LINE.
3. DIM G1, TRUE POSITION TO BE MEASURED AT DATUM -T-, SEATING PLANE.
4. DIM R AND U DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION IS 0.25 (0.010) PER SIDE.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
6. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.32	12.57	0.485	0.495
B	12.32	12.57	0.485	0.495
C	4.20	4.57	0.165	0.180
E	2.29	2.79	0.090	0.110
F	0.33	0.48	0.013	0.019
G	1.27 BSC		0.050 BSC	
H	0.66	0.81	0.026	0.032
J	0.51		0.020	
K	0.64		0.025	
R	11.43	11.58	0.450	0.456
U	11.43	11.58	0.450	0.456
V	1.07	1.21	0.042	0.048
W	1.07	1.21	0.042	0.048
X	1.07	1.42	0.042	0.056
Y		0.50		0.020
Z	2°	10°	2°	10°
G1	10.42	10.92	0.410	0.430
K1	1.02		0.040	
Z1	2°	10°	2°	10°

MECL Logic Surface Mount

WHY SURFACE MOUNT?

Surface Mount Technology is now being utilized to offer answers to many problems that have been created in the use of insertion technology.

Limitations have been reached with insertion packages and PC board technology. Surface Mount Technology offers the opportunity to continue to advance the State-of-the-Art designs that cannot be accomplished with Insertion Technology.

Surface Mount Packages allow more optimum device performance with the smaller Surface Mount configuration. Internal lead lengths, parasitic capacitance and inductance that placed limitations on chip performance have been reduced.

The lower profile of Surface Mount Packages allows more boards to be utilized in a given amount of space. They are stacked closer together and utilize less total volume than insertion populated PC boards.

Printed circuit costs are lowered with the reduction of the number of board layers required. The elimination or reduction of the number of plated through holes in the board, contribute significantly to lower PC board prices.

Surface Mount assembly does not require the preparation of components that are common on insertion technology lines. Surface Mount components are sent directly to the assembly line, eliminating an intermediate step.

Automatic placement equipment is available that can place Surface Mount components at the rate of a few thousand per hour to hundreds of thousands of components per hour.

Surface Mount Technology is cost effective, allowing the manufacturer the opportunity to produce smaller units and offer increased functions with the same size product.

MECL AVAILABILITY IN SURFACE MOUNT

Motorola is now offering MECL 10K and MECL 10KH in the PLCC (Plastic Leaded Chip Carrier) packages.

MECL in PLCC may be ordered in conventional plastic rails or on Tape and Reel. Refer to the Tape and Reel section for ordering details.

TAPE AND REEL

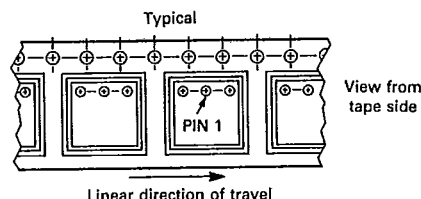
Motorola has now added the convenience of Tape and Reel packaging for our growing family of standard Integrated Circuit products. The packaging fully conforms to

the latest EIA RS-481A specification. The antistatic embossed tape provides a secure cavity sealed with a peel-back cover tape.

GENERAL INFORMATION

- Reel Size 13 inch (330 mm) Suffix: R2
- Tape Width 16 mm
- Units/Reel 1000

MECHANICAL POLARIZATION



ORDERING INFORMATION

- Minimum Lot Size/Device Type = 3000 Pieces.
- No Partial Reel Counts Available.
- To order devices which are to be delivered in Tape and Reel, add the appropriate suffix to the device number being ordered.

EXAMPLE:

ORDERING CODE

MC10100FN
MC10100FNR2
MC10H100FN
MC10H100FNR2
MC12015D
MC12015DR2

SHIPMENT METHOD

Magazines (Rails)
13 inch Tape and Reel
Magazines (Rails)
13 inch Tape and Reel
Magazines (Rails)
13 inch Tape and Reel

DUAL-IN-LINE PACKAGE TO PLCC PIN CONVERSION DATA

The following tables give the equivalent I/O pinouts of Dual-In-Line (DIL) packages and Plastic Leaded Chip Carrier (PLCC) packages.

Conversion Tables

16 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
20 PIN PLCC	2	3	4	5	7	8	9	10	12	13	14	15	17	18	19	20

20 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
20 PIN PLCC	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

24 PIN DIL	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
28 PIN PLCC	2	3	4	5	6	7	9	10	11	12	13	14	16	17	18	19	20	21	23	24	25	26	27	28