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SPECIFICATION

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APPLICABLE DIVISION
■ Mobile LCD Group I

DEVICE SPECIFICATION FOR

CG-Silicon TFT-LCD module

MODEL No. LS035B7UG01C

☐ CUSTOMER'S	APPROVAL
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DATA	
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PRESENTED

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$\underline{\text{RECORDS OF REVISION}}$

MODEL No: LS035B7UG01C

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2009.06.12	MB1-1 C096-027	-	-	1st Issue
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Others

- (1) The liquid-crystal is deteriorated by ultraviolet rays. Do not leave it in direct sunlight and strong ultraviolet rays for many hours.
- (2) If it is kept at a temperature below the rated storage temperature, it becomes coagulated and the panel may be broken. Also, if it is kept at a temperature above the rated storage temperature, it becomes isotropic liquid and does not return to its original state. Therefore, it is desirable to keep it at room temperature as much as possible.
- (3) If the LCD breaks, don't put internal liquid crystal into the mouth. When the liquid crystal sticks to the hands, feet and clothes, wash it out immediately.
- (4) Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.
- (5) Observe general precautions for all electronic components.
- (6) Epoxy resin (amine series curing agent), silicone adhesive material (dealcoholization series and oxime series), tray forming agent (azo compound) etc, in the cabinet or the packing materials may induce abnormal display with polarizer film deterioration regardress of contact or noncontact to polarizer film. Be sure to confirm the component of them.
- (7) Use after you examine it fully because when liquid crystal is included into the product, stress such as a twist is added, and it becomes the cause which glass broken and brightness occasion unevenness occur in when condition is taken.

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(1) Application

This literature applies to LS035B7UG01C.

(2) Overview

This module is a color reflective and active matrix LCD module incorporating CG silicon TFT (Thin Film Transistor), named AD-TFT(Advanced TFT). It is composed of a color TFT-LCD panel, driver ICs, an FPC, a back light.

Graphics and texts can be displayed on a $320 \times 3 \times 480$ dots panel with 262,144 colors by supplying. Optimum view angle is 1:30 o'clock (direction: driver on the top).

(3) General specifications

Table 1. Description

Parameter	Specifications	*Remarks
LCD Type	Normally White, Transflective ECB TFT	
Screen size (Diagonal)	3.54"	
Pixel format	$320(H) \times 480(V)$	
	$(1 \text{ pixel} = R+G+B \text{ dots}) \dots RGB \text{ vertical stripe}$	
Pixel pitch	0.052 (H) × 0.156 (V) mm	
Top Polarizer	Anti Reflection(LT4), Hard coat	
	34%-Haze in adhesive	
Interface	MPL&SPI	
Display active area	49.92(H) × 74.88(V) mm	
Unit outline dimension	$55.22(W) \times 82.88(H) \times 1.85(D) \text{ mm (Typ.)}$	【Note3-1】
Mass	13.5 gram (Typ.)	
BTB connector on the FPC	SMK CPB7324-0250F(receptacle), 24Pin	

^{*}Remarks

[Note 3-1]

Excluding protrusion. For detailed measurements and tolerances, please refer to Drawing No.LDM-03336A.



(4)Input/Output terminal

4-1)TFT-LCD panel driving section

The pin connections are provide in Table2. The interface connector is a 24pin board-to-board connector mounted on the FPC tail.

Table2. Pin Assignment

Pin No.	Symbol	I/O	Description	Remarks
1	VDDA	-	Display voltage	5.8V typical
2	LED-	-	LED Cathode	
3	GND	-	Ground	
4	LED+	-	LED Anode	
5	MPL_PD_N	I	MPL Link Power Down	Active Low
6	NC	-	No connect	
7	FLM	0	First Line Marker (XFER)	PE parity error for MPL interface testing
8	IND	О	Timing back to MLB	340kHz
9	RESET	I	Reset	Active Low
10	GND	-	Ground	
11	GND	-	Ground	
12	SCS	I	SPI Chip Select	Active Low
13	MD0	I	MPL DATA	MPL Interface
14	SCLK	I	SPI DATA	
15	GND	-	Ground	
16	SDI	I	SPI DATA In	
17	MC	I	MPL CLK	MPL Interface
18	SDO	O	SPI DATA Out	
19	GND	-	Ground	
20	NC	-	No Connect (Open)	
21	MD1	ı	MPL DATA	MPL Interface
22	VDDD	-	Logic Power Supply	1.8V
23	GND	-	Ground	
24	VDD_DC	-	DC to DC Power Supply	3.0V

Used BTB receptacle connector (LCM side): 0.4mm pitch CPB7324-0259E (SMK)

Corresponding connector (User side): CPB7424-0250F (SMK)

Recommended MPL transmitter: LM2512A(National Semiconductor)

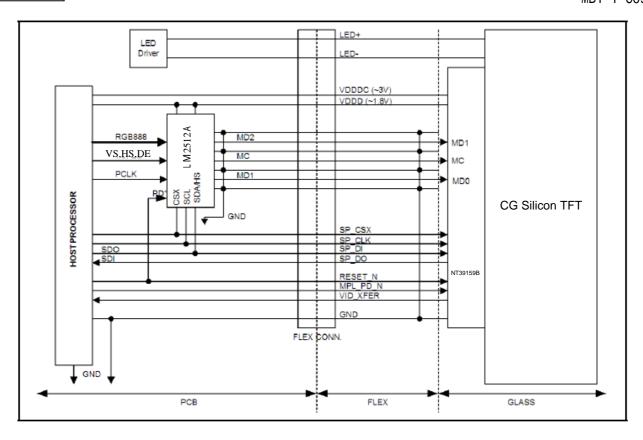


Figure 1. MPL1 signal connections

(5) Absolute Maximum Ratings

Table 3. Absolute Maximum Rating

Table 5. Absolute Maximum Nating							
Parameter	Symbol	Ratings	Unit	Remark			
Supply voltage for LCD	V_{DDDC}	- 0.3 ~ +4.0	V				
Supply voltage for Logic I/O	$V_{ m DDD}$	- 0.3 ~ +2.5	V				
VDDA Voltage	V_{DDA}	6.0	V				
Logic Input Voltage	$V_{\rm IN}$	$-0.3 < V_{\text{IN}} < V_{\text{DDD}} + 0.3$		【Note3-1】			
LED Power Consumption	P_{LED}	120	mW	【 Note3-2 】			
LED current	I LED	35	mA				
Operating temperature (panel	Тор	- 20 ~ +70		【Note3-3】			
Storage temperature	T _{stg}	- 30 ~ +80					
Humidity	Н	5% ~ 95%	RH				

^{*}Remarks

[[]Note3-1] Applies to RESET, SCS, SCLK, SDI, SDO, and FLM. [Note3-2] Applies for each LED individually [Note3-3] Humidity: 95%RH Max, non-condensing>40

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(6)Block Diagram & Window Address

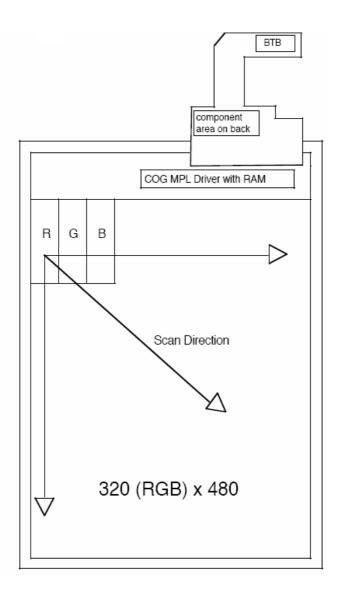


Figure 2. Display Block diagram

^{*}please refer to Drawing No.LDM-03336A.

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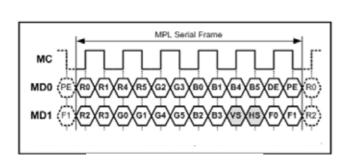
(7)Color Input Reference & Data Transfer

The Brightness of each primary color (R,G,B) is based on the 6-6-6 bit gray scale data respectfully input for the color. The display outputs 18-bit color data. The higher the binary input, the brighter the color. Table3 below provides a reference for color versus data input.

Table4. Color vs DATA

Colors &	Gray									ata :	Signa	al							
Gray	scale	R	R	R	R	R	R	G	G	G	G	G	G	В	В	В	В	В	В
Scale	Level	0	1	2	3	4	5	ō	1	2	3	4	5	ō	1	2	3	4	5
	S		_				_	_							_				
Black		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Blue	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Green		0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Cyan		0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
Red		1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Magenta		1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
Yellow		1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
White		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	GS1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Darker	GS2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	+				+						,					+			
	↓				<u> </u>					↓						<u> </u>			
J. J.	GS61	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	GS62	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Red	GS63	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	GS1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Darker	GS2	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	+				+						r								
Brighter	+		-	_		-	-		-			-			-	<u>+</u>	_		
Jingincei ↓	GS61	0	0	0	0	0	0	1	0	1	1	1	1	0	0	0	0	0	0
-	GS62	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0
Green	GS63	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
Black	GS0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Darker	GS1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Darker	GS2	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
	+				+						,					*			
Brighter	CC61	0	0	0	0	_	0	0	0		0	0	0	-	0	¥	1	1	-
	GS61 GS62	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Blue	GS62 GS63	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
Blue	0503	U	U	U	U	U	U	٥	U	U	U	U	U	1	ĹŢ	Ι.	1	Ι.	Т

<Transfer 24-bit to 18-bit Dithered, 2 MD Lane, RGB Transaction>



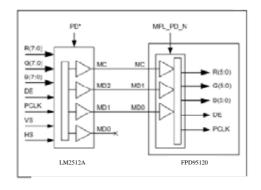


Figure 3. MPL Data Frame*

Figure 4. 2 Lane MPL Interface

*MD0 and MD1 of NT39159 correspond to MD1 and MD2 of LM2512A

(8) Electrical characteristics

8-1) Recommended operating conditions

a) TFT-LCD panel driving section

Table 5. Electrical Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit	Notes
LCD Supply Voltage	VDDDC-VSS	2.85	3.0	3.15	V	
Logic I/O Voltage	VDDD-VSS	1.65	1.80	1.95	V	【Note8-2】
VDDA Voltage	VDDA	5.68	5.80	5.92	V	
VDDA ripple Voltage		-	-	25	mV	【Note8-6】
Panel Input Current	IDDDC +IDDD	-	9	10	mA	【Note8-1】
LED Input Current	$I_{ m LED}$	-	20	25	mA	
VDDA current	IVDDA	-	5.5	-	mA	
"H" Level Input Voltage	V_{IH}	0.8VDDD	-	-	V	
"L" Level Input Voltage	V_{IL}	-	-	0.2VDDD	V	【Note8-2】
"H" Level Output Voltage	V_{OH}	0.8VDDD	-	-	V	[Noteo-2]
"L" Level Output Voltage	V_{OL}	-	-	0.2VDDD	V	
Driver Power Supply Stability		-	-	250	ms	【Note8-5】
Inrush Current (3V supply)				200	mA	
MPL Line Impedance		45	55	60	Ohm	
Power, MPL full refresh	P MPL	-	53	-	mW	【Note8-1】
Power, Backlight	PВ	-	384	420	mW	【Note8-3】
Power, Sleep mode	PS	-	-	60	μW	【Note8-4】

*Notes

[Note 8-1] Conditions: VDDDC=3.0V, VDDD=1.8V, VDDA=5.8V, T=25, 60Hz frame rate/frequency, Black fill pattern is displayed, and line inversion used.

- [Note 8-2] Input mode of RESET, SCS, SCLK and SDI. Output mode of SDO and FLM
- [Note 8-3] LED Backlight assumptions; 3.2Vf, 20mA, 6LED's.
- [Note 8-4] VDDDC&VDDD are present; RESET is high.
- [Note 8-5] Time from VDDDC & VDDD applied until driver power supplies are stable.
- [Note 8-6] VDDA generated circuit is introduced in Figure 5. (Reference)

SHARP is using this VDDA generated circuit for LCM display inspection's MP line (setup).

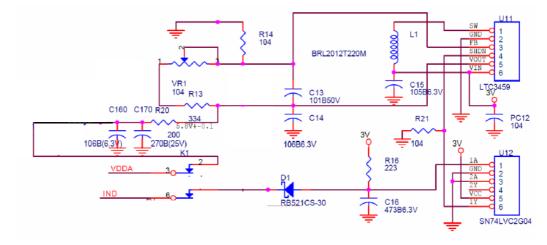


Figure 5. (Reference) V_{DDA} generated circuit



8-2) Timing diagrams of input signals

a) Write/Read timing

The system input timing characteristics are provides in Table 5 and illustrated in Figure 6.

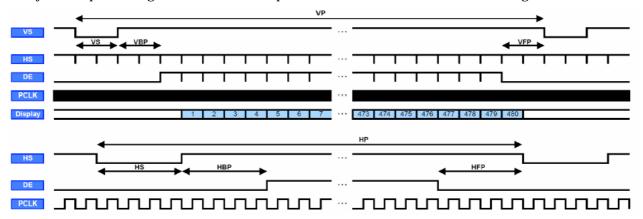


Figure 6. Timing Characteristics

Table 6. Interface Timing Characteristics

Item	Symbol	Timing	unit	Notes
Vertical cycle	VP	492	Line	
Vertical low pulse width	VS	4	Line	
Vertical front porch	VFP	4	Line	
Vertical back porch	VBP	4	Line	
Vertical display area	VDISP	480	Line	
Horizontal cycle	HP	366	clk	
Horizontal low pulse width	HS	4	clk	【Note8-6】
Horizontal front porch	HFP	22	clk	
Horizontal back porch	HBP	20	clk	
Horizontal display area	HDISP	320	clk	
Pixel Clock	fPCLK	10.80	MHz	
	tPCLK	92.6	ns	

^{*}Notes

[Note 8-6] VDD= $2.85\sim3.15V$, VEE= $1.65\sim1.95V$

(9)Software Flow & Register Settings

9-1) Software Flow

The LCM for LS035B7UG01 displays all follow the basic software flowchart illustrated Figure 7 and in the following Tables.

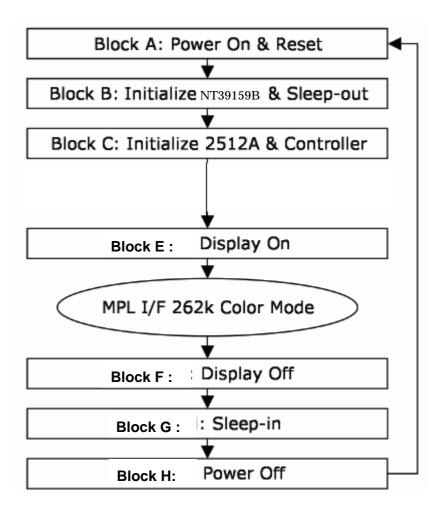


Figure 7. Software Flowchart

9-2) Register Settings

Table 7. Block A: Power On & RESET

Step	Operation
1	Power switched on to VDDD & VDDDC simultaneously
2	MPL_PD_N=0 "L"
3	PWRDWN_2512A=0 "L" (LM2512A Power OFF)
4	RESET=1 "H \rightarrow L"
5	Delay 10ms
6	RESET=0 "L → H"
7	PWRDWN_2512A=1 "L → H" (LM2512A Power ON)
8	Delay 10ms

Power to VDDDC and VDDD are switched on simultaneously.

The sequence for power on is shown in Figure 8.

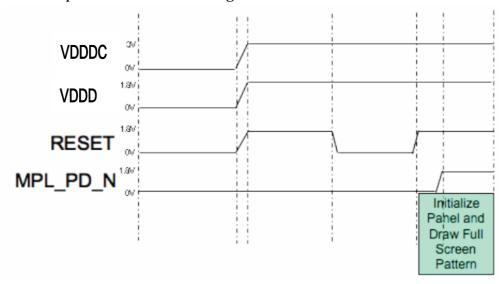


Figure 8. Power On Sequence

Table8. Block B: Initialize NT39159B & Sleep-out

Step	Regster / Command	Parameter / Setting	Operation					
1		DE= " L → H "						
2		Turn on LCD Signals (RGB interface from controller to LM2512A)						
3	5F	01 Command Mode						
4		Delay 10ms						
5	OP 11h - Sleep Out							
6		MPL_PD_N= 1 " H "						

Table 9. Block C: Initialize LM2512A & Controller

Step	Regster /	Parameter /	
	Command	Setting	Operation
1			MPL_PD_N=1 " H "
2	2512A 16h	FFh	Unlock LM2512A (locks NT39159B)
3	2512A 00h	10h	Enable access to LM2512A registers
4	2512A 0Ah	02h	Forces 2 Lane Config
5	2512A 08h	01h	Bipass dithering
6	2512A 02h	00h	Red ram address
7	2512A 03h	00h	Red ram data
8	2512A 04h	00h	Green ram address
9	2512A 05h	00h	Green ram data
10	2512A 06h	00h	Blue ram address
11	2512A 07h	00h	Blue ram data
12	2512A 01h	10h	MPL slow edge rate
13	2512A 16h	00h	Unlock NT39159B (Locks LM2512A)
14			Delay 1 ms

Table 10. Block D: Display Settings (MTP Data)

Step	Regster / Parameter /				
	Command		Setting	Operation	
1	1D		94	SCAN	
2	1E		17	INVERSION_MODE	
3	1F		11	CKH1_HI_PM	
4	20		11	CKH_HI_PM	
5	21		04	CKH_NOV_PM	
6	22		09	DE_CKH1_PM	
7	23		01	DE_GOE_RE_PM	
8	24		C8	MODE	
9	25		11	CKH1_HI	
10	32		11	CKH_HI	
11	33		04	CKH_NOV	
12	34		09	DE_CKH1	
13	35		01	DE_GOE_RE	
14	37		91	DE_CKV	
15	3B		00	DE_VCOM	
16	3C		01	STV_CTL	
17	3D		91	DE_CKV_PM	
18	3E		00	DE_VCOM_PM	
19	3F		A8 COL_OFFSET		
20	40		Dx	OSC_PER_LINE_LSB	
21	41		Fx	LINE_PER_FRAME_LSB	
22	42		01	OPL_LPF_MSBS	
23	43		00	VDDGR_ADJ	
24	44		00	VDD_ADJ	
25	45		00	GVDD_ADJ	
26	46		00	VCOMDC_ADJ	
		Bin1	31		
		Bin2	28		
27	47	Bin3	17	VCOMH_ADJ	
		Bin4	0B	1	
28	48		41	VCOML_ADJ	
29	49		00	VX_RISE	
30	4A		01	VX_FALL	

				WIDT-1 COS
31	4B		00	VCOM_MODE
32	52		C0	GAMMA_CFG1
33	55	03		BLANK
34	60	A1		WRID1
35	61		D1	WRID2
36	62		2B	WRID3
37	63		00	PWCTR1
38	64		07	PWCTR2
39	65		00	PWCTR3
40	66 67		<u>08</u> 26	PWMCTRL1 PWMCTRL2
41	07	Bin1	1004700300F00F0170	F WINC I KLZ
		Bin2	0004710301F00F03BA	
42	68			GAMCTRP0
		Bin3	3005421301F0050273	
		Bin4	0017321305D00400D8	
	69	Bin1	4F7037F601FF000007	
43		Bin2	4F6037F703FF0001AB	GAMCTRN0
		Bin3	4E5327F402F5000137	
		Bin4	4E5406F700D400058D	
	6A	Bin1	1004722200F00F01D0	
44		Bin2	0005720401F00F03D6	GAMCTRP1
11		Bin3	6007751201A00700B1	G/M/ICTIVI I
		Bin4	4007640003800600E8	
		Bin1	5D5037F601FF00000D	
45	op.	Bin2	3F5027F703FF00016D	CAMCEDNIA
45	6B	Bin3	5E2007F100A700011B	GAMCTRN1
		Bin4	7F3107F3008600038E	
		Bin1	2007717700F20F0104	
	0.7	Bin2	1007715704F20F033A	an compa
46	6C	Bin3	7007310701F9050020	GAMCTRP2
		Bin4	4007000406D6030088	
		Bin1	086007F501FF020040	
.~	0.5	Bin2	0A6007F603FF0204A3	CANCEDIA
47	6D	Bin3	0F6407F000F5090102	GAMCTRN2
		Bin4	3F7707F300D3060688	

One of the $4^{\rm th}$ gannma curve set (Bin1,2,3,4) is applied to each LCM. Adjusting driven voltage for LC is covered acceptable optical specification.

Table11. Block E: Display On

Step	Regster /	Parameter /				
	Command	Setting	Operation			
1	OP DEh	-	Enter Register Access Mode			
2	50	01	CAL_SEL Setting(Continuous)			
3	5F	01	01 Command Mode			
4		Delay 10ms				
5	OP 29h	-	Display On command (alternatively write setting 00h			
			to register 55h to blank in register Access mode)			
6			Turn Backlight On			

Table 12. Block F: Display Off

Step	Regster / Command	Parameter / Setting	Operation			
1			Turn Backlight Off			
2	5F	01	Command Mode			
3	Delay 10ms					
4	OP 28h	-	Display off			
5			Delay 40ms			

Table13. Block G: Sleep In

Step	Regster / Command	Parameter / Setting	Operation				
1	5F	01	Command Mode				
	Delay 10ms						
2	OP 10h	-	Sleep in				
3	Delay 70ms						

Table 14. Block H: Power Off

Step	Regster /	Parameter /					
	Command	Setting	Operation				
1		Turn off L	CD Signals (RGB interface from controller to LM2512A)				
2			DE= " H → L "				
3	MPL_PD_N = 0 " H → L "						
4	Delay 100ms						
5	RESET =1 "H → L"						
6	Delay 1ms						
7	PWRDWN_2512A=0 " Sleep Mode "						
8		Power d	own simultaneously or 3V supply first then 1.8V logic				

Power to VDDC and VDDD is removed.

The sequence for power on is shown in Figure 9.

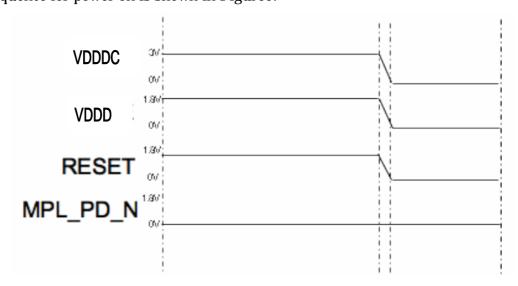


Figure 9. Power Off Sequence

(10)Optical characteristics

10-1)Not driving the Back light condition

Table 15. Optical Characteristics - Backlight OFF

VDDDC=3.0V、VDDD=1.8 V、VDDA=5.8V

Ta=25°C

Parameter	Symbol	Condition	Min	Тур	Max	Unit	Remarks
	$\theta_{ ext{LEFT}}$		45	-	-		DV - 40 4 01
V:	θ_{UP}	CD>0	45	-	-	0(-]	
Viewing angle range	$\theta_{ m RIGHT}$	CR≥2	45	-	-	°(degree)	[Note 10-1,2]
	θ_{DOWN}		45	-	-		
Contrast ratio	CR	Optimal	6	8	-	-	[Note 10-1,2]
Reflectivity	R	Optimal	1.15	1.8	2.5	%	[Note 10-5]
Response rise time	r	=0 °	-	5	7	ms	[N]10.4]
Response fall time	d	Ta=25	-	10	11	ms	[Note 10-4]
Wilette Clement at attent	X	CIE	0.290	0.310	0.330		
White Chromaticity	Y		0.316	0.336	0.356		
Ded Classes at the	X	CIE	0.398	0.425	0.452		
Red Chromaticity	Y		0.297	0.322	0.347		[Note10-3]
Green	X	CIE	0.275	0.300	0.325		
Chromaticity	Y	CIE	0.375	0.395	0.415		
Blue Chromaticity	X	CIE	0.196	0.227	0.258		
	Y	CIE	0.193	0.227	0.261		

- * The display is oriented landscape with this driver in the upper side.
- * The measuring method of the optical characteristics is shown by the following figure.
- * A measurement device is DMS diffuse measurement system.

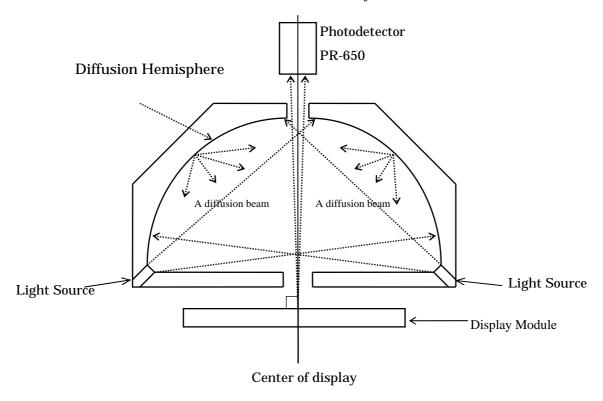


Figure 10. Measuring method for reflective optical characteristics

10-2)Driving the Back light condition

Table 16. Optical Characteristics – Backlight ON

VDDDC=3.0V、VDDD=1.8 V、VDDA=5.8V

Ta=25°C

VDDDC=3.0V、VDDD=1.8 V、VDDA=5.8V Ta=25°C							
Parameter	Symbol	Condition	Min	Тур	Max	Unit	Remarks
	$\theta_{ ext{LEFT}}$		50	60	-		[Note 10-1,2]
	$\theta_{ ext{UP}}$	CR≥10	50	60	-		
	θ_{RIGHT}		50	60	-		
Contrast Viewing	θ_{DOWN}		45	55	-	Degrees	
Angle Range	θ1:30	CIVZIU	50	60	-	Degrees	[Note 10-1,2]
	θ4:30		50	60	-		
	$\theta_{7:30}$		45	55	-		
	θ10:30		50	60	-		
	$\theta_{ ext{LEFT}}$		50	60	-		
	θ_{UP}		50	60	-		
	$\theta_{ m RIGHT}$	High Gray	50	60	-		
No High Gray Level	θ_{DOWN}	Level =	50	60	-	.	[37 · 40 4 0]
Inversion Angle	θ1:30	lighter	45	55	-	Degrees	[Note 10-1,2]
(White Level)	θ4:30	shades	50	60	-		
	θ7:30		25	35	-		
	θ10:30		50	60	-		
	$\theta_{ ext{LEFT}}$		50	60	-	Degrees	[Note 10-1,2]
	θυР		45	55	_		
	θright	Low Gray	50	60	_		
No Low Gray Level	θ _{DOWN}	Level =	50	60	_		
Inversion Angle	θ _{1:30}	darker shades	30	40	_		
(Black Level)	θ4:30		50	60	_		
	θ7:30		50	60	_		
	θ10:30		50	60	_		
Contrast ratio	CR	Optimal	150	180	_		[Note10-1,2]
Brightness	Y	Optimal	450	550	_	cd/m ₂	[[1000010 1,2]
Brightness Uniformity	Y	Optimal	85	-	_	%	[Note 10-6]
Gamma		Optimal	-	2.2	_	70	[TVOCC TO O]
Blue Shift (including	Х	Optimal			0.000		
RGB gamma			-	-	0.030		
correction)	У	Optimal	-	-	0.050		
Flicker	F	Optimal	-	-	6	%	[Note 10-7]
Cross Talk	D _{SHA}	Optimal	-	-	4	%	[Note 10-8]
Viewing Direction			-	7:30	-	o'clock	[Note 10-1]
Response rise time	тr	$\theta = 0^{\circ}$	-	6	8	ms	
Response fall time	тd	Ta = 25	-	17	20	ms	[Note 10-4]
with all the second	X	- CTE	-	0.312	-		
White Chromaticity	Y	CIE		0.338	-		

D 101	X	GVF.	-	0.609	-		
Red Chromaticity	Y	CIE	-	0.355	-	-	
G Gl	X	CIE	-	0.326	-	-	
Green Chromaticity	Y		-	0.560	-	-	
Blue Chromaticity	X	CIE	-	0.150	-	-	
	Y	CIE	-	0.122	-	-	

 $[\]ensuremath{^*}$ The display is oriented landscape with his driver in the upper side.

^{*} A measurement device is TOPCON luminance meter SR-3.(Viewing cone 1)

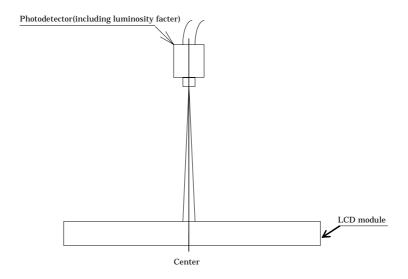


Figure 11. Measuring method for transmitance optical characteristics

 $^{^{\}ast}$ The measuring method of the optical characteristics is shown by the following figure.

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*Remarks

[Note 10-1] Viewing angle range is defined as follows.

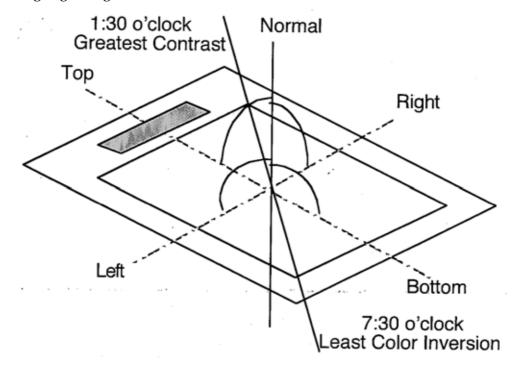


Figure 12. Definition for viewing angle

[Note10-2] Definition of contrast ratio:

The contrast ratio is defined as follows:

Photodetector output with all pixels white (GS63)

Contrast ratio(CR)= -

Photodetector output with all pixels black (GS0)

[Note10-3] A measurement device is Minolta CM-2002.

[Note10-4] Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white".

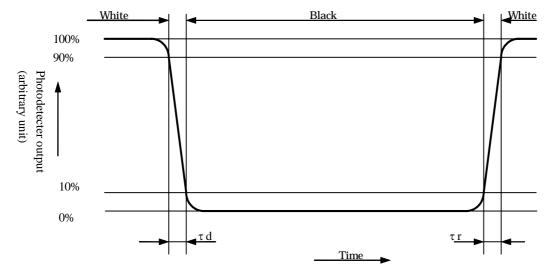


Figure 13. Response Time Diagram

 $[Note 10-5] \quad \begin{array}{ll} Definition \ of \ reflection \ ratio \\ Reflectivity &= \frac{Light \ level \ of \ reflection \ from \ display \ with \ all \ white \ pixels}{Light \ level \ of \ reflection \ from \ reflective \ standard} \end{array}$

[Note10-6] Definition of Brightness & Brightness Uniformity

The brightness should be measured on 13spots of the display as follows.

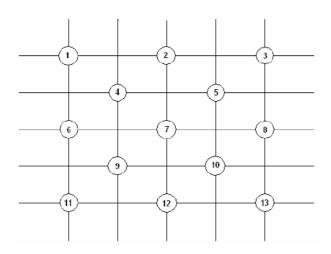


Figure 14. Brightness measurement points

[Note10-7] Flicker

The Flicker level is measured with horizontal stripes with every other line black and middle gray(V31).

And, Flicker is measured in the center of the active area of the LC display.

The flicker is the ratio of the power in the frequency spectrum at 30Hz(Px) to the power at 0Hz(P0) in percent:

Flicker =
$$\frac{\text{The power in the frequency spectrum at 30Hz (Px)}}{\text{The power in the frequency spectrum at 0Hz}} \times 100\%$$

The frame frequency of the panel is set to 60Hz and VDD is set to 3.0V.

[Note10-8] Cross-Talk

To perform crosstalk measurement, two luminance values are measured at the center spot with 50×50 pixels. The cross-talk, D_{SHA} , is defined as:

$$D_{SHA} = \left(\frac{(L_B - L_A)}{L_B}\right) x 100\%$$
 Where, L_A = Luminance in Pattern A L_B = Luminance in Pattern B.

Pattern A Pattern B

Pattern B

Gray Scale = 31 in center Black in surrounding area

Figure 15. Cross-talk measurement

(11)Display quality

The display quality of the color TFT-LCD module shall be in compliance with the Incoming Inspection Standards for TFT-LCD.

(12) Mechanical characteristics

12-1) External appearance

See Drawing No.LDM-03336A

12-2) FPC bending characteristics

(1)Specific connector

CPB7324-0250F (SMK)

(2)Bending endurance of the bending slits portion

This FPC guarantees the folding number of times in each place.

Bend Area A: +90 ° ~ -90 ° 3 cycles Bend Area B: +180 ° ~ 0 ° 3 cycles Bend Area C: +90 ° ~ -90 ° 3 cycles

Must not bend it except for three territories.

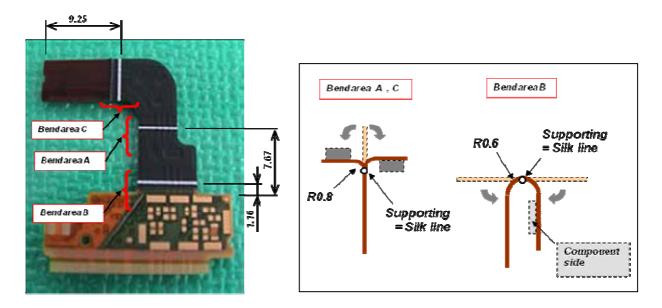


Figure 16. FPC bending Area (A,B,C)

(13) Handling Precautions

13-1) Insertion and taking out of FPCs

Be sure insert and take out of the FPC into the connector of the set after turning off the power supply on the set side.

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13-2) Handling of FPCs

The FPC for LCD panel shall be bent only slit portion. The bending slit shall be bent uniformly on the whole slit portion with bending radius larger than 0.6mm ,and only inner side (back side of the module). Don't bend it outer side (display surface side).

Don't give the FPCs too large force, for example, hanging the module with holding FPC.

13-3) Installation of the module

On mounting the module, be sure to fix the module on the same plane. Taking care not to warp or twist the module.

13-4) Precaution when mounting

- (1) If water droplets and oil attaches to it for a long time, discoloration and staining occurs. Wipe them off immediately.
- (2) Glass is used for the TFT-LCD panel. If it is dropped or bumped against a hard object, it may be broken. Handle it with sufficient care.
- (3)As the CMOS IC is used in this module, pay attention to static electricity when handling it. Take a measure for grounding on the human body.

13-5) Others

- (1) The liquid-crystal is deteriorated by ultraviolet rays. Do not leave it in direct sunlight and strong ultraviolet rays for many hours.
- (2) If it is kept at a temperature below the rated storage temperature, it becomes coagulated and the panel may be broken. Also, if it is kept at a temperature above the rated storage temperature, it becomes isotropic liquid and does not return to its original state. Therefore, it is desirable to keep it at room temperature as much as possible.
- (3) If the LCD breaks, don't put internal liquid crystal into the mouth. When the liquid crystal sticks to the hands, feet and clothes, wash it out immediately.
- (4) Wipe off water drop or finger grease immediately. Long contact with water may cause discoloration or spots.
- (5) Observe general precautions for all electronic components.

(14) Reliability Test Conditions for CGS TFT-LCD Module

Table 17. Reliability Test Conditions

Table I	7. Reliability Test Conditions				
No.	Test items	Test conditions			
1	Low Temperature Storage Test	Ta= - 30	240h		
2	High Temperature Storage test	Ta=+80	240h		
3	High Temperature and High Humidity Storage Test	Ta=+60 , 90%RH	240h		
4	Thermal Shock Storage Test	$Ta = -30 : 15min \sim 80 : 15min$	50cycles		
5	Low Temperature Operating Test	Ta= - 20	240h		
6	High Temperature Operating Test	Ta=+70	240h		
7	High Temperature and	Ta=+50 , 90%RH	240h		
	High Humidity Operating Test				
8	Four Corner Test	Ta=+50 10%RH, Ta=+50 90%RH Ta=+10 10%RH, Ta=+10 90%RH	72h		
9	Electrostatic Discharge Test	250V 200pF,(MM method)1 time for each termina including EEPROM programming test point			
10	Shock Test	At least 5000G in a half sine pulse of 0.50+/ - 0.20ms at each 6 sides (MIL-STD-202F Method 213B,test condition A)			
11	Vibration Test 3G from 5-500Hz random for 30 minutes (MIL-STD-202F, method A)				

[Note] Ta = Ambient temperature

[Check items] Test No.1 \sim 11 : In the standard condition, there shall be no practical problems that may affect the display function.

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(15) Others

15-1) Indication of lot number

The lot number is printed in the position shown in Drawing No.LDM-03336A. (Outline Dimensions).

15-2) Used Regulation of Chemical Substances Breaking Ozone Stratum

Substances with the object of regulating: CFCS, Carbon tetrachloride.

1,1,1-Trichloro ethane (Methyl chloroform)

- (a) This LCD module, Constructed part and Parts don't contain the above substances.
- (b) This LCD module, Constructed part and Parts don't contain the above substances in processes of manufacture.

15-3) If some problems arise about mentioned items in this document and other items, the user of the TFT-LCD module and Sharp will cooperate and make efforts to solve the problems with mutual respect and good will.

(16) Forwarding form

a) Piling number of cartons: 8deep

b) Package quantity in one cartons: 320 (pcs)

c) Carton size: (w) 525×(D) 360×(H) 225 (mm)

d) Total mass of 1 carton filled with full modules: approximately 9.8 (Kg)

Conditions for storage

Environment

(1) Temperature : $0 \sim 40$

(2) Humidity : 60%RH or less (at 40)

No dew condensation at low temperature and high humidity.

(3)Atmosphere : Harmful gas, such as acid or alkali which bites electronic

components and/or wires, must not be detected.

(4)Period : about 3 months

(5)Opening of the package : In order to prevent the LCD module from breakdown by

electrostatic charges, please control the room humidity over 50%RH and open the package taking sufficient countermeasures against electrostatic charges, such as

earth, etc.

