

*Designer's Data Sheet*

**TMOS IV**

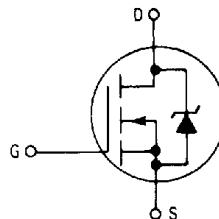
**Power Field Effect Transistor**

**N-Channel Enhancement-Mode**

**DPAK for Surface Mount or Insertion Mount**

This advanced "E" series of TMOS power MOSFETs is designed to withstand high energy in the avalanche and commutation modes. These new energy efficient devices also offer drain-to-source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

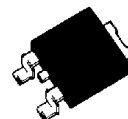
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode — Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C.
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits.
- Source-to-Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode.
- Diode is Characterized for Use in Bridge Circuits.
- Available With Long Leads, Add -1 Suffix



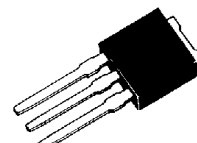
**MTD10N05E**

Motorola Preferred Device

TMOS POWER FETs  
 10 AMPERES  
 $R_{DS(on)} = 0.1 \text{ OHM}$   
 50 VOLTS



CASE 369A-10  
 TO-252  
 MTD10N05E



CASE 369-06  
 TO-251  
 MTD10N05E1

**MAXIMUM RATINGS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	50	Vdc
Drain-Gate Voltage ( $R_{GS} = 1 \text{ M}\Omega$ )	$V_{DGR}$	50	Vdc
Gate-Source Voltage — Continuous — Non-repetitive ( $t_p \leq 50 \mu\text{s}$ )	$V_{GS}$ $V_{GSM}$	$\pm 20$ $\pm 40$	Vdc Vpk
Drain Current — Continuous — Pulsed	$I_D$ $I_{DM}$	10 24	Adc
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	20 0.16	Watts W/°C
Operating and Storage Temperature Range	$T_J, T_{stg}$	-65 to 150	°C

**THERMAL CHARACTERISTICS**

Thermal Resistance — Junction to Case — Junction to Ambient — Junction to Ambient (1)	$R_{\theta JC}$ $R_{\theta JA}$	6.25 100 71.4	°C/W
Maximum Device Temperature for Soldering Purposes (for 5 seconds maximum)	$T_L$	260	°C

(1) These ratings are applicable when surface mounted on the minimum pad size recommended (continued)

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design

**Preferred** device is a Motorola recommended choice for future use and best overall value.

**ELECTRICAL CHARACTERISTICS** ( $T_C = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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**OFF CHARACTERISTICS**

Drain-Source Breakdown Voltage ( $V_{GS} = 0, I_D = 0.25 \text{ mA}$ )	$t$	$V_{(BR)DSS}$	50	—	Vdc
Zero Gate Voltage Drain Current ( $V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$ ) ( $V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$ )		$I_{DSS}$	—	10 100	$\mu\text{A}$
Gate-Body Leakage Current, Forward ( $V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$ )		$I_{GSSF}$	—	100	nAdc
Gate-Body Leakage Current, Reverse ( $V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$ )		$I_{GSSR}$	—	100	nAdc

**ON CHARACTERISTICS\***

Gate Threshold Voltage ( $V_{DS} = V_{GS}, I_D = 1 \text{ mA}$ ) $T_J = 100^\circ\text{C}$		$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ( $V_{GS} = 10 \text{ Vdc}, I_D = 5 \text{ Adc}$ )		$R_{DS(on)}$	—	0.1	Ohm
Drain-Source On-Voltage ( $V_{GS} = 10 \text{ V}$ ) ( $I_D = 10 \text{ Adc}$ ) ( $I_D = 5 \text{ Adc}, T_J = 100^\circ\text{C}$ )		$V_{DS(on)}$	—	1.1 0.9	Vdc
Forward Transconductance ( $V_{DS} = 15 \text{ V}, I_D = 5 \text{ A}$ )		$g_{FS}$	4.5	—	mhos

**DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS**

Unclamped Drain-to-Source Avalanche Energy See Figures 16 and 17 ( $I_D = 24 \text{ A}, V_{DD} = 6 \text{ V}, T_C = 25^\circ\text{C}$ , Single Pulse, Non-repetitive) ( $I_D = 10 \text{ A}, V_{DD} = 6 \text{ V}, T_C = 25^\circ\text{C}, P.W. \leq 10 \mu\text{s}$ , Duty Cycle $\leq 1\%$ ) ( $I_D = 4 \text{ A}, V_{DD} = 6 \text{ V}, T_C = 100^\circ\text{C}, P.W. \leq 10 \mu\text{s}$ , Duty Cycle $\leq 1\%$ )		$W_{DSCR}$	—	5 6 2.5	mJ
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**DYNAMIC CHARACTERISTICS**

Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz})$ See Figure 14	$C_{iss}$	—	850	pF
Output Capacitance		$C_{oss}$	—	350	
Reverse Transfer Capacitance		$C_{rss}$	—	100	

**SWITCHING CHARACTERISTICS\* ( $T_J = 100^\circ\text{C}$ )**

Turn-On Delay Time	$(V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50 \text{ ohms})$ See Figure 18	$t_{d(on)}$	—	30	ns
Rise Time		$t_r$	—	90	
Turn-Off Delay Time		$t_{d(off)}$	—	45	
Fall Time		$t_f$	—	35	
Total Gate Charge	$(V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V})$ See Figure 15	$Q_g$	14 (Typ)	17	nC
Gate-Source Charge		$Q_{gs}$	7 (Typ)	—	
Gate-Drain Charge		$Q_{gd}$	7 (Typ)	—	

**SOURCE DRAIN DIODE CHARACTERISTICS\***

Forward On-Voltage	$(I_{FM} = 0.5 \text{ Rated } I_D,$ $dI_S/dt = 100 \text{ A}/\mu\text{s}, V_{GS} = 0)$	$V_{SD}$	1 (Typ)	2	Vdc
Forward Turn-On Time		$t_{on}$	Limited by stray inductance		
Reverse Recovery Time		$t_{rr}$	50 (Typ)	—	ns

\*Pulse Test Pulse Width =  $300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

# TYPICAL ELECTRICAL CHARACTERISTICS

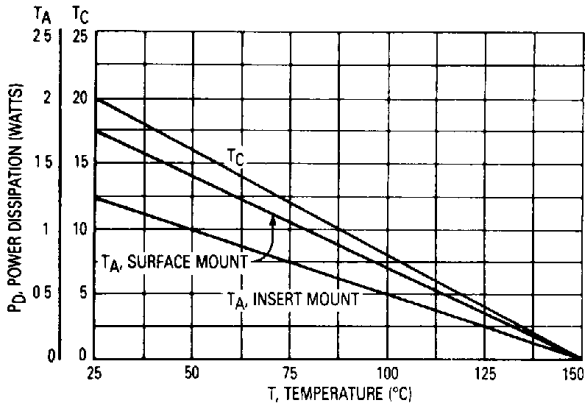


Figure 1. Power Derating

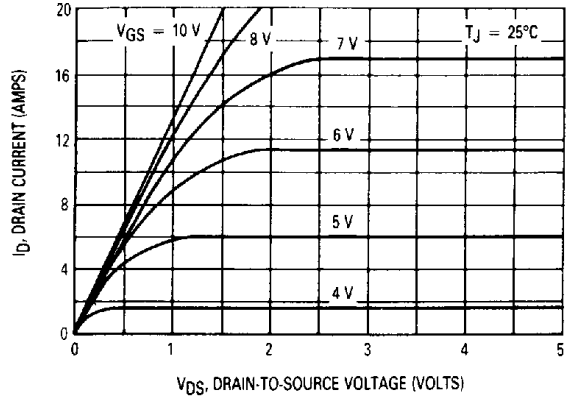


Figure 2. On-Region Characteristics

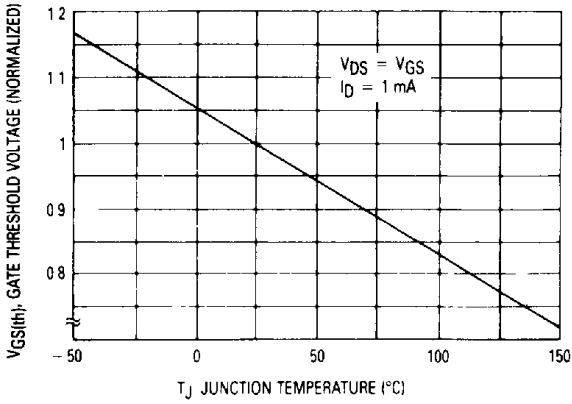


Figure 3. Gate-Threshold Voltage Variation With Temperature

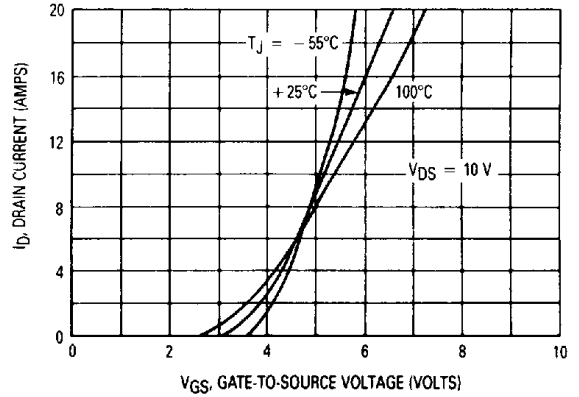


Figure 4. Transfer Characteristics

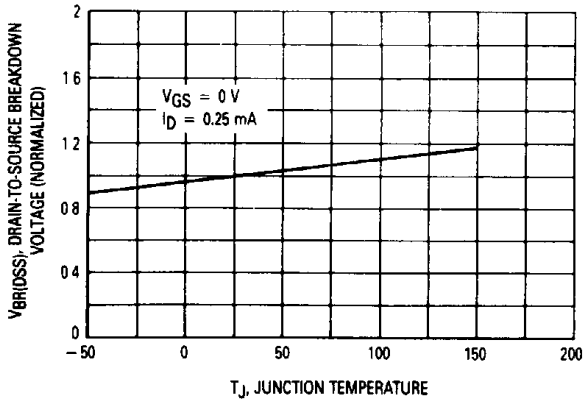


Figure 5. Breakdown Voltage Variation With Temperature

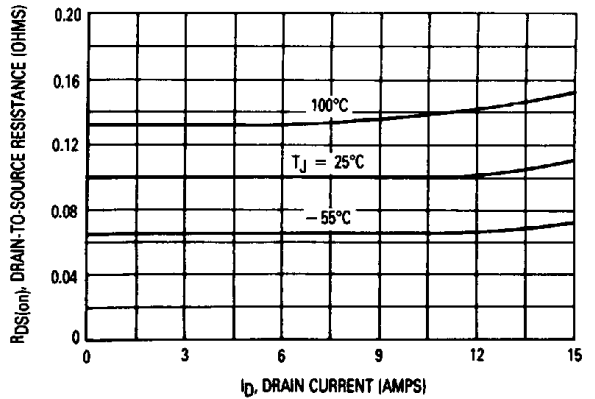


Figure 6. On-Resistance versus Drain Current

# SAFE OPERATING AREA INFORMATION

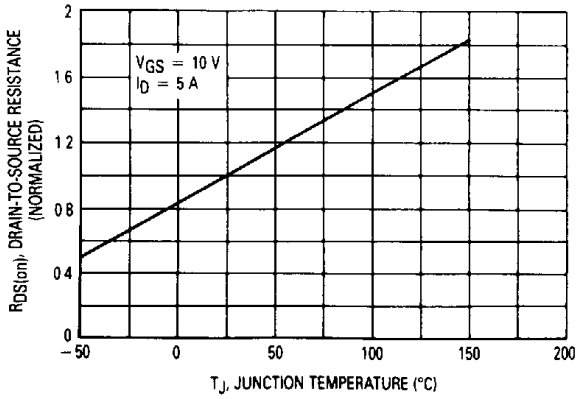


Figure 7. On-Resistance Variation With Temperature

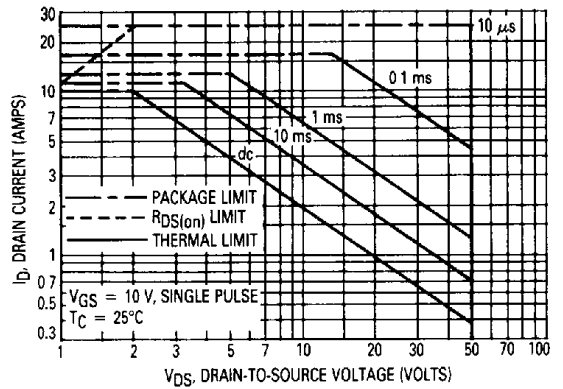


Figure 8. Maximum Rated Forward Biased Safe Operating Area

## FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of  $25^{\circ}C$  and a maximum junction temperature of  $150^{\circ}C$ . Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

## SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 9 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current,  $I_{DM}$  and the breakdown voltage,  $V_{(BR)DSS}$ . The switching SOA shown in Figure 9 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

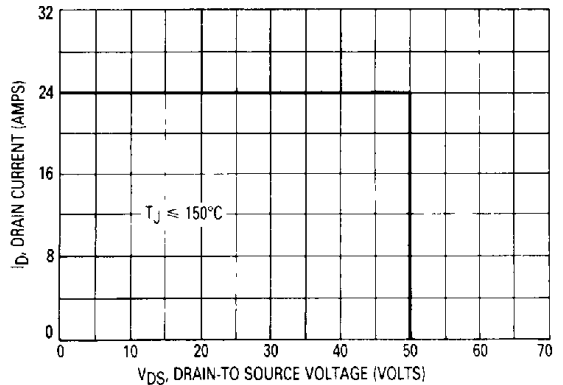


Figure 9. Maximum Rated Switching Safe Operating Area

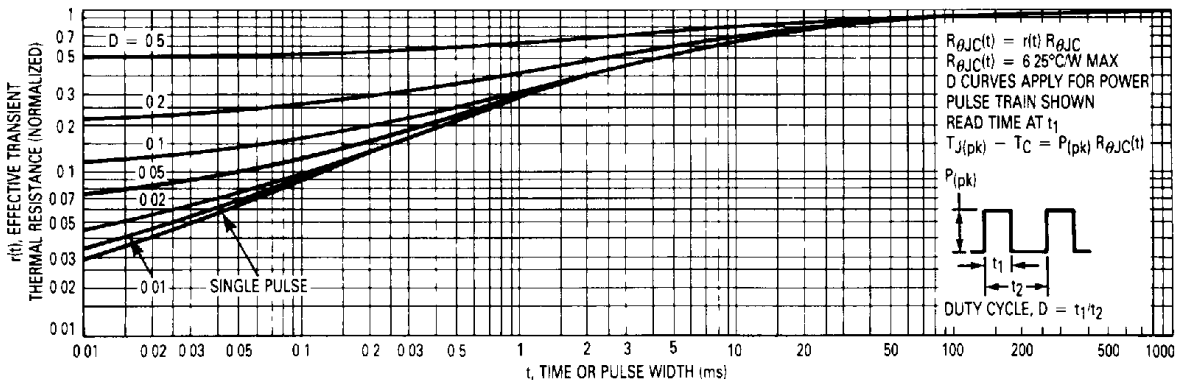


Figure 10. Thermal Response

## COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of  $I_{FM}$  and peak  $V_R$  for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval  $t_{frr}$  is the speed of the commutation cycle. Device stresses increase with commutation speed, so  $t_{frr}$  is specified with a minimum value. Faster commutation speeds require an appropriate derating of  $I_{FM}$ , peak  $V_R$  or both. Ultimately,  $t_{frr}$  is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during  $t_{rr}$  as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$  is the peak drain-to-source voltage that the device must sustain during commutation;  $I_{FM}$  is the maximum forward source-drain diode current just prior to the onset of commutation.

$V_R$  is specified at 80% of  $V_{(BR)DSS}$  to ensure that the CSOA stress is maximized as  $I_S$  decays from  $I_{RM}$  to zero.

$R_{GS}$  should be minimized during commutation.  $T_J$  has only a second order effect on CSOA.

Stray inductances,  $L_i$  in Motorola's test circuit are assumed to be practical minimums.

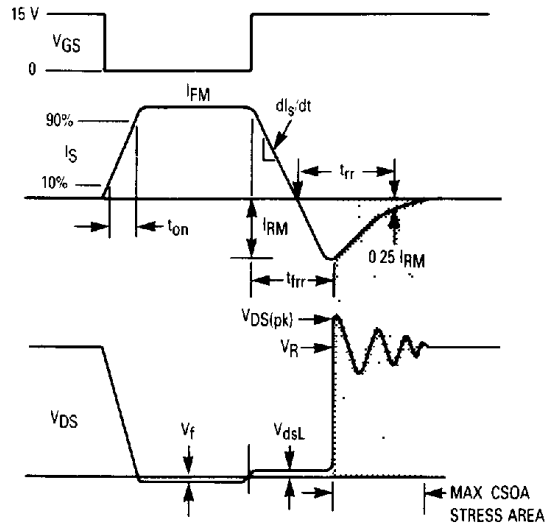


Figure 11. Commutating Waveforms

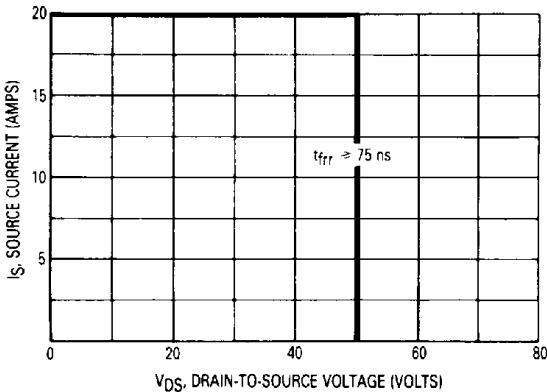


Figure 12. Commutating Safe Operating Area (CSOA)

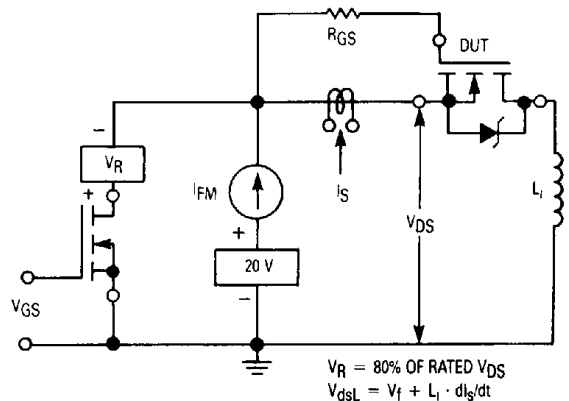


Figure 13. Commutating Safe Operating Area Test Circuit

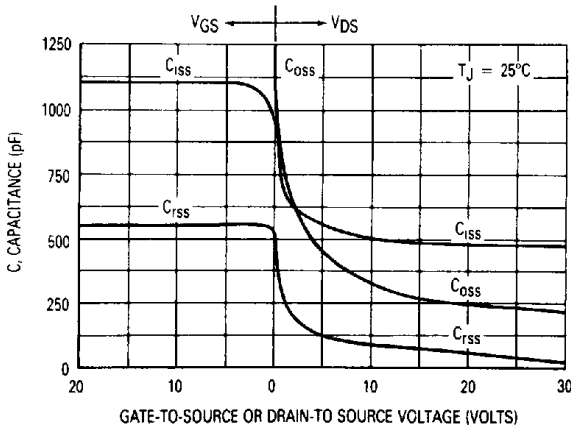


Figure 14. Capacitance Variation

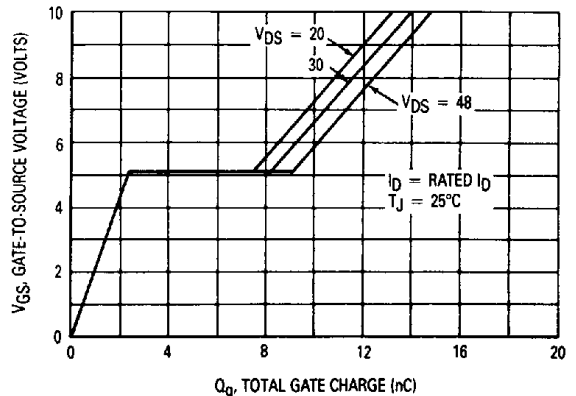
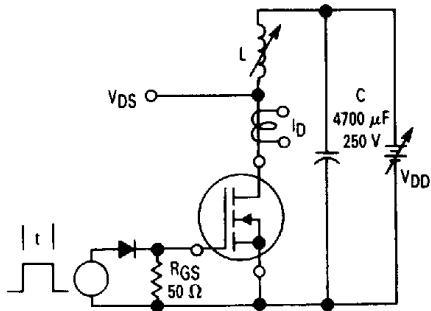
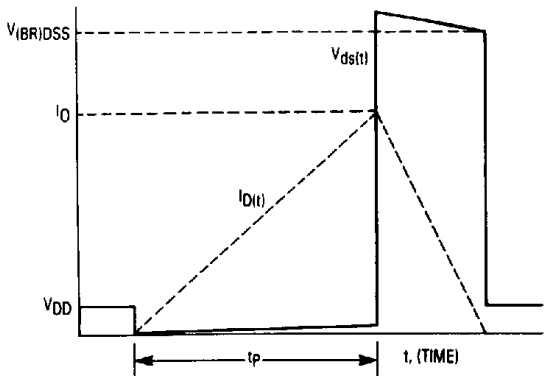


Figure 15. Gate-Charge versus Gate-to-Source Voltage



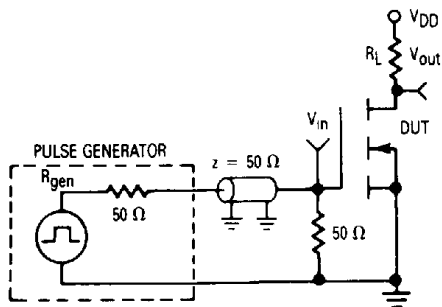
**Figure 16. Unclamped Inductive Switching Test Circuit**



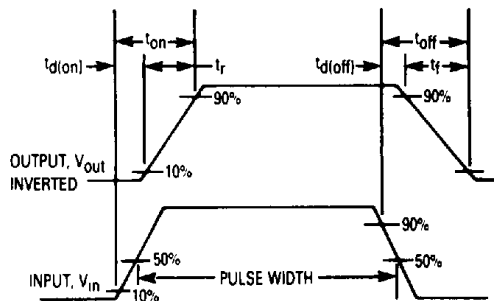
$$W_{DSR} = \left( \frac{1}{2} L I_0^2 \right) \left( \frac{V_{IBRIDSS}}{V_{IBRIDSS} - V_{DD}} \right)$$

**Figure 17. Unclamped Inductive Switching Waveforms**

## RESISTIVE SWITCHING



**Figure 18. Switching Test Circuit**



**Figure 19. Switching Waveforms**