AKD4562
Evaluation board Rev.A for AK4562

GENERAL DESCRIPTION

AKD4562 is an evaluation board for the portable digital audio 20bit A/D and D/A converter, AK4562. The AKD4562 can evaluate A/D converter D/A converter separately in addition to loopback mode (A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards directly. The AKD4562 has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards. Therefore, it's easy to evaluate the D/A section. The AKD4562 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4562 --- Evaluation board for AK4562
(Cable for connecting with printer port of IBM-AT,
compatible PC and control software are packed with this.)

FUNCTION

- **Compatible with 2 types of interface**
  - **Direct interface with AKM's A/D & D/A converter evaluation boards**
  - **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**
- **10pin Header for serial control mode**

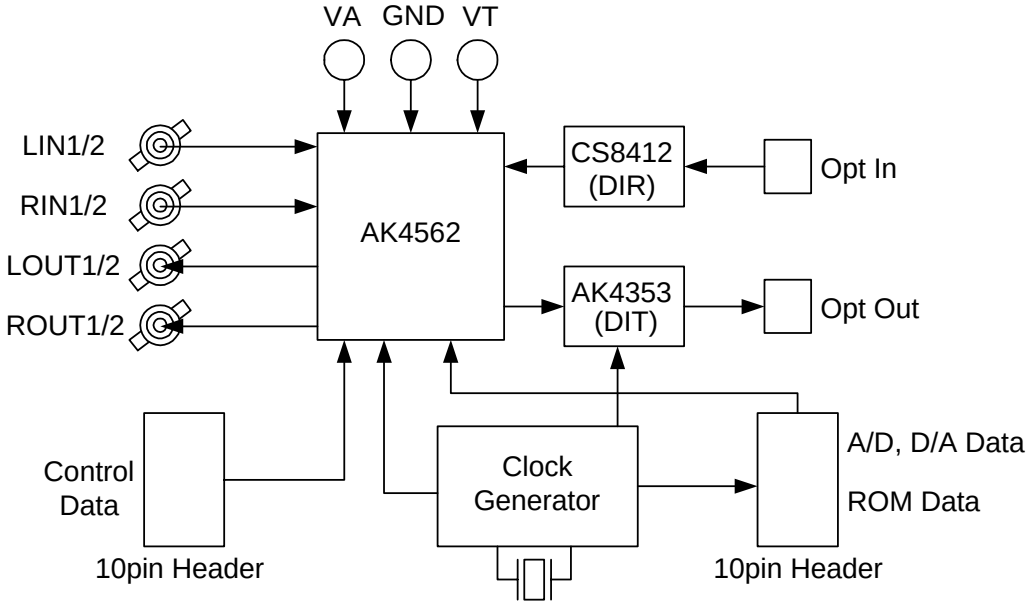


Figure 1. AKD4562 Block Diagram

* Circuit diagram and PCB layout are attached at the end of this manual.

1. Evaluation Board Manual

■ Input / Output circuits & Set-up jumper pin for Input / Output circuits

(1) LINE Block

(a) LIN1,2/RIN1,2 Input circuits

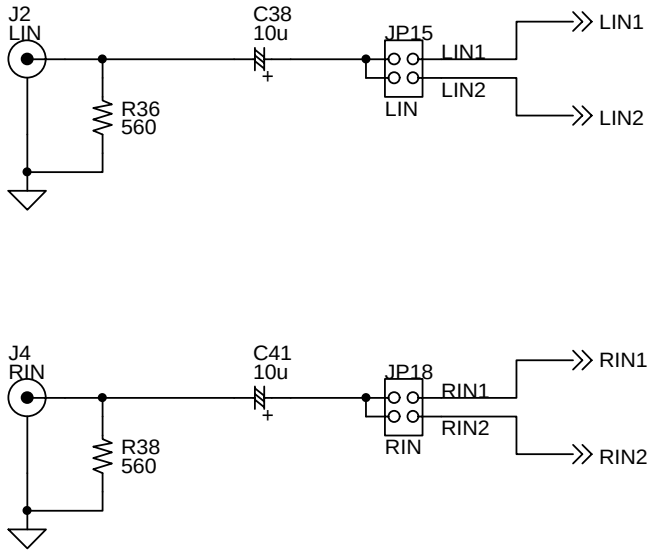
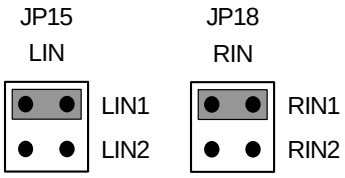
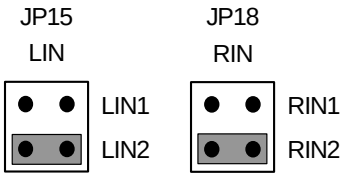


Figure 2. LIN1,2/RIN1,2 Input circuits

1. Analog signal is input to LIN1 and RIN1 pins via J2 and J4 connectors.



2. Analog signal is input to LIN2 and RIN2 pins via J2 and J4 connectors.



(b) LOUT1/ROUT1 and OPGAL/OPGAR Selection circuits

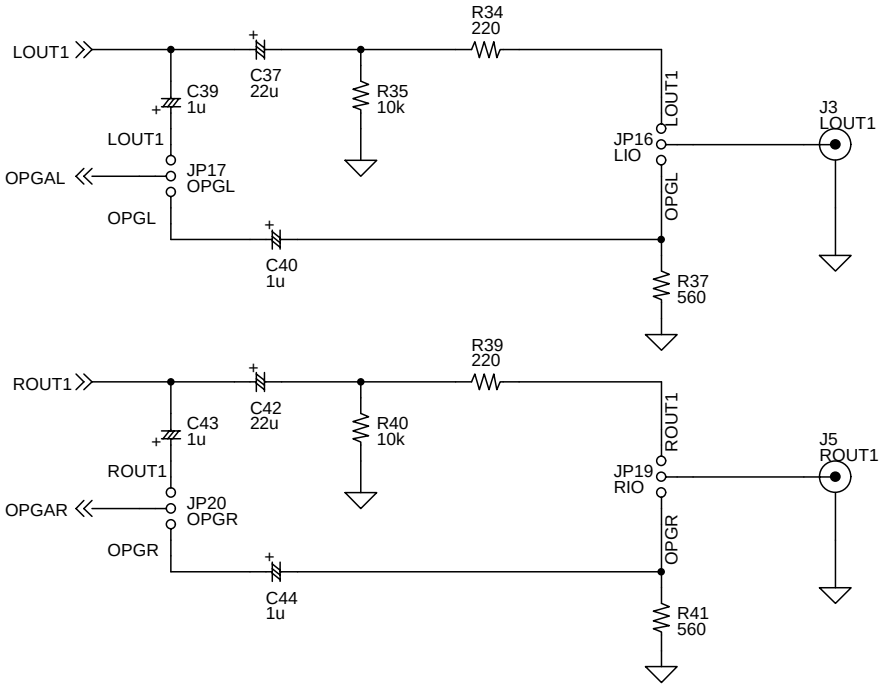
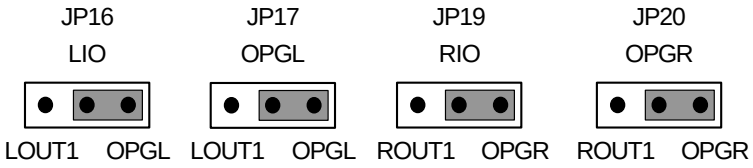
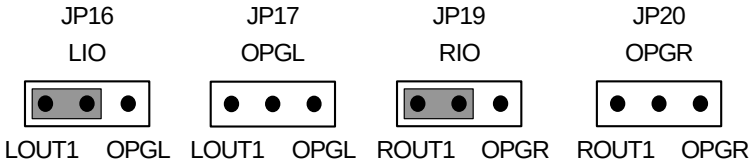


Figure 3. LOUT1/ROUT1 and OPGAL/OPGAR Selection circuits

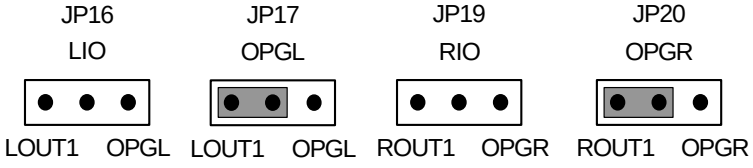
1. Analog signal is input to OPGAL and OPGAR pins via J3 and J5 connectors.



2. Analog signal is output to LOUT1 and ROUT1 pins via J3 and J5 connectors.



3. Analog signal is input to OPGAL and OPGAR pins via LOUT1 and ROUT1 pins.



(2) Other Jumper pins

1. JP1 (CSN) : Selection of CSN pin
   SSB : SSB mode.
   AKM : AKM mode.

2. JP2 (SSB) : Selection of SSB mode or AKM mode
   OPEN : AKM mode.
   SHORT : SSB mode.

3. JP3 (TST) : Selection of TEST pin
   OPEN : Normal mode.
   SHORT : Test mode.
   * Always open.

4. JP4 (GND) : Analog ground and Digital ground
   OPEN : Separated.
   SHORT : Common. (The connector "DGND" can be open.) <default>

5. JP5 (VT) : D2V and VT
   OPEN : Separated. <default>
   SHORT : Common. (The connector "VT" can be open.)

6. JP9 (SDTO) : SDTO of AK4562
   Always open. It can be short for only evaluation mode "7)".

7. JP10 (MODE) : Setting mode of CS8412
   OPEN : I^2S compatible mode.
   SHORT : 16 bit LSB justified.

* AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Operation sequence

1) Set up the power supply lines.

[VA]	(orange)	= 2.2 ~ 3.0V	: for VA of AK4562 (typ. 2.5V)
[VT]	(orange)	= 1.8 ~ 3.0V	: for VT of AK4562 (typ. 2.5V)
[D2V]	(orange)	= 1.8 ~ 3.0V	: for 74LVC541 (typ. 2.5V)
[D5V]	(red)	= 3.6 ~ 5.0V	: for logic (typ. 5.0V)
[AGND]	(black)	= 0V	: for analog ground
[DGND]	(black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.
VT and D2V must be same voltage level.

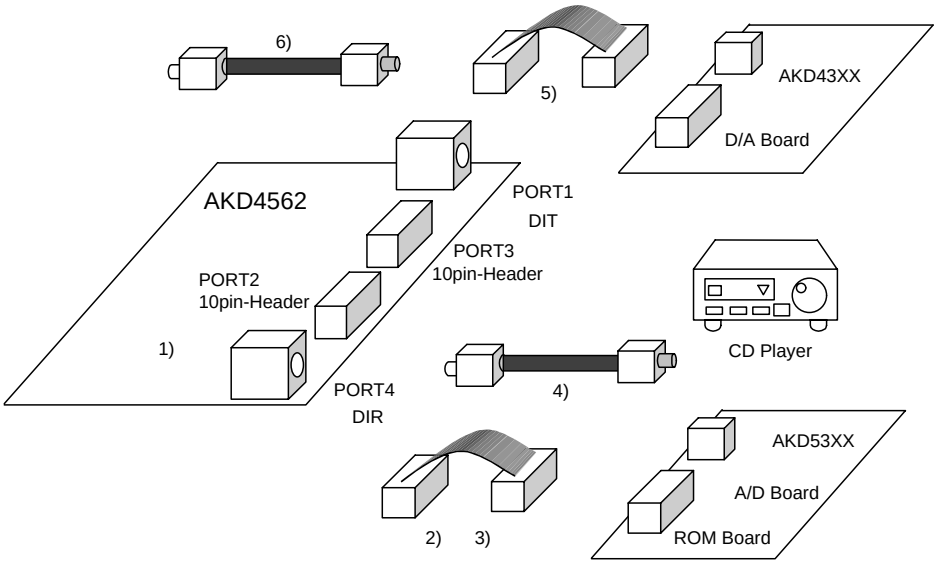
2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)
   Note : This evaluation board corresponds to I^2S compatible mode for evaluation of A/D.

3) Power on.
   The AK4562 and AK4353 should be reset once bringing SW1, 2 "L" upon power-up.

■ Evaluation mode

Applicable Evaluation Mode

1) Evaluation of loopback mode (default)
2) Evaluation of D/A using ideal sine wave generated by ROM data
3) Evaluation of D/A using A/D converted data
4) Evaluation of D/A using DIR (Optical Link)
5) Evaluation of A/D using D/A converted data
6) Evaluation of A/D using DIT (Optical Link)
7) All interface signals including master clock are fed externally.

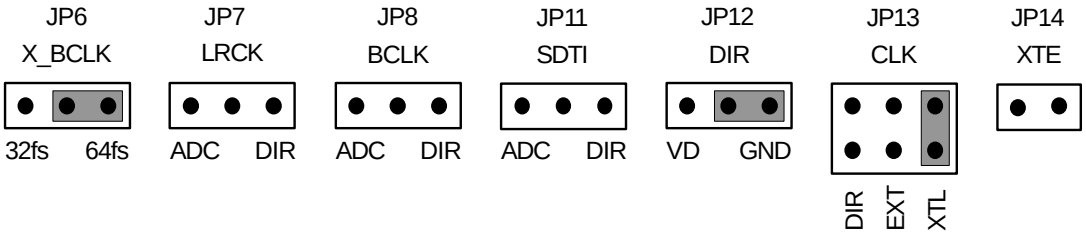


1) Evaluation of loopback mode. <default>

Nothing should be connected to PORT3 and PORT4. In case of using external clock through a BNC connector (J1), select EXT on JP13 (CLK) and short JP14 (XTE). This mode corresponds to only I^2S compatible mode.

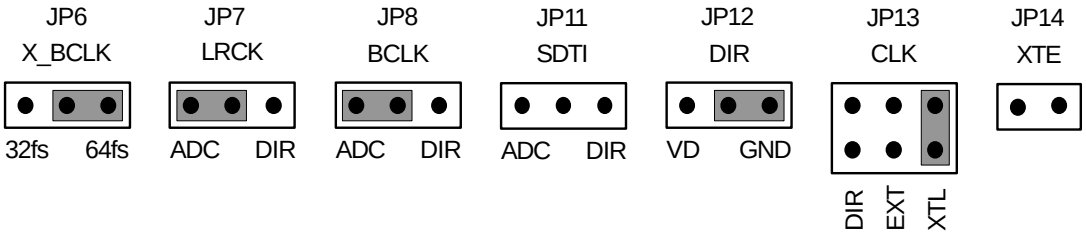
2) Evaluation of D/A using A/D converted data from ideal sine wave generated by ROM data.

Digital signals generated by AKD43XX are used. PORT3 is used for the interface with AKD43XX. Master clock is sent from AKD4562 to AKD43XX and BCLK, LRCK, SDTI are sent from AKD43XX to AKD4562. Nothing should be connected to PORT4. In case of using external clock through a BNC connector (J1), select EXT on JP13 (CLK) and short JP14 (XTE).



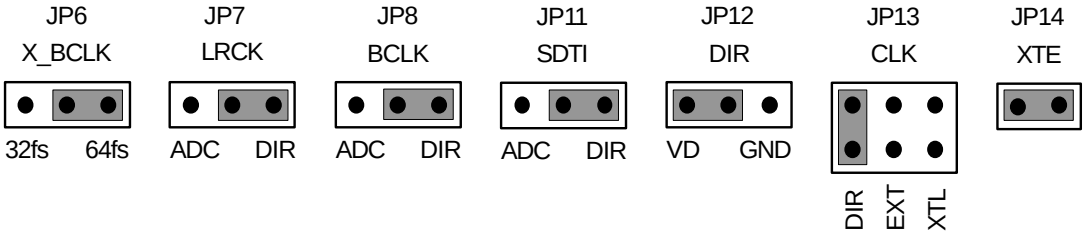
3) Evaluation of D/A using A/D converted data.

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards with PORT3. Nothing should be connected to PORT4. In case of using external clock through a BNC connector (J1), select EXT on JP13 (CLK) and short JP14 (XTE).



4) Evaluation of D/A using DIR. (Optical link)

PORT4 (DIR) is used. DIR generates MCLK, BCLK, LRCK and SDATA from the received data through optical connector (TORX176). Used for the evaluation using CD test disk. Nothing should be connected to PORT3. DIR (CS8412) corresponds to only I^2S compatible mode or 16 bit LSB justified.

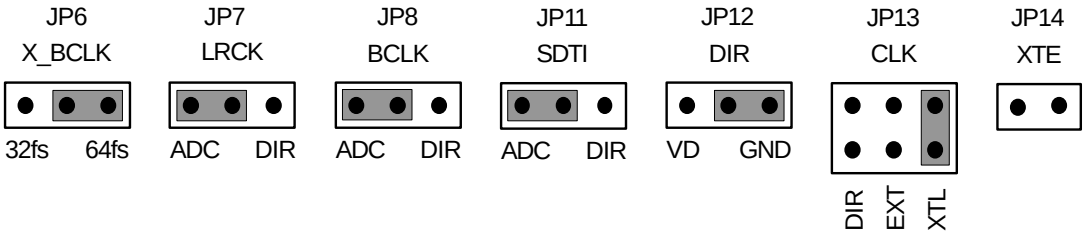


5) Evaluation of A/D using D/A converted data.

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards with PORT3. Nothing should be connected to PORT4.

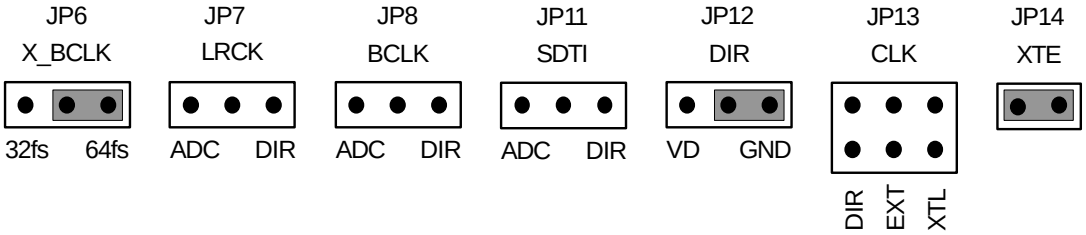
6) Evaluation of A/D using DIT. (Optical link)

PORT1 (DIT) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input. Nothing should be connected PORT3 and PORT4. In case of using external clock through a BNC connector (J1), select EXT on JP13 (CLK) and short JP14 (XTE). DIT (AK4353) corresponds to only I^2S compatible mode.



7) All interfacing signals (MCLK, BCLK, LRCK) are fed from the external circuit through PORT3.

PORT3 is used. JP7, 8, 11 and 13 should be open.



■ The function of the toggle SW

Upper-side is "H" and lower-side is "L".

[SW1] (PDN): Power down of AK4562. Keep "H" during normal operation.

[SW2] (DIT): Power down of AK4353. Keep "H" during normal operation.

■ Indication for LED

[LED1] (VERF): Monitor VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.

[LED2] (PREM): Indicate whether the input data of CS8412 is pre-emphasized or not.

■ Serial Control

The AK4562 can be controlled via the printer port (parallel port) of IBM-AT compatible PC. Connect PORT2 (CTRL) with PC by 10 wire flat cable packed with the AKD4562.

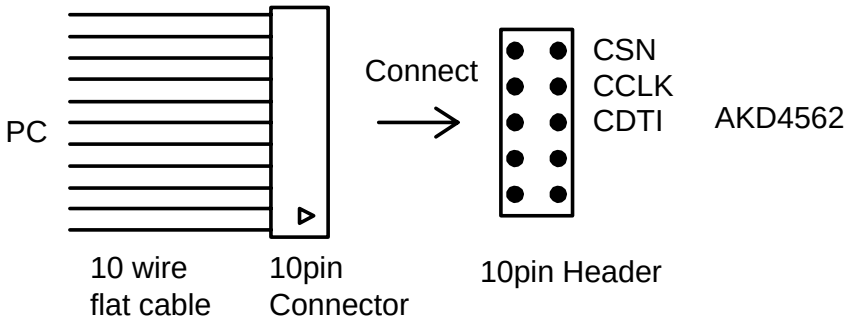


Figure 4. Connect of 10 wire flat cable

2. Control Software Manual

■ Set-up of evaluation board and control software

1. Set up the AKD4562 according to previous term.

2. Connect IBM-AT compatible PC with AKD4562 by 10-line type flat cable (packed with AKD4562). Take care of the direction of 10pin header. (This control software does not operate on Windows NT, therefore please operate it on Windows95/98.)

3. Insert the floppy-disk labeled “AKD4562 Control Program ver 1.0” into the floppy-disk drive.

4. Access the floppy-disk drive and double-click the icon of “AKD4562.exe” to set up the control program. This software corresponds to only AKM mode.

5. Then please evaluate according to the follows.

■ Explanation of each buttons

1. [Port Setup] : Set up the printer port.
2. [Reset] : Initialize the register of AK4562.
3. [Function1] : Dialog to write data by keyboard operation.
4. [Function2] : Dialog to evaluate IPGA and OPGA.
5. [Write] : Dialog to write data by mouse operation.

Note : AK4353(DIT) is fixed to MCLK=256fs and I^2S compatible mode. Therefore, in the case of evaluation for AK4562’s ADC, it is necessary for AK4562 to set up MCLK=256fs and I^2S compatible mode.

■ Explanation of each dialog

1. [Function1 Dialog] : Dialog to write data by keyboard operation

Address Box: Input register address in 2 figures of hexadecimal.
Data Box: Input register data in 2 figures of hexadecimal.

If you want to write the input data to AK4562, click “OK” button. If not, click “Cancel” button.

2. [Function2 Dialog] : Dialog to evaluate IPGA and OPGA

This dialog corresponds to only addr=03H and 04H.

Address Box: Input register address in 2 figures of hexadecimal.
Start Data Box: Input start data in 2 figures of hexadecimal.
End Data Box: Input end data in 2 figures of hexadecimal.
Interval Box: Data is written to AK4562 by this interval.
Step Box: Data changes by this step.
Mode Select Box:

If you check this check box, data reaches end data, and returns to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09 09 08 07 06 05 04 03 02 01 00

If you do not check this check box, data reaches end data, but does not return to start data.
[Example] Start Data = 00, End Data = 09
Data flow: 00 01 02 03 04 05 06 07 08 09

If you want to write the input data to AK4562, click “OK” button. If not, click “Cancel” button.

3. [Write Dialog] : Dialog to write data by mouse operation

There are dialogs corresponding to each register.

Click the “Write” button corresponding to each register to set up the dialog. If you check the check box, data becomes “H” or “1”. If not, “L” or “0”.

If you want to write the input data to AK4562, click “OK” button. If not, click “Cancel” button.

■ Operation flow

Keep the following flow surely.

1. Set up the control program according to explanation above.
2. Click “Port Setup” button.
3. Click “Write default” button.
4. Then set up the dialog and input data.

■ Indication of data

Input data is indicated on the register map. Red letter indicates “H” or “1” and blue one indicates “L” or “0”. Blank is the part that is not defined in the datasheet.

■ Attention on the operation

If you set up Function1 or Function2 dialog, input data to all boxes. Attention dialog is indicated if you input data or address that is not specified in the datasheet or you click “OK” button before you input data. In that case set up the dialog and input data once more again. These operations does not need if you click “Cancel” button or check the check box.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit: Audio Precision, System Two
- MCLK : 256fs
- BCLK : 64fs
- fs : 44.1kHz
- Bit : 20bit
- Power Supply : VA=VD=VT=2.5V
- Interface : DIR/DIT
- Temperature : Room

[Measurement Results]

Parameter		Input pin	Results (Lch / Rch)	Unit
ADC Analog Input Characteristics				
S/(N+D)	(-0.5dB Input)	LIN1 / RIN1	85.3 / 84.8	dB
		LIN2 / RIN2	85.4 / 84.7	dB
D-Range	(A-weighted)	LIN1 / RIN1	88.6 / 88.6	dB
		LIN2 / RIN2	88.6 / 88.6	dB
S/N	(A-weighted)	LIN1 / RIN1	88.6 / 88.6	dB
		LIN2 / RIN2	88.6 / 88.6	dB
Interchannel Isolation		LIN1 / RIN1	109.6 / 108.7	dB
		LIN2 / RIN2	109.7 / 109.8	dB
DAC Analog Output Characteristics				
S/(N+D)		-	89.5 / 89.5	dB
D-Range	(A-weighted)	-	93.0 / 93.0	dB
S/N	(A-weighted)	-	93.2 / 93.2	dB
Interchannel Isolation		-	109.5 / 108.7	dB
Output PGA Characteristics (OPGA)				
S/(N+D)		OPGAL / OPGAR	91.7 / 91.7	dB
S/N	(A-weighted)	OPGAL / OPGAR	94.2 / 94.2	dB
Noise level at Mute	(A-weighted)	OPGAL / OPGAR	108.5 / 108.6	dB

[ADC Plot]

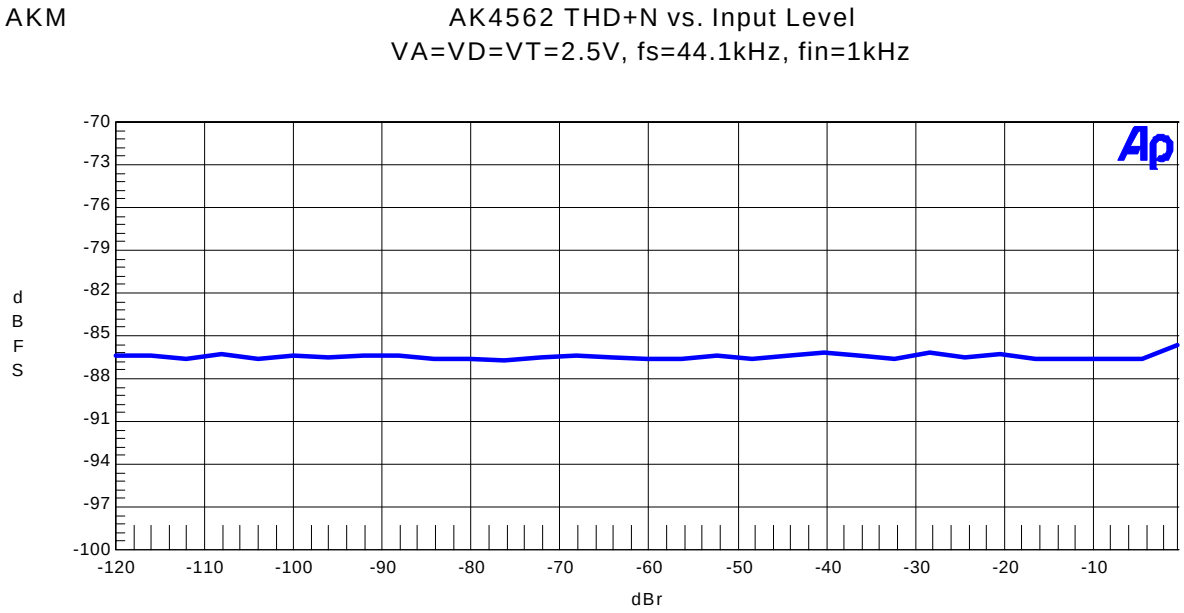


Figure 1. THD+N vs. Input Level

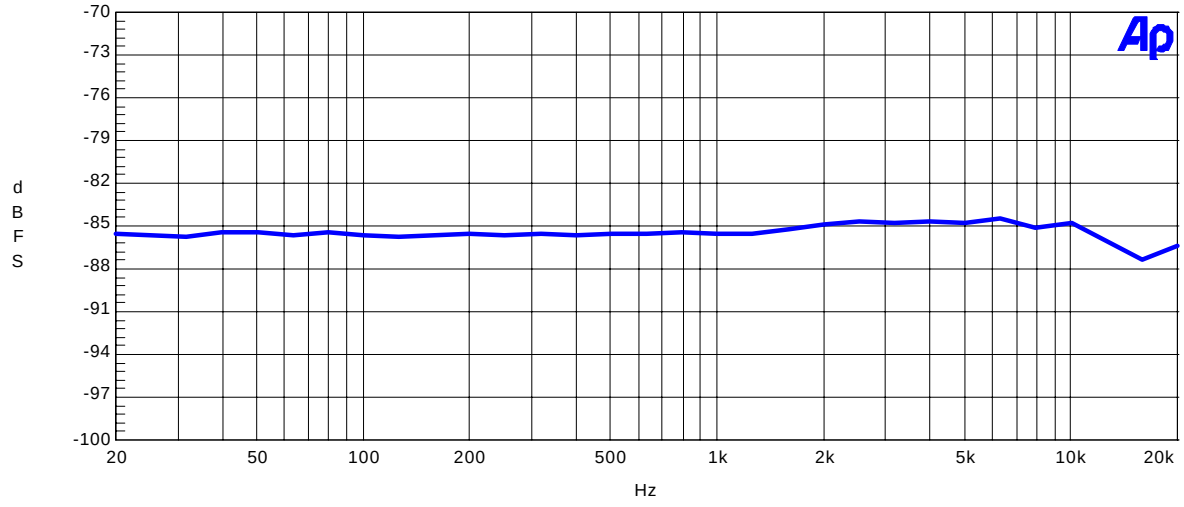


Figure 2. THD+N vs. Input Frequency

AKM

AK4562 Linearity
VA=VD=VT=2.5V, fs=44.1kHz, fin=1kHz

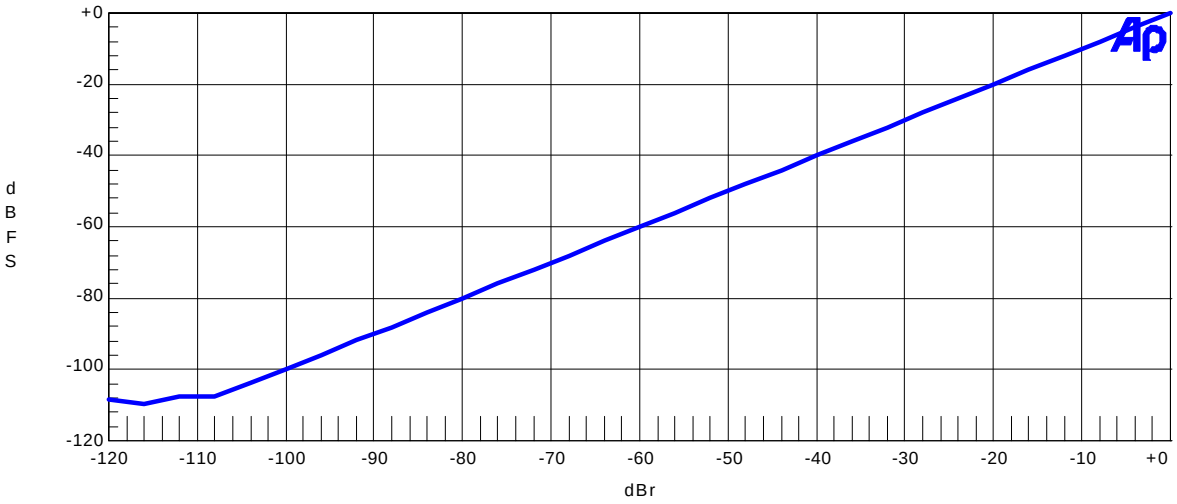


Figure 3. Linearity

AKM

AK4562 Frequency Response
VA=VD=VT=2.5V, fs=44.1kHz, Input=-0.5dBr

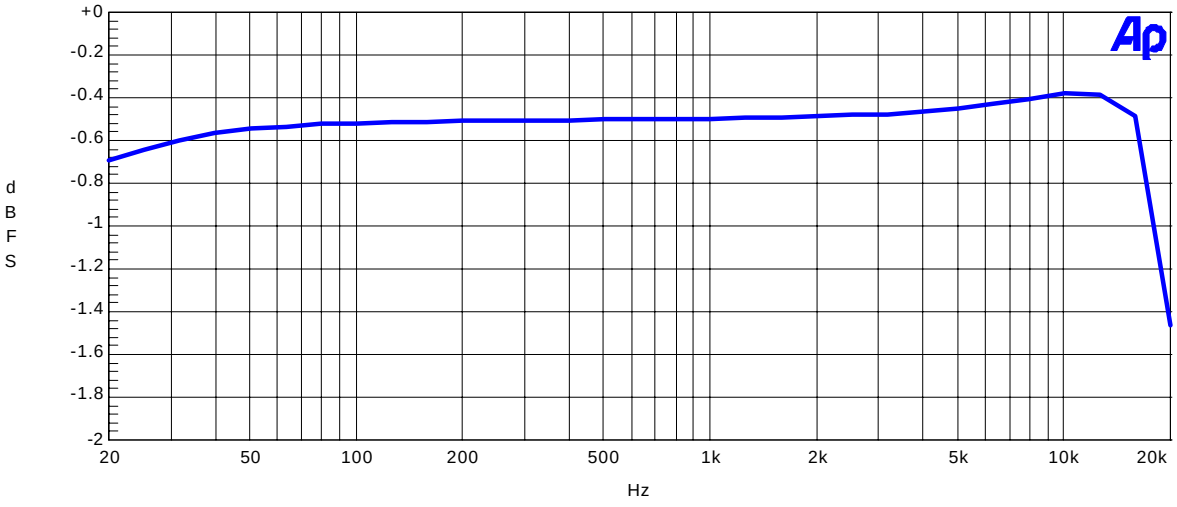


Figure 4. Frequency Response

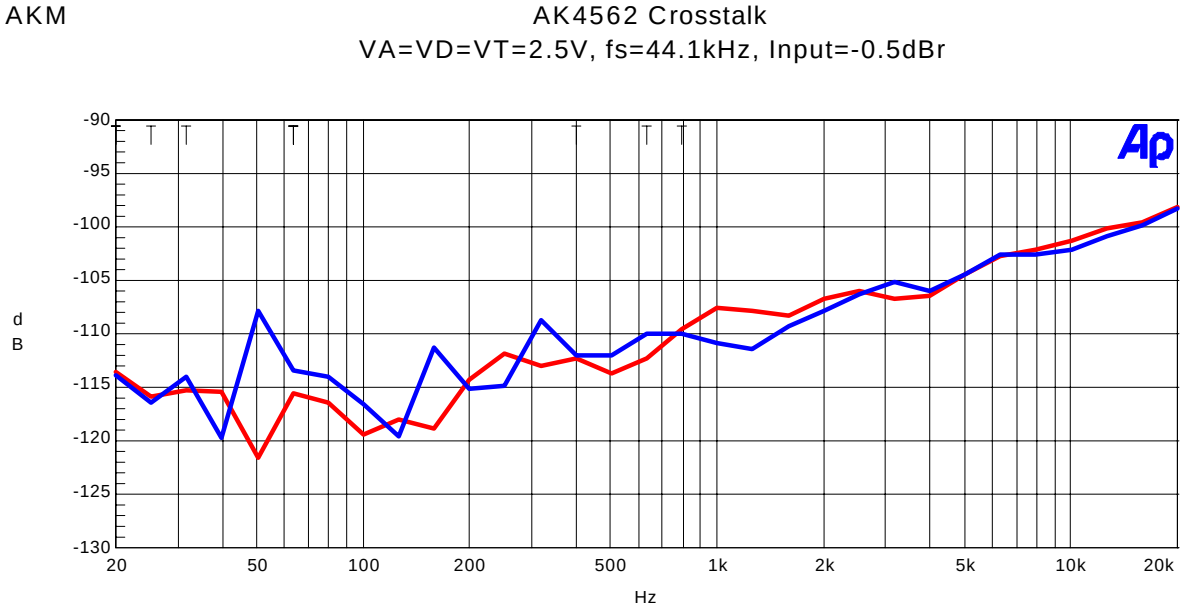


Figure 5. Crosstalk

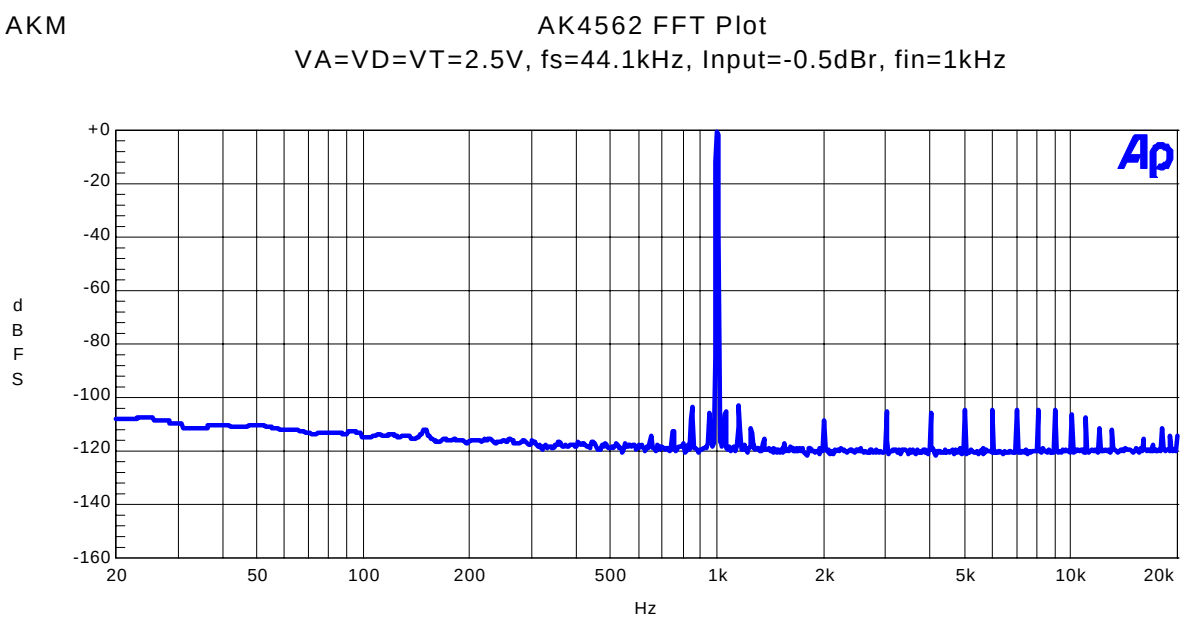


Figure 6. FFT Plot

AKM

AK4562 FFT Plot
VA=VD=VT=2.5V, fs=44.1kHz, Input=-60dBr, fin=1kHz

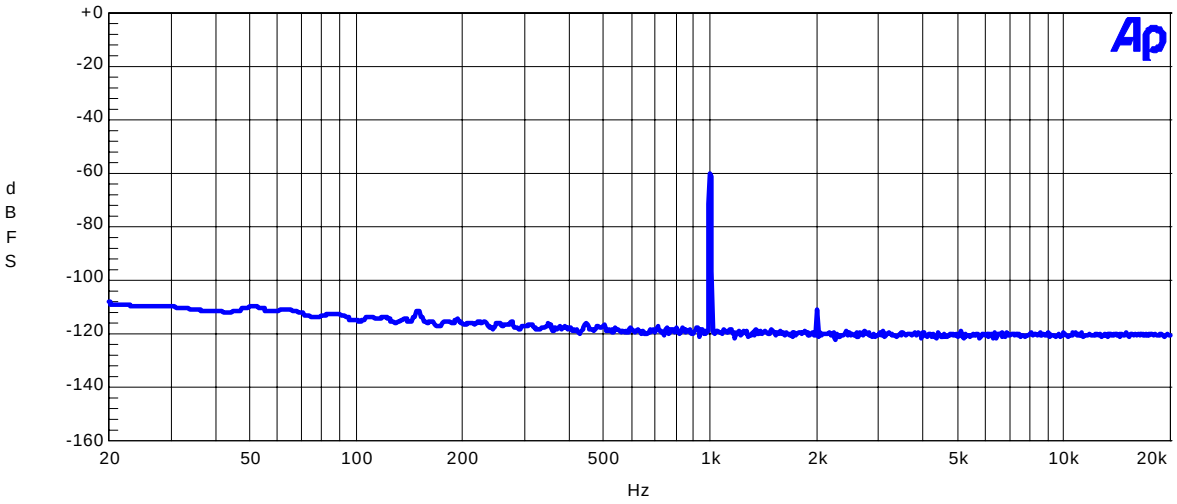


Figure 7. FFT Plot

AKM

AK4562 FFT Plot
VA=VD=VT=2.5V, fs=44.1kHz, fin=None

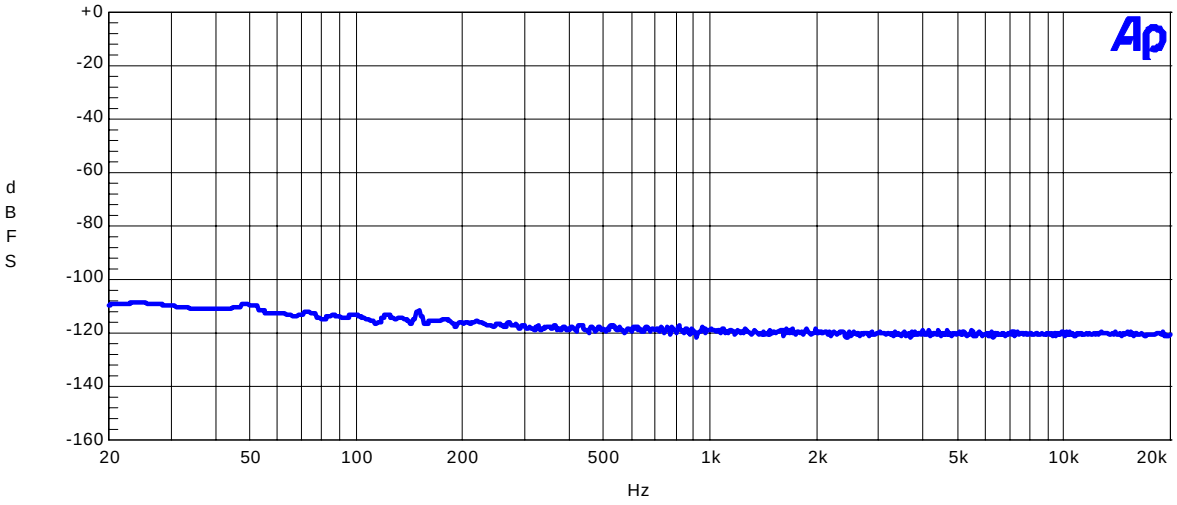


Figure 8. FFT Plot

[DAC Plot]

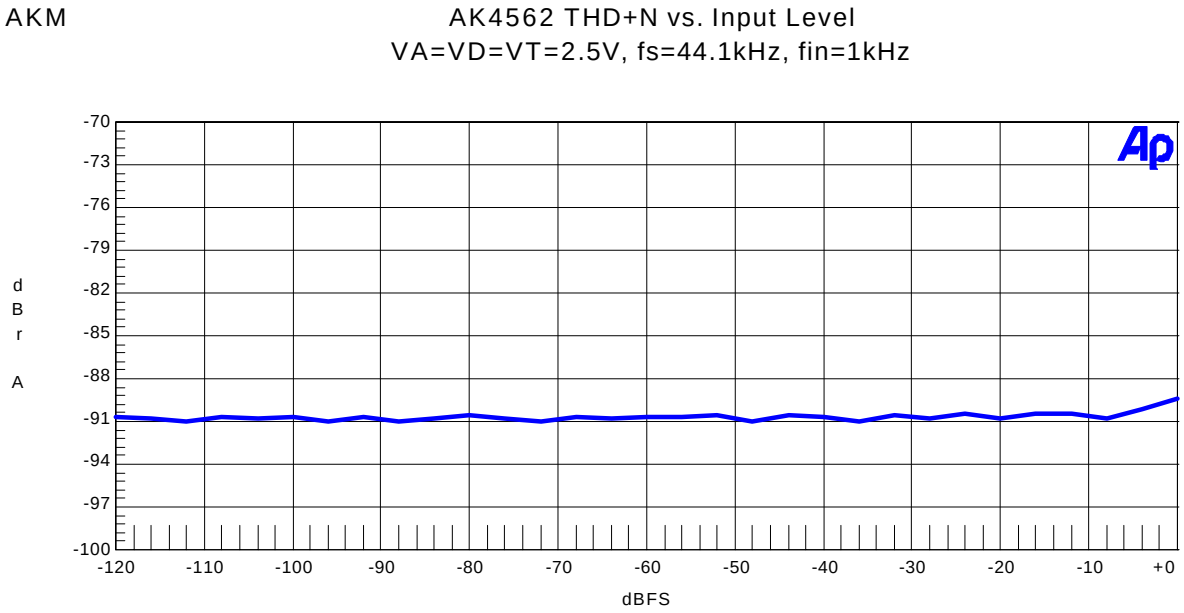


Figure 1. THD+N vs. Input Level

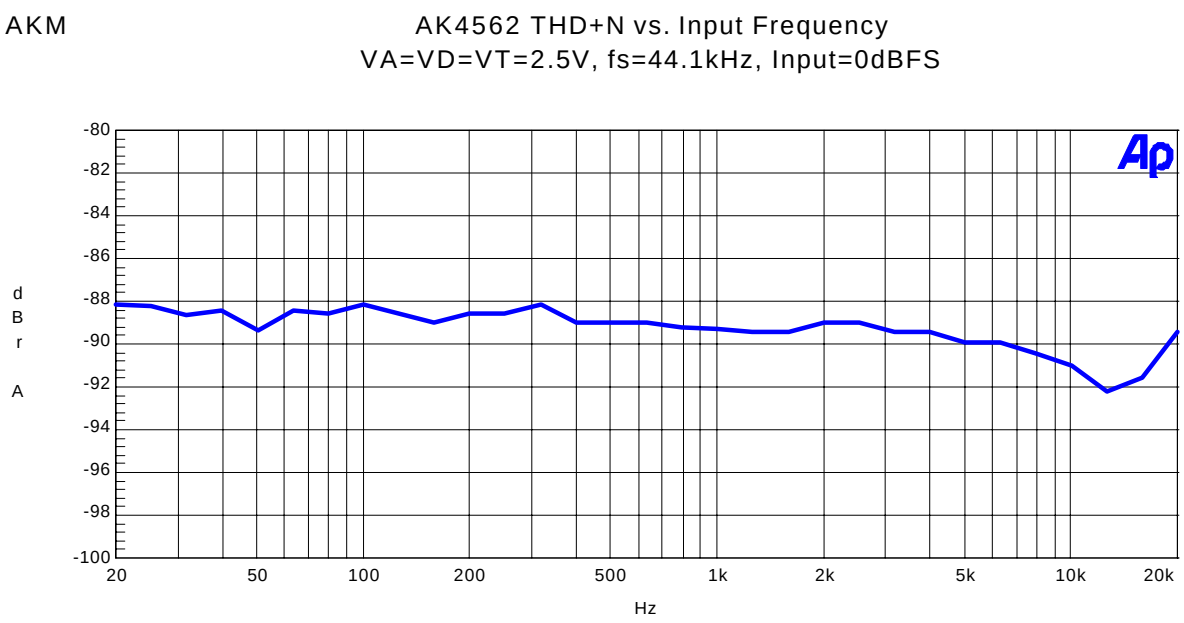


Figure 2. THD+N vs. Input Frequency

AKM

AK4562 Linearity
VA=VD=VT=2.5V, fs=44.1kHz, fin=1kHz

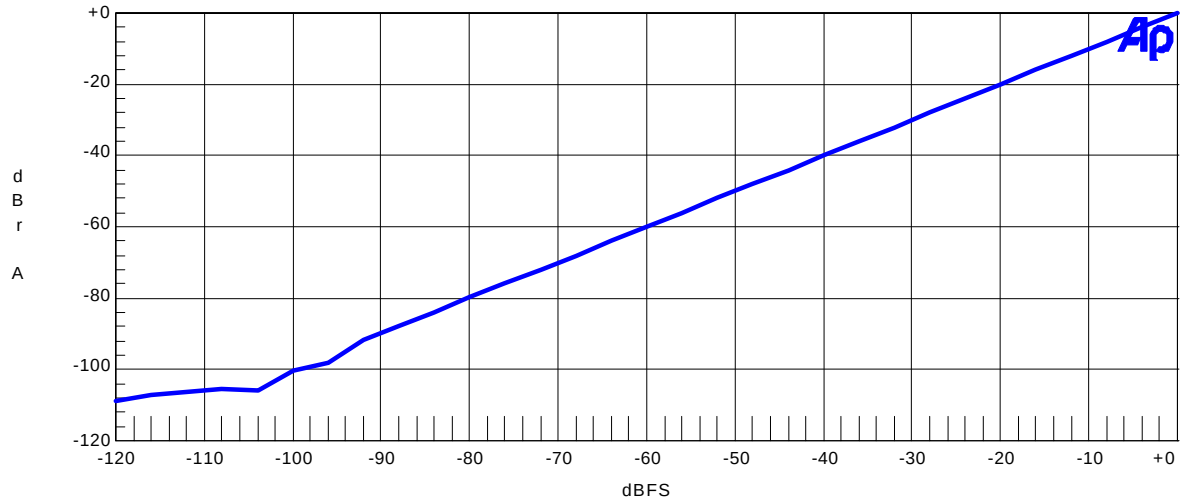


Figure 3. Linearity

AKM

AK4562 Frequency Response
VA=VD=VT=2.5V, fs=44.1kHz, Input=0dBFS

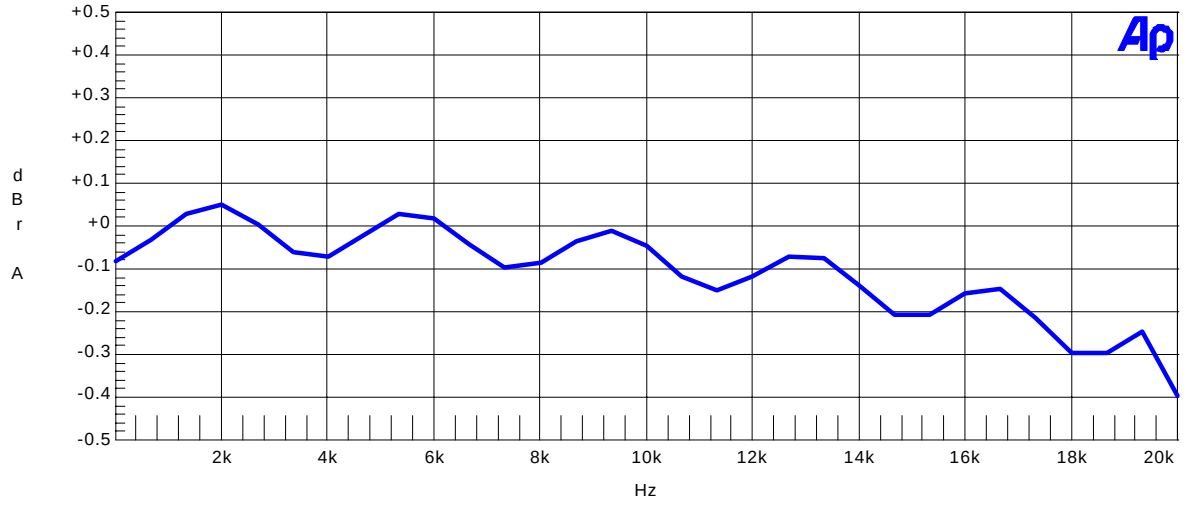


Figure 4. Frequency Response

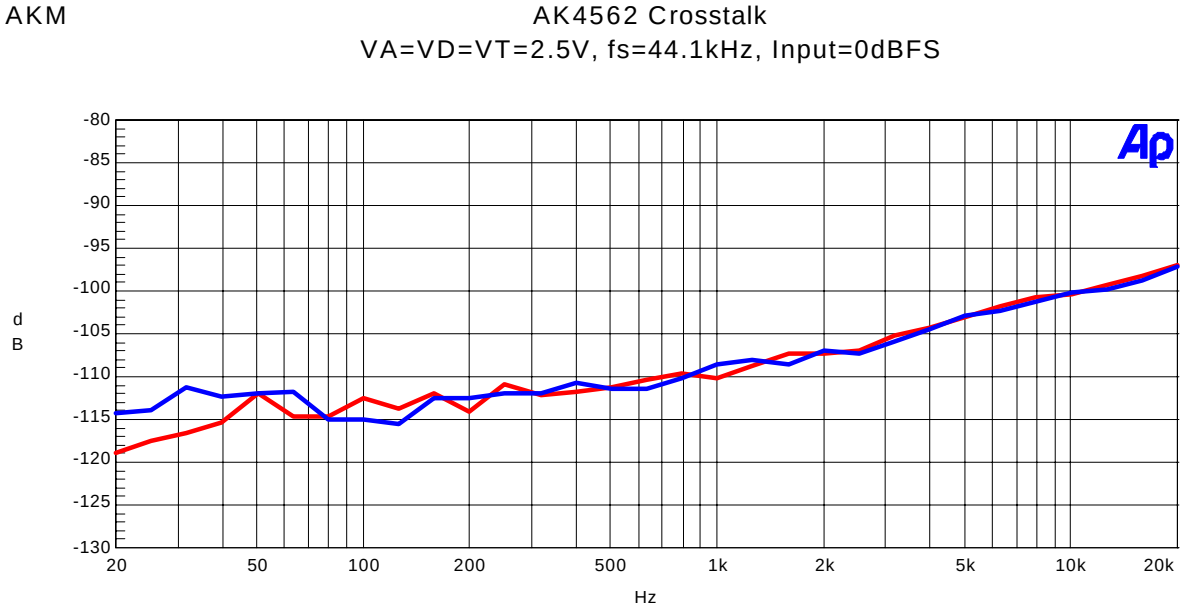


Figure 5. Crosstalk

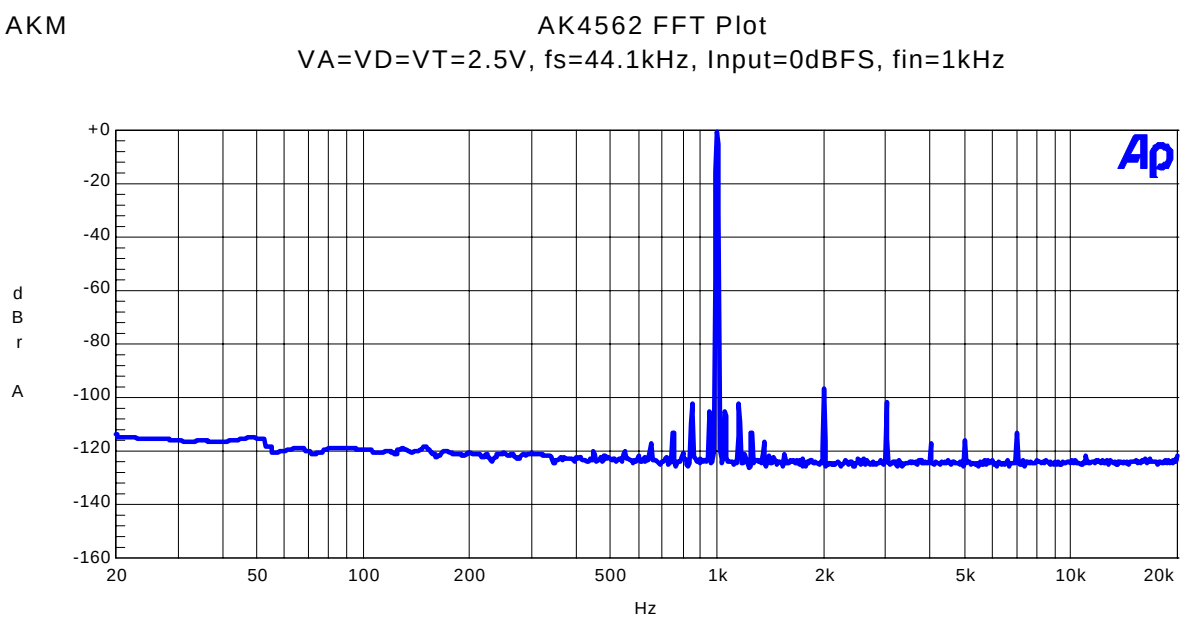


Figure 6. FFT Plot

AKM

AK4562 FFT Plot
VA=VD=VT=2.5V, fs=44.1kHz, Input=-60dBFS, fin=1kHz

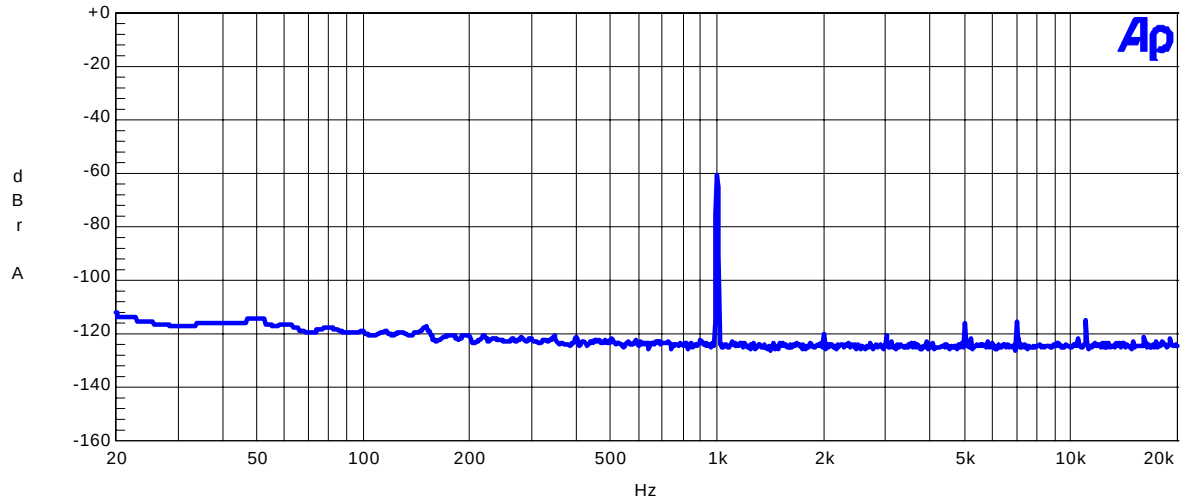


Figure 7. FFT Plot

AKM

AK4562 FFT Plot
VA=VD=VT=2.5V, fs=44.1kHz, fin=None

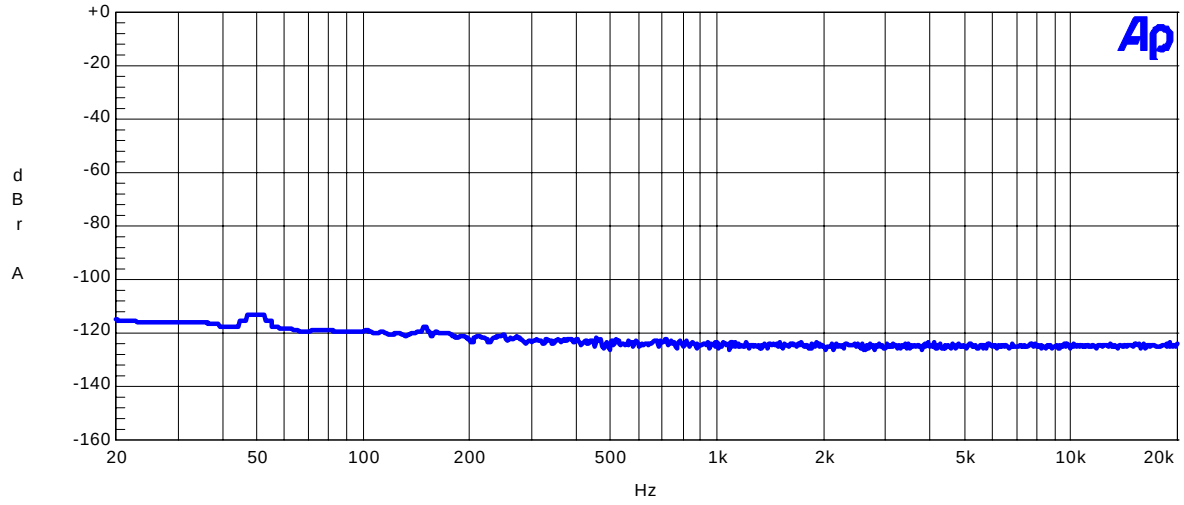
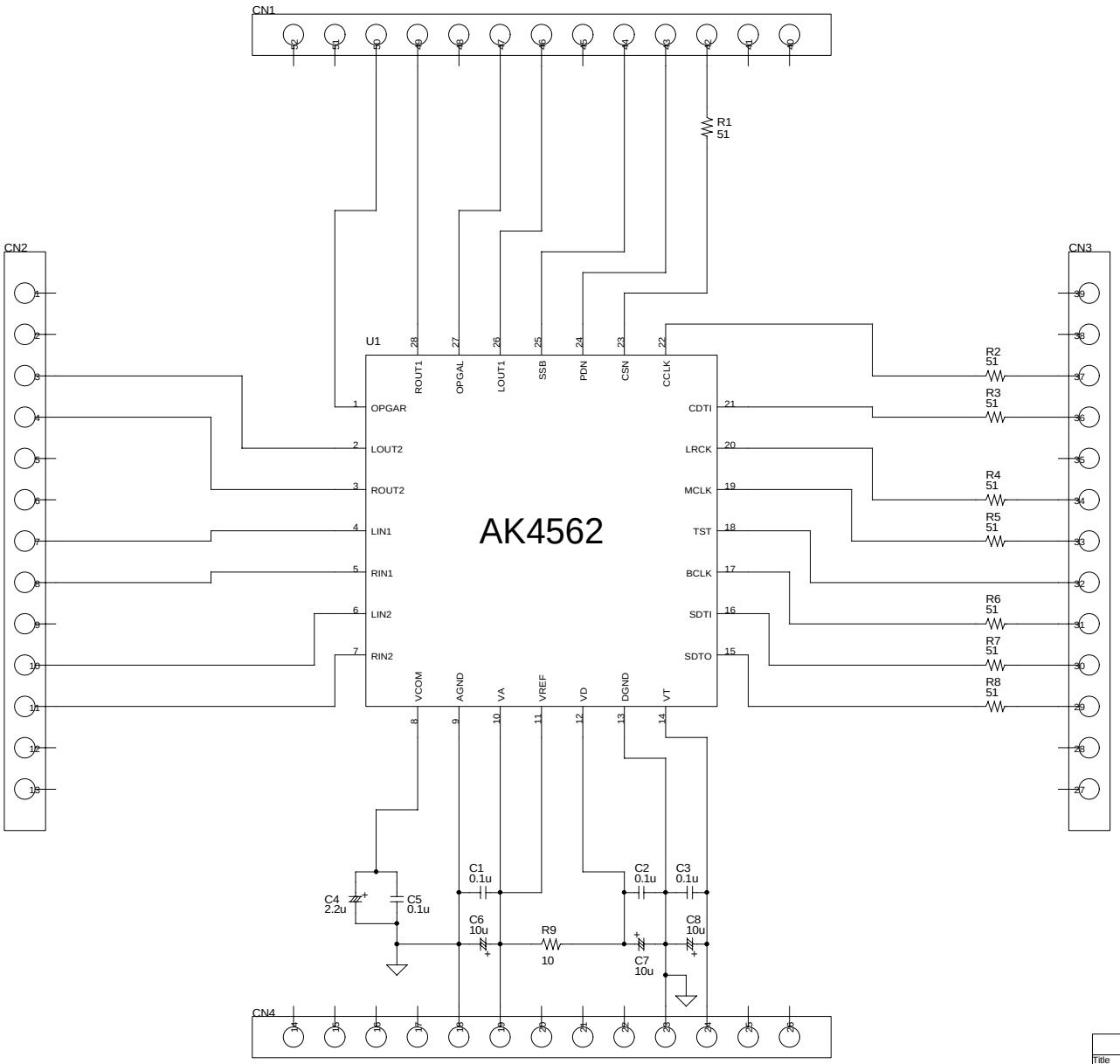


Figure 8. FFT Plot



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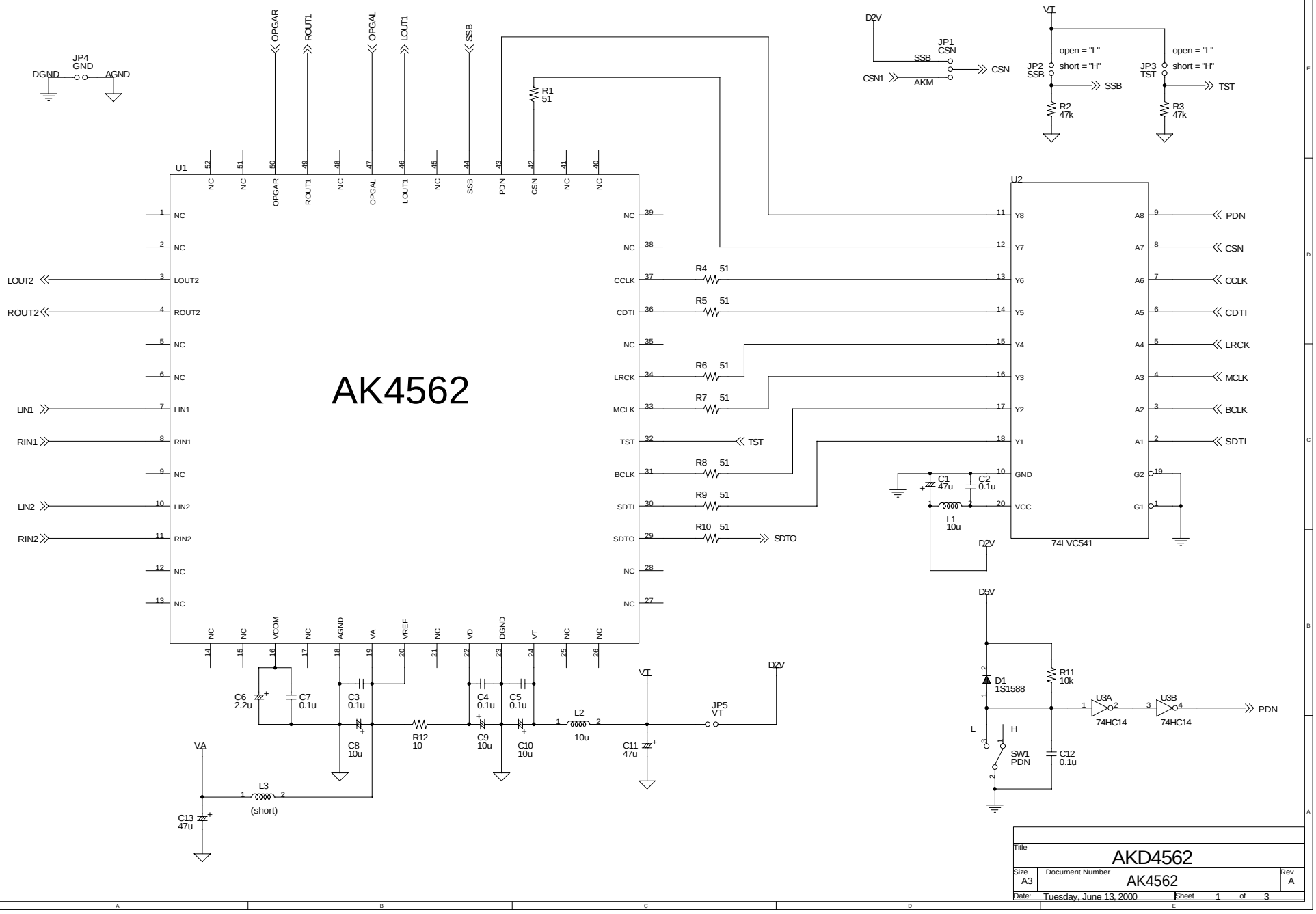
Date: Wednesday, February 02, 2000	Sheet 1 of 1	



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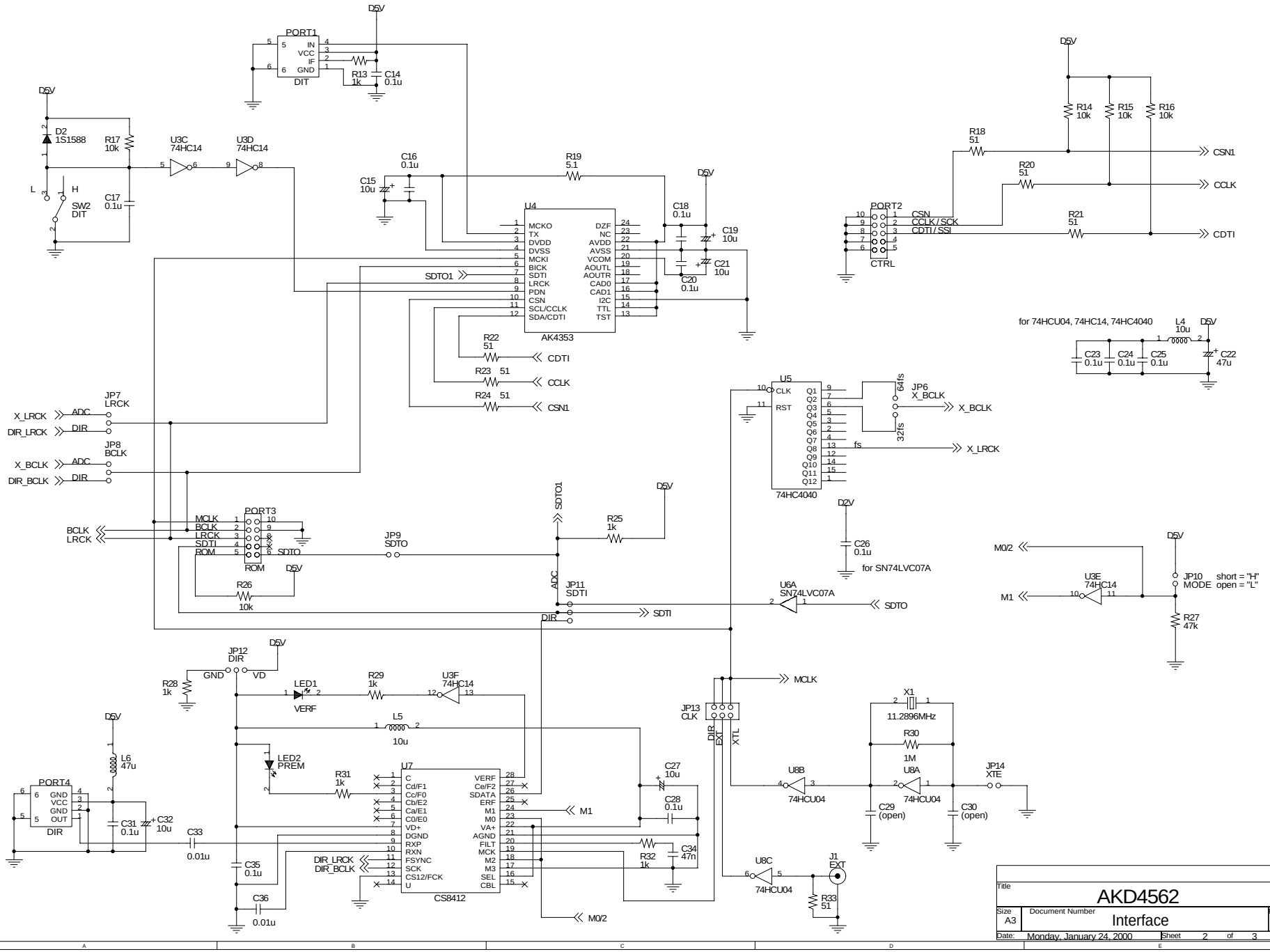
Size A3	Document Number AK4562	Rev A
Date: Tuesday, June 13, 2000	Sheet 1 of 3	



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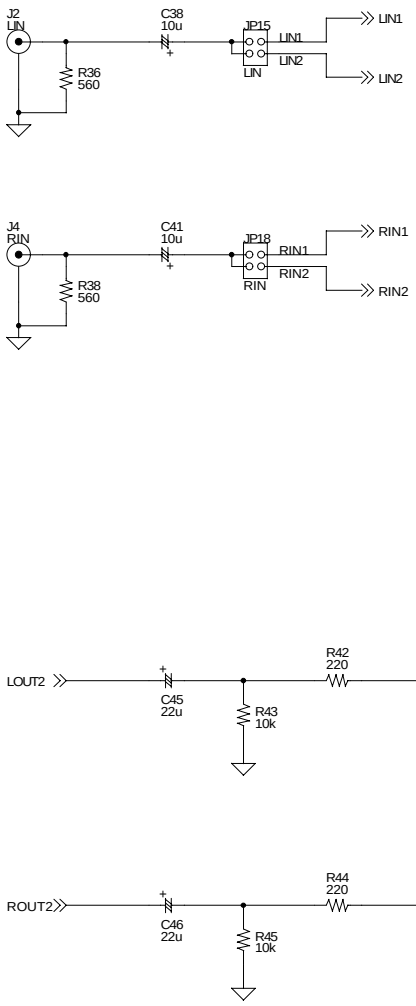

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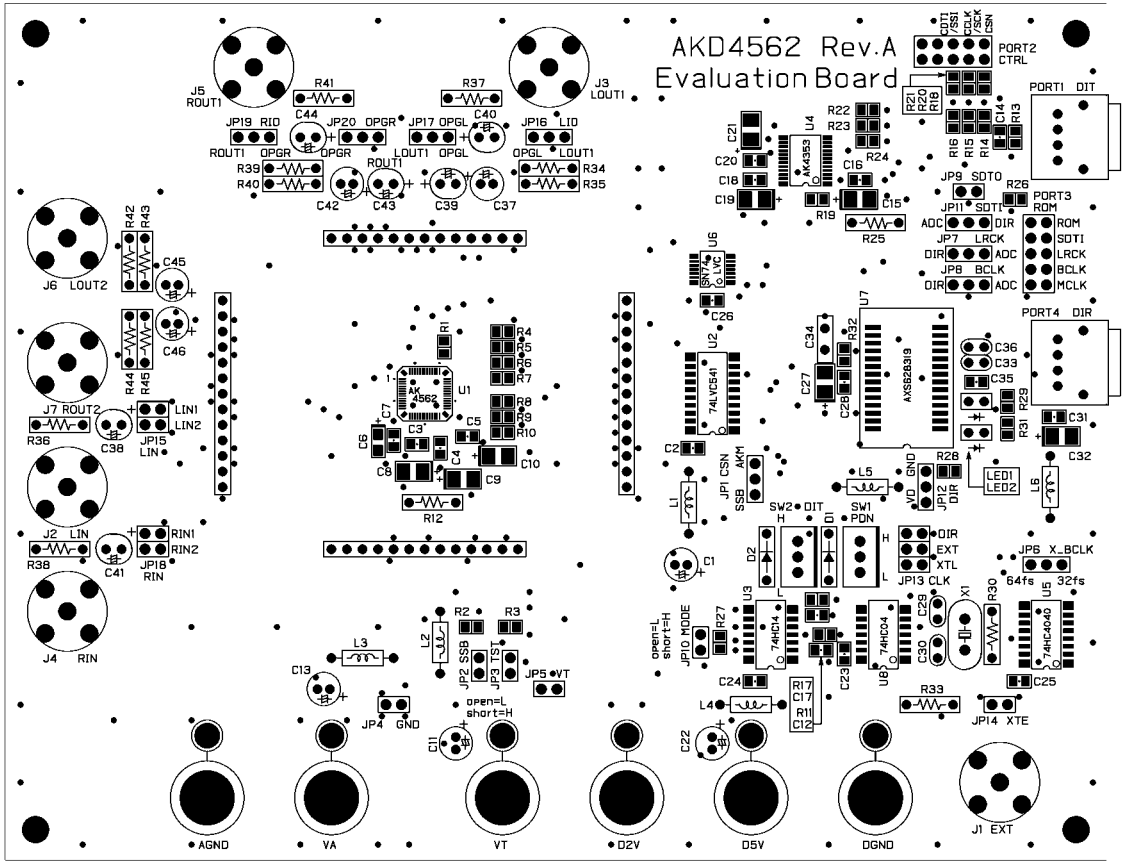
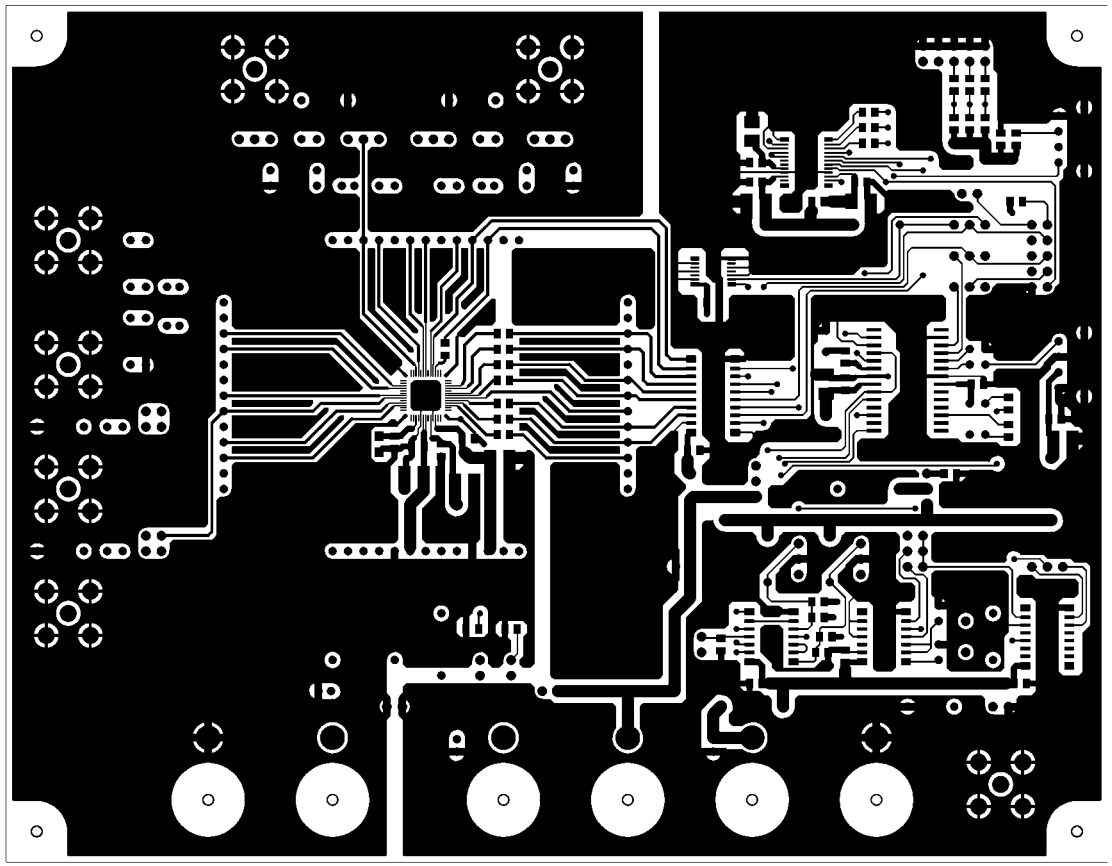
Date: Tuesday, December 21, 1999	Sheet 3 of 3	

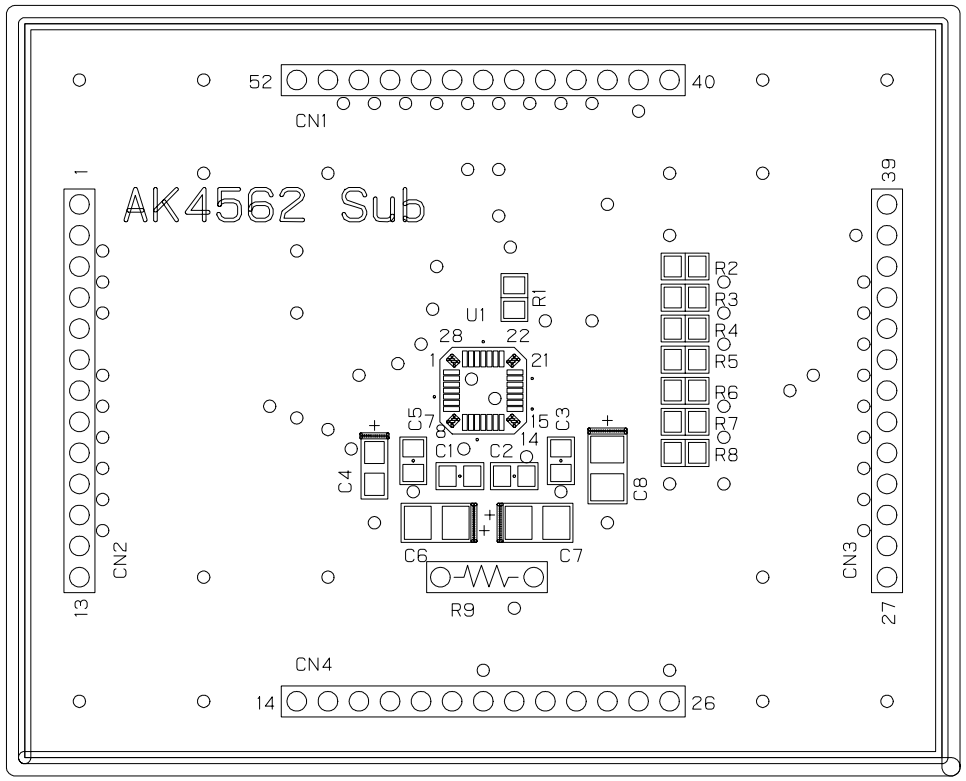


L1 部品面　　レジスト シルク AKD4562 Rev.A



L1 部品面 パターン　　AKD4562 Rev.A

AKD4582 Rev.A　　ボトム面パターン



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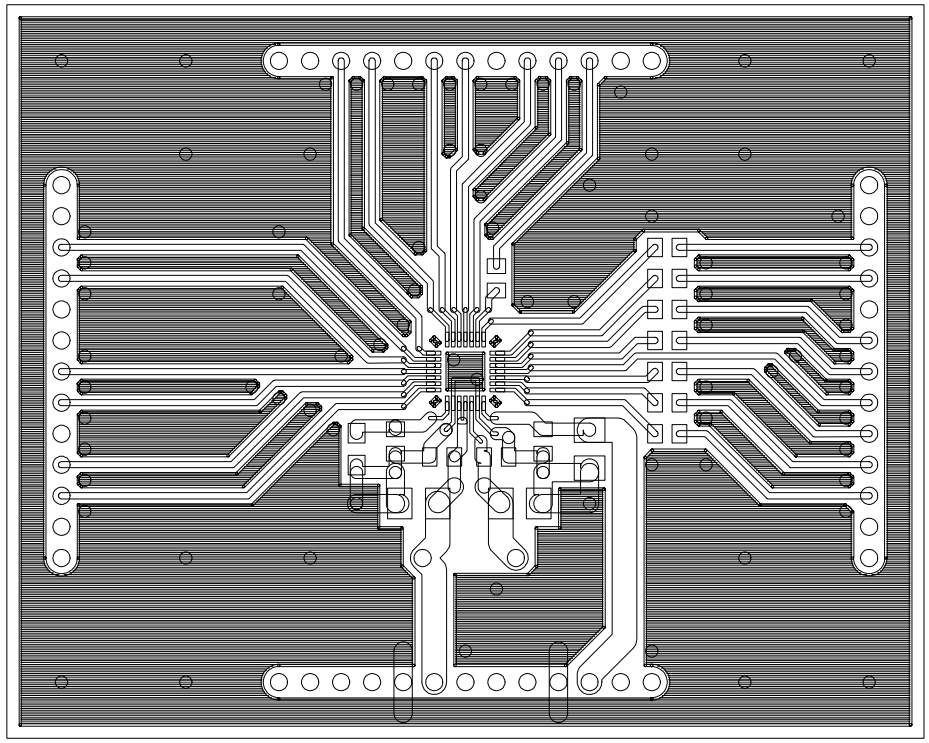
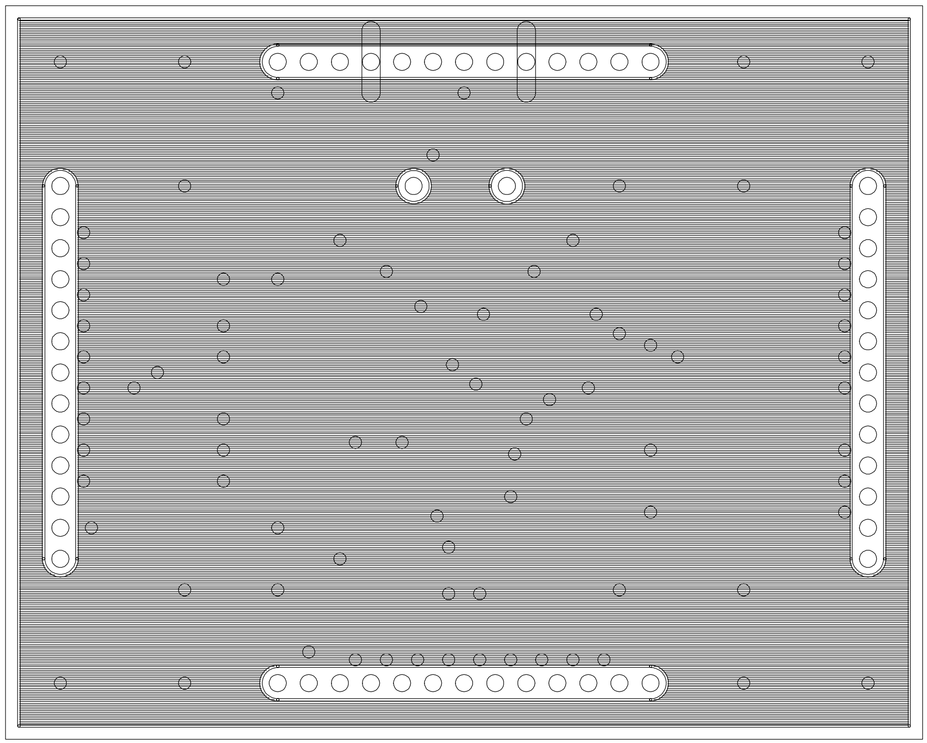
AKD4562SUB(1)



L1 部品面 パターン

AKD4562SUB(1)

AKD4562SUB(1)
L2 半田面 パターン



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