Switched-mode power supply control circuit

5560

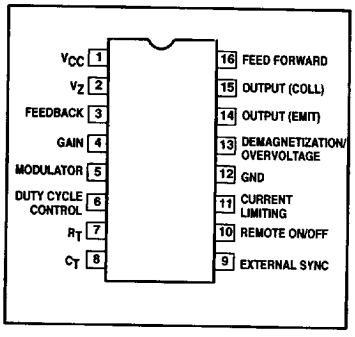
FEATURES

- Stabilized power supply
- Temperature compensated reference source
- Sawtooth generator
- Pulse width modulator
- Remote on/off switching
- Current limiting
- Low supply voltage protection
- Loop fault protection
- Demagnetization/overvoltage protection
- Maximum duty cycle clamp
- Feed forward control
- External synchronization

DESCRIPTION

The 5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener references, sawtooth generator, pulse width modulator, output stage and various protection circuits.

PIN CONFIGURATION



ORDERING INFORMATION

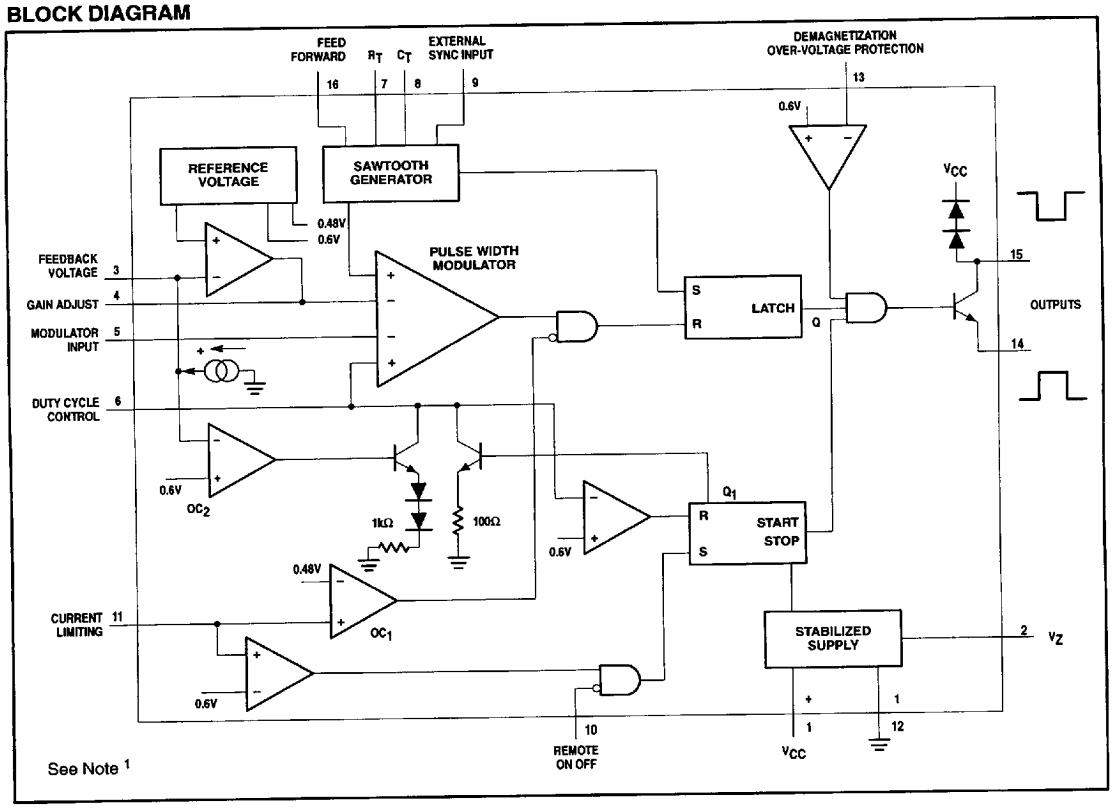
DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
16-Pin Ceramic DIP	5560/BEA	GDIP1-T16

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING[2]	UNIT
	Supply[1]		
V_S	Voltage forced mode	+18	V
I_S	Current fed mode	30	mA
	Output transistor (at 20 - 30V max)		
I_C	Output current	40	mA
V_C	Collector voltage (Pin 15)	V_{CC} + 1.4V	V
V_E	Max. emitter voltage (Pin 14)	+5	V
T_{STG}	Storage temperature range	-65 to +150	°C

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

V_{CC} = 12V, unless otherwise specified.

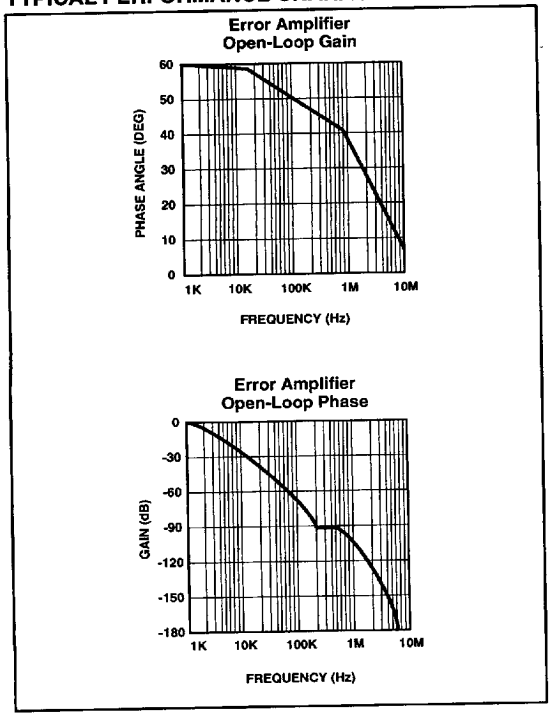
SYMBOL	PARAMETER	TEST CONDITIONS	T_{amb} = +25°C			T_{amb} = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section									
V_{REF}	Internal reference voltage		3.69	3.72	3.81	3.65		3.85	V
$\Delta V_{REF}/\Delta T$	Temperature coefficient						-100		ppm/°C
V_Z	Internal Zener reference	I_L = -7mA	7.8	8.4	8.8				V
$\Delta V_Z/\Delta T$	Temperature coefficient						200		ppm/°C
Oscillator Section									
f_R	Frequency range		50		100k	50		100k	Hz
Δf_R	Initial accuracy oscillator	R = 5kΩ		5					%
D.C.	Duty cycle range[4]	f_o = 20kHz	0		98				%
Modulator, Pin 5									
I_I	Modulation input current	Voltage at Pin 5 = 2V			20			20	µA
Housekeeping Function									
I_I	Pin 6, input current	Pin 6 = 2V			20			20	µA
D.C. (6)	Pin 6, duty cycle limit control	(for 50% max duty cycle) 15kHz to 50kHz/41% of V_Z	40	50	60				% of duty cycle
$V_{CC(TH)}$	Pin 1, low supply voltage protection thresholds		8	9.0	10.5				V
$V_{TH(3)}$	Pin 3, feedback loop protection trip threshold		400	600	720				mV
I_{fo}	Pin 3, pull up current	Pin 3 = 2V	-7	-15	-35	-7		-35	µA
$V_{TH(13)}$	Pin 13, demagnetization/over voltage protection trip on threshold		470	600	720				mV
$I_{I(13)}$	Pin 13, input current	Pin 13 = 0.25V		-0.6	-10			-20	µA
D.C.-ff	Pin 16, feed forward duty cycle control	Pin 16 = 2V_Z	30	40	50				% original duty cycle
$I_{I(16)}$	*Pin 16, feed forward input[3]	Pin 16 = 16V, V_{CC} = 18V		0.2	5			10	µA
External Synchronization									
$V_{OFF(9)}$	Pin 9 off		0		0.8				V
$V_{ON(9)}$	Pin 9 on		2		V_Z				V
$I_{I(9)}$	Pin 9 sink current	Pin 9 = 0V		-65	-100			-125	µA
Remote									
$V_{OFF(10)}$	Pin 10 off		0		0.8				V
$V_{ON(10)}$	Pin 10 on		2		V_Z				V
$I_{I(10)}$	Pin 10 sink current	Pin 10 = 0V		-85	-100			-125	µA
Current Limiting									
$I_{I(11)}$	Pin 11	Pin 11 = 250mV		-2	-20			-40	µA
$T_{D(11)}$	Single pulse inhibit delay[4] (Pin 11)	Inhibit delay time for 20% overdrive at 40mA I_{OUT}		0.7	0.8				µs
$V_{TH(SD)}$	Trip Levels: Shut down, Slow start		0.500	0.600	0.700				V
$V_{TH(CL)}$	Trip Level: Current limit		0.400	0.480	0.560				V

DC ELECTRICAL CHARACTERISTICS(Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	T_A = +25°C			T_A = -55°C, +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Error Amplifier									
V_{OH}	Output voltage swing		6.2		9.5	6.2		9.5	V
V_{OL}	Output voltage swing				0.7			0.85	V
A_O	Open-loop gain		54	60		50			dB
R_f	Feedback resistor		10k						Ω
BW	Small signal bandwidth			3					MHz
Output Stage									
$V_{CE(SAT)}$	Output collector (Pin 15)	$V_{CE(SAT)}$ I_C = 40mA			0.5				V
$V_{E(MAX)}$	Max emitter voltage (Pin 14)[4]	V_C = 12V, I_E = -200mA	5	6					V
Supply Voltage/Current									
I_{CC}	Pin 1	I_Z = 00, voltage forced			10			15	mA
V_{CC}	Pin 1	I_{CC} = 10mA current fed	20		23				V
V_{CC}	Pin 1	1_{CC} = 30mA current fed	20		30				V

NOTE:
1. See voltage-forced, maximum is 18V; when current-fed maximum is 30mA. See voltage/current-fed supply characteristics curve.
2. Operation beyond limits in the table may impair the useful life of the device.
3. Does not include current for timing resistors or capacitors.
4. This parameter is guaranteed, but not tested.

TYPICAL PERFORMANCE CHARACTERISTICS

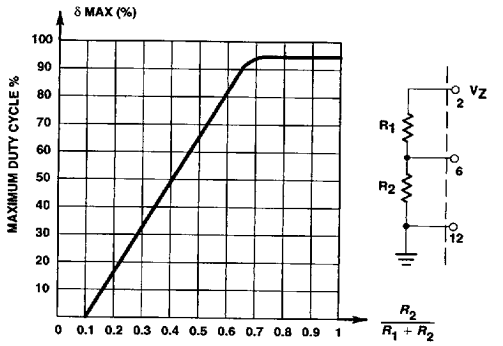


MAXIMUM PIN VOLTAGES

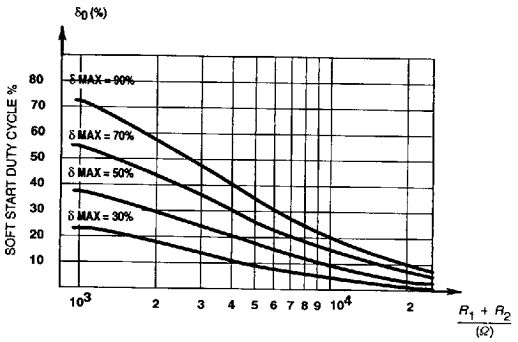
FUNCTION	MAXIMUM VOLTAGE
1. V_{CC}	See Note 1
2. V_Z	Do not force (8.4V)
3. Feedback	V_Z
4. Gain	
5. Modulator	V_Z
6. Duty Cycle Control	V_Z
7. R_T	Current force mode
9. C_T	
9. External Synch	V_Z
10. Remote On/Off	V_Z
11. Current Limiting	V_{CC}
12. GND	GND
13. Demagnetization/Overvoltage	V_{CC}
14. Output (Emit)	V_Z
15. Output (Collector)	V_{CC} + 2Vbe
16. Feed Forward	V_{CC}

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

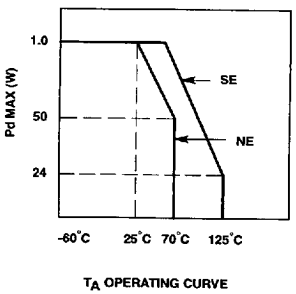
Graph for Determining δ_{MAX}



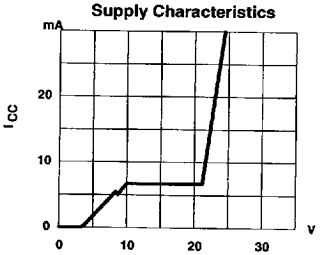
Soft-Start Min. Duty Cycle vs $R_1 + R_2$



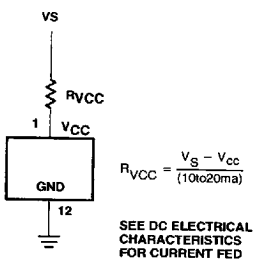
Power Derating Curve



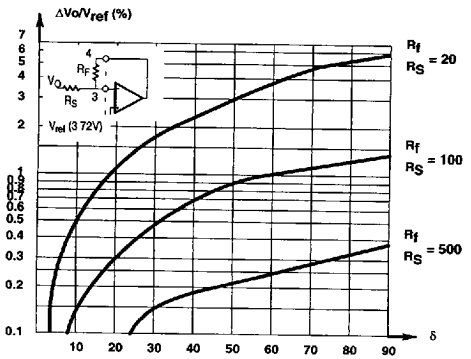
5560 Voltage-/Current-Fed Supply Characteristics



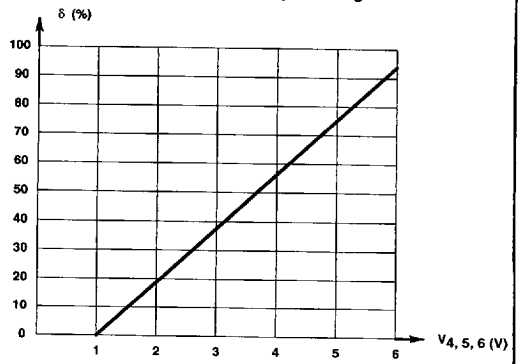
Current-Fed Dropping Resistor



Regulation vs Error Amp Closed-Loop Gain

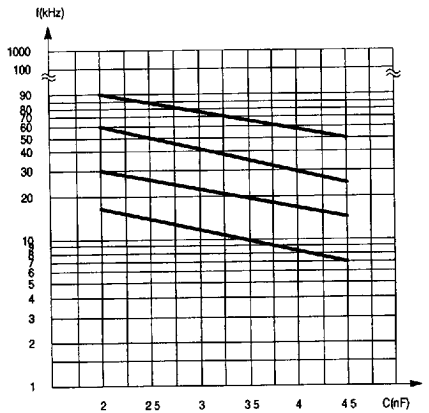


Transfer Curve of Pulse-Width Modulator Duty Cycle vs Input Voltage

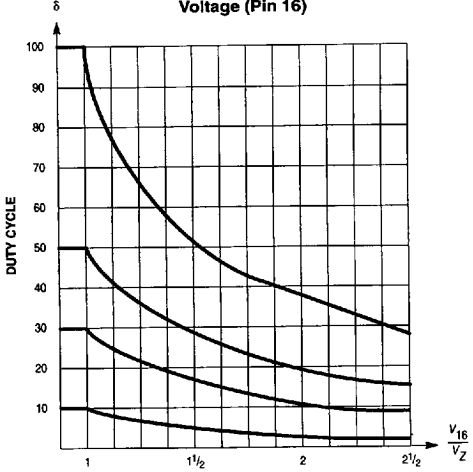


TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

Typical Frequency Plot vs R_T and C_T



Duty Cycle Sensitivity to Feed-Forward Voltage (Pin 16)



THEORY OF OPERATION

The following functions are incorporated:

- A temperature compensated reference source.
- An error amplifier with Pin 3 as input. The output is connected to Pin 4 so that the gain is adjustable with external resistors.
- A sawtooth generator with a TTL-compatible synchronization input (Pins 7,8,9).
- A pulse-width modulator with a duty-cycle range from 0 to 95%.

(The PWM has two additional inputs:

Pin 6 can be used for a precise setting of δ max.

Pin 5 gives a direct access to the modulator, allowing for real constant current operation:)

- A gate at the output of the PWM provides a simple dynamic current limit.
- A latch that is set by the flyback of the sawtooth and reset by the output pulse of the above-mentioned gate prohibits double pulsing.
- Another latch functions as a start-stop circuit; it provides a fast switch-off and a slow start.
- A current protection circuit that operates via the start-stop circuit. This is a combined function with the current limit circuit, therefore Pin 11 has two trip-on levels; the lower one for cycle-by-cycle current limiting, the upper one for current protection by means of switch-off and slow-start.
- A TTL-compatible remote on/off input at Pin 10, also operating via the start-stop circuit.
- An inhibit input at Pin 13. The output pulse can be inhibited immediately.
- An output gate that is commanded by the latches and the inhibit circuit.
- An output transistor of which both the collector (Pin 15) and the emitter (Pin 14) are externally available. This allows for normal or inverse output pulses.
- A power supply that can be either voltage or current driven (Pins 1 and 12). The internally generated stabilized output voltage V_Z is connected to Pin 2.
- A special function is the so-called feed-forward at Pin 16. The amplitude of the sawtooth generator is modulated in such a way that the duty cycle becomes inversely proportional to the voltage on this pin: δ ~ 1/V16
- Loop fault protection circuits assure that the duty-cycle is reduced to zero or a low value for open or short-circuited feedback loops.

Stabilized Power Supply (Pins 1, 2, 12)

The power supply of the 5560 is of the well known series regulation type and provides a stabilized output voltage of typically 8.5V.

This voltage V_Z is also present at Pin 2 and can be used for precise setting of δ max. and to supply external circuitry. Its max. current capability is 5mA.

The circuit can be fed directly from a DC voltage source between 10.5V and 18V or can be current driven via a limiting resistor. In the latter case, internal pinch-off resistors will limit the maximum supply voltage: typical 23V for 10mA and max. 30V for 30mA.

The low supply voltage protection is active when V(1 - 12) is below 10.5V and inhibits the output pulse (no hysteresis).

When the supply voltage surpasses the 10.5V level, the IC starts delivering output pulses via the slow-start function.

The current consumption at 12V is less than 10mA, provided that no current is drawn from V_Z and R(7 - 12) > 20kΩ.

The Sawtooth Generator

Figure 1 shows the principal circuitry of the oscillator. A resistor between Pin 7 and Pin 12 (GND) determines the constant current that charges the timing capacitor C(8 - 12).

This causes a linear increasing voltage on Pin 8 until the upper level of 5.6V is reached. Comparator H sets the RS flip-flop and Q_1 discharges C(8 - 12) down to 1.1V, where comparator L resets the flip-flop. During this flyback time, Q_2 inhibits the output.

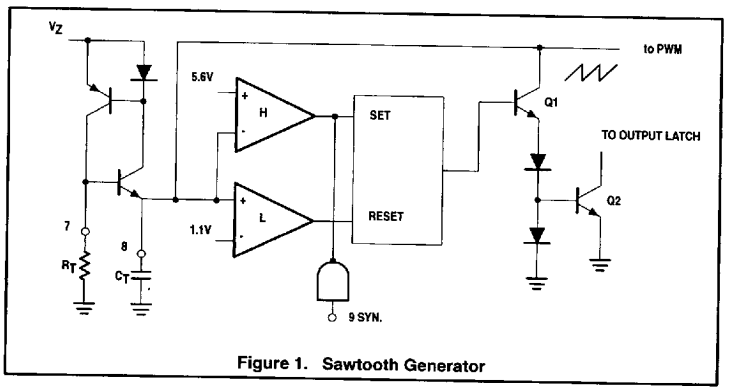


Figure 1. Sawtooth Generator

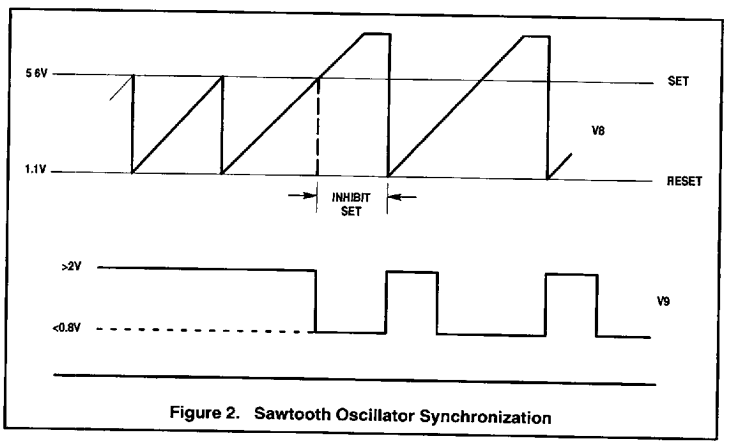


Figure 2. Sawtooth Oscillator Synchronization

Synchronization at a frequency lower than the free-running frequency is accomplished via the TTL gate on Pin 9. By activating this gate (V^9 < 2V), the setting of the sawtooth is prevented. This is indicated in Figure 2.

Figure 3 shows a typical plot of the oscillator frequency against the timing capacitor. The frequency range of the 5560 goes from < 50Hz up to > ~100kHz.

Reference Voltage Source

The internal reference voltage source is based on the bandgap voltage of silicon. Good design practice assures a temperature dependency typically ± 100ppm/°C. The reference voltage is connected to the positive input of the error amplifier and has a typical value of 3.72V.

Error Amp Compensation

For closed-loop gains less than 40dB, it is necessary to add a simple compensation capacitor as shown in Figures 3, 4.

Error Amplifier with Loop-Fault Protection Circuits

This operational amplifier is of a generally used concept and has an open-loop gain of typically 60dB. As can be seen in Figure 4, the inverting input is connected to Pin 3 for a feedback information proportional to V_O.

The output goes to the PWM circuit, but is also connected to Pin 4, so that the required gain can be set with R_S and R(3 - 4). This is indicated in Figure 4, showing the relative change of the feedback voltage as a function of the duty cycle. Additionally, Pin 4 can be used for phase shift networks that improve the loop stability.

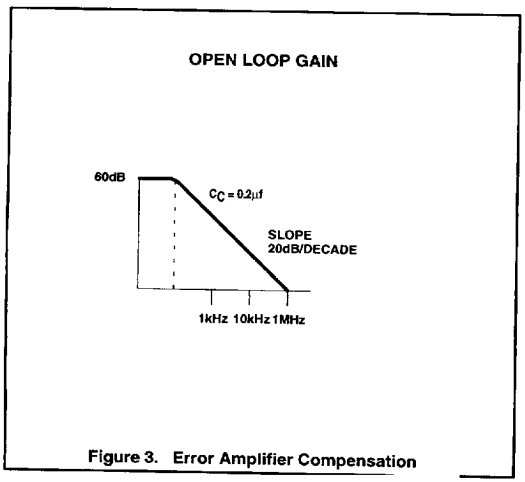


Figure 3. Error Amplifier Compensation

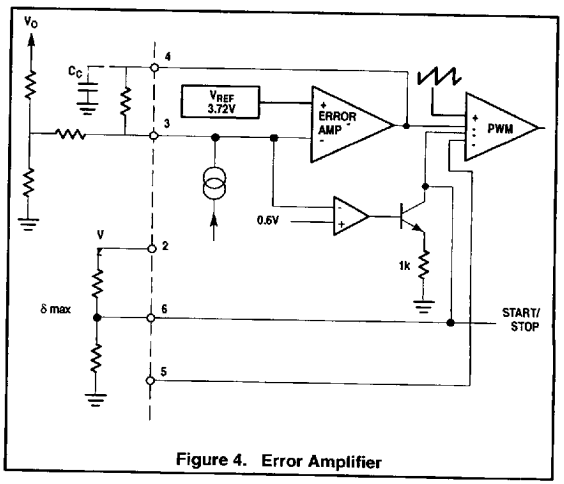
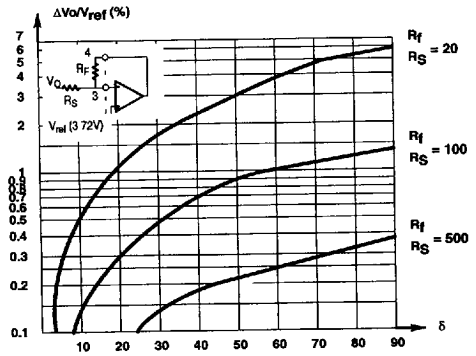
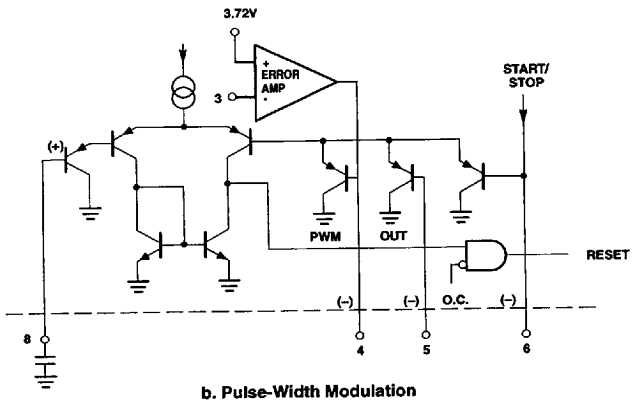


Figure 4. Error Amplifier



a. Duty Cycle – δ – % Regulation



b. Pulse-Width Modulation

Figure 5.

When the SMPS feedback loop is interrupted, the error amplifier would settle in the middle of its active region because of the feedback via R(3 - 4). This would result in a large duty cycle. A current source on Pin 3 prevents this by pushing the input voltage high via the voltage drop over R(3 - 4). As a result, the duty cycle will become zero, provided that R(3 - 4) > 100k. When the feedback loop is short-circuited, the duty cycle would jump to the adjusted max. duty cycle. Therefore, an additional comparator is active for feedback voltages at Pin 3 below 0.6V. Now an internal resistor of typically 1k is shunted to the impedance on the δ_{MAX} setting Pin 6. Depending on this impedance, δ will be reduced to a value δ_o. This will be discussed further.

The Pulse-Width Modulator

The function of the PWM circuit is to translate a feedback voltage into a periodical pulse of which the duty cycle depends on that feedback voltage. As can be seen in Figure 5, the PWM circuit in the 5560 is a long-tailed pair in which the sawtooth on Pin 8 is compared with the LOWEST voltage on either Pin 4 (error amplifier), Pin 5, or Pin 6 (δ_{MAX} and slow-start). The transfer graph is given in Figure 6. The output of the PWM causes the resetting of the output bistable.

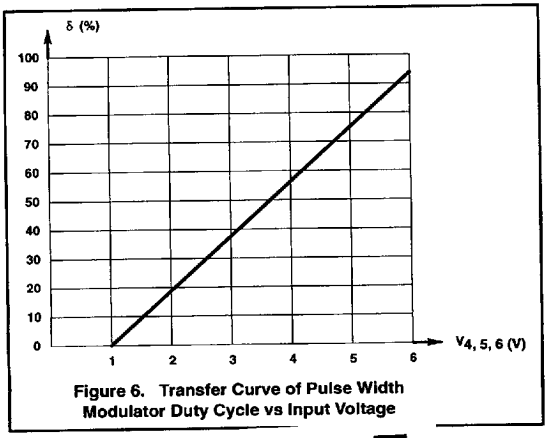


Figure 6. Transfer Curve of Pulse Width Modulator Duty Cycle vs Input Voltage

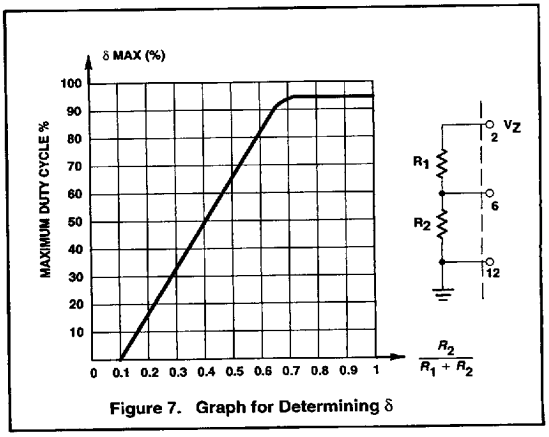


Figure 7. Graph for Determining δ

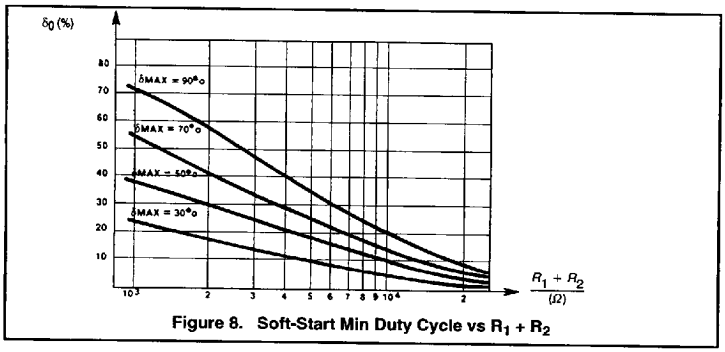


Figure 8. Soft-Start Min Duty Cycle vs $R_1 + R_2$

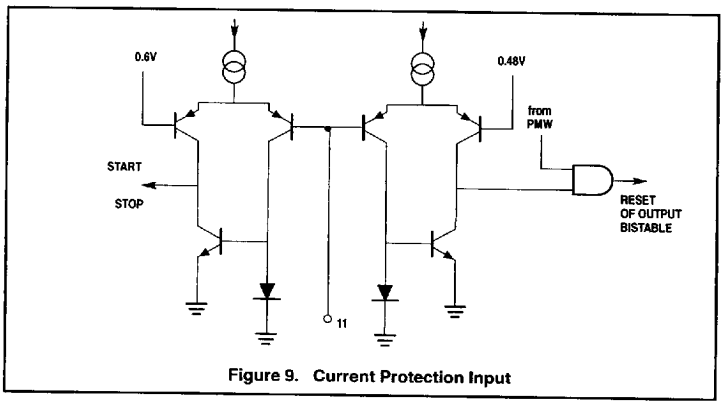


Figure 9. Current Protection Input

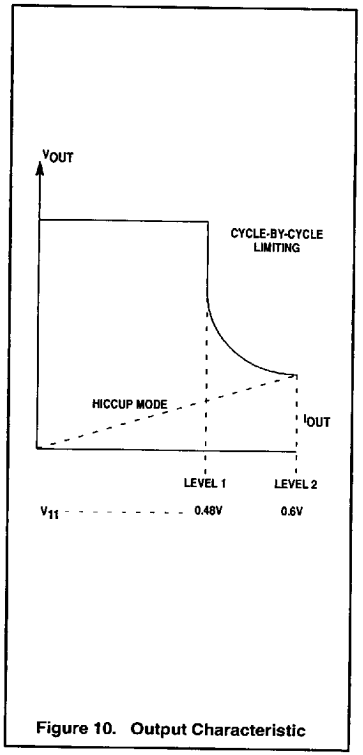


Figure 10. Output Characteristic

Limitation of the Maximum Duty Cycle

With Pins 5 and 6 not connected and with a rather low feedback voltage on Pin 3, the 5560 will deliver output pulses with a duty cycle of ≈95%. In many SMPS applications, however, this high δ will cause problems. Especially in forward converters, where the transformer will saturate when δ exceeds 50%, a limitation of the max. duty-cycle is a must.

A DC voltage applied to Pin 6 (PWM input) will set δ_{MAX}, at a value in accordance with Figure 6. For low tolerances of δ_{MAX}, this voltage on Pin 6 should be set with a resistor divider from V_Z (Pin 2). The upper and lower sawtooth levels are also set by means of an internal resistor divider form V_Z, so forming a bridge configuration with the δ_{MAX} setting is low because tolerances in V_Z are compensated and the sawtooth levels are determined by internal resistor matching rather than by absolute resistor tolerance. Figure 7 can be used for determining the tap on the bleeder for a certain δ_{MAX} setting

As already mentioned, Figure 7 gives a graphical representation of this. The value δ_O is limited to the lower and the higher side;

- It must be large enough to ensure that at max. load and min. input voltage the resulting feedback voltage on Pin 3 exceeds 0.6V.
- It must be small enough to limit the amount of energy in the SMPS when a loop-fault occurs. In practice a value of 10 - 15% will be a good compromise.

Extra PWM Input (Pin 5)

The PWM has an additional inverting input: Pin 5. It allows for attacking the duty cycle via the PWM circuit, independently from the feedback and the δ_{MAX} information. This is necessary when the SMPS must have a real constant current behavior, possibly with a fold-back characteristic. However, the realization of this feature must be done with additional external components. When not used, Pin 5 should be tied to Pin 6.

Dynamic Current Limit and Current Protection (Pin 11)

In many applications, it is not necessary to have a real constant current output of the SMPS.

Protection of the power transistor will be the prime goal. This can be realized with the 5560 in an economical way. A resistor (or a current transformer) in the emitter of the power transistor gives a replica of the collector current. This signal must be connected to Pin 11. As can be seen in Figure 9, this input has two comparators with different reference levels. The output of the comparator with the lower 0.48V reference is connected to the same gate as the output of the PWM.

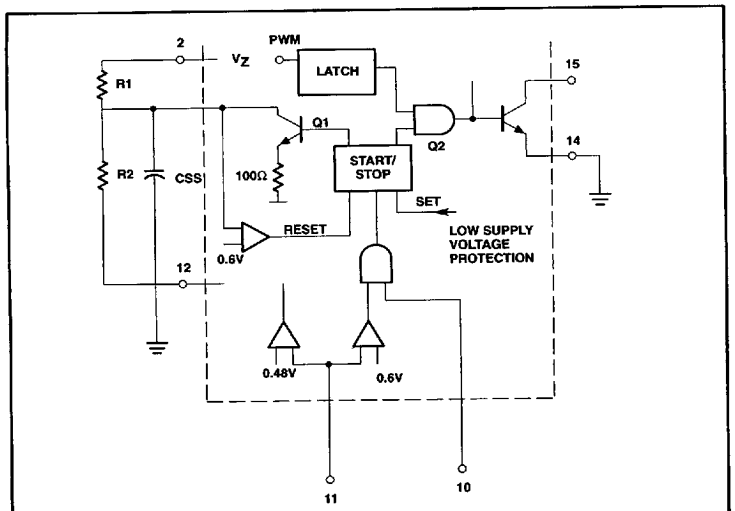


Figure 11. Start/Stop Circuit

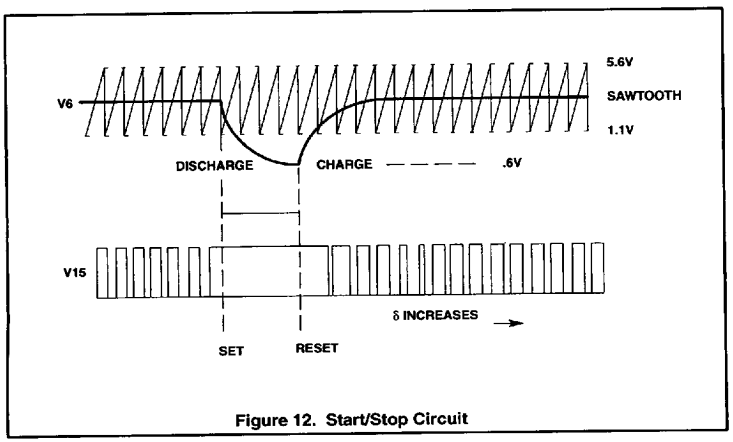


Figure 12. Start/Stop Circuit

When activated, it will immediately reset the output flip-flop, so reducing the duty cycle. The effectiveness of this cycle-by-cycle current limit diminishes at low duty cycle values. When δ becomes very small, the storage time of the power transistor becomes dominant. The current will now increase again, until it surpasses the reference of the second comparator. The output of this comparator activates the start/stop circuit and causes an immediate inhibit of the output pulses. After a certain dead-time, the circuit starts again with very narrow output pulses. The effect of this two-level current protection circuit is visualized in Figure 10.

The Start/Stop Circuit

The function of this protection circuit is to stop the output pulses as soon as a fault occurs and to keep the output stopped for several periods.

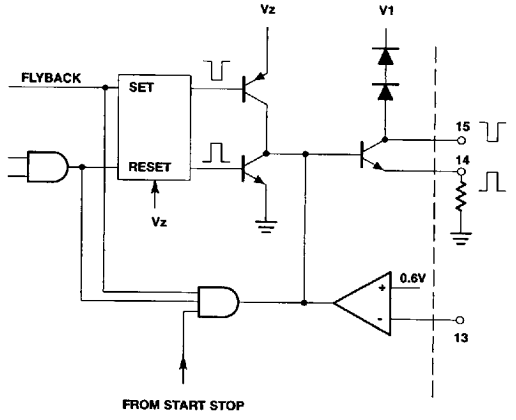
After this dead-time, the output starts with a very small, gradually increasing duty cycle. When the fault is persistent, this will cause a cyclic switch-off/switch-on condition. This "hiccup" mode limits effectively the energy during fault conditions. The realization and the working of the circuit is indicated in the Figures 11 and 12. The dead-time and the soft-start are determined by an external capacitor that is connected to Pin 6 (δ_{MAX} setting).

A RS flip-flop can be set by three different functions:

1. Remote on/off on Pin 10.
2. Overcurrent protection on Pin 11.
3. Low supply voltage protection (internal).

As soon as one of these functions cause a setting of the flip-flop, the output pulses are blocked via the output gate. In the same time transistor Q_1 is forward-biased, resulting in a discharge of the capacitor on Pin 6.

The discharging current is limited by an internal 150Ω resistor in the emitter of Q_1. the voltage at Pin 6 decreases to below the lower level of the sawtooth. When V6 has dropped to 0.6V, this will activate a comparator and the flip-flop is reset. The output stage is no longer blocked and Q_1 is cut-off. Now V_Z will charge the capacitor via R_1 to the normal δ_{MAX} voltage. The output starts delivering very narrow pulses as soon as V_6 exceeds the lower sawtooth level. The duty-cycle of the output pulse now gradually increases to a value determined by the feedback on Pin 3, or by the static δ_{MAX} setting on Pin 6.



NOTE: The signal V13 can be derived from the demagnetizing winding in a forward converter as shown below

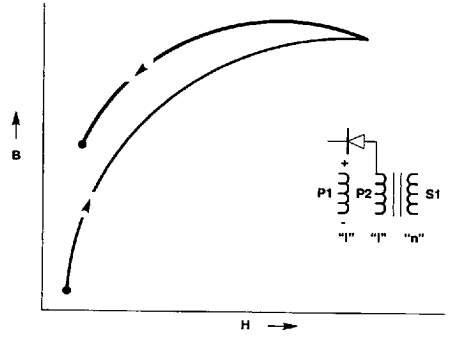


Figure 13. Output Stage

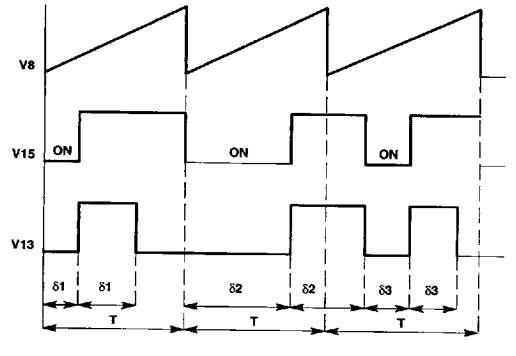


Figure 14. Output Stage Inhibit

Remote On/Off Circuit (Pin 10)

In systems where two or more power supplies are used, it is often necessary to switch these supplies on and off in a sequential way.

Furthermore, there are many applications in which a supply must be switched by a logical signal. This can be done via the TTL-compatible remote on/off input on Pin 10. The output pulse is inhibited for levels below 0.8V. The output of the IC is no longer blocked when the remote on/off input is left floating or when a voltage > 2V is applied. Start-up occurs via the slow-start circuit.

The Output Stage

The output stage of the 5560 contains a flip-flop, a push-pull driven output transistor, and a gate, as indicated in Figure 13. The flip-flop is set by the flyback of the sawtooth. Resetting occurs by a signal either from the PWM or the current limit circuit. With this configuration, it is assured that the output is switched only once per period, thus prohibiting double pulsing. The collector and emitter of the output transistor are connected respectively to Pin 15 and Pin 14, allowing for normal or inverted output pulses. An internally grounded emitter would cause intolerable voltage spikes over the bonding wire, especially at high output currents.

This current capability of the output transistor is 40mA peak for $V_{CE} \cong 0.4V$. An internal clamping diode to the supply voltage protects the collector against overvoltages. The max. voltage at the emitter (Pin 14) must not exceed +5V. A gate, activated by one of the set or reset pulses, or by a command from the start-stop circuit will immediately switch-off the output transistor by short-circuiting its base. The external inhibitor (Pin 13) operates also via this base.

Demagnetization Sense

As indicated in Figure 13, the output of this NPN comparator will block the output pulse, when a voltage above 0.6V is applied to Pin 13. A specific application for this function is to prevent saturation of forward converter transformers. This is indicated in Figure 14.

Feed-Forward (Pin 16)

The basic formula for a forward converter is

$$V_{OUT} = \frac{\delta V_{IN}}{n} \quad \text{(n=transformer ratio)}$$

This means that in order to keep V_{OUT} at a constant value, the duty cycle δ must be made inversely proportional to the input voltage. A preregulation (feed-forward) with the function $\delta \sim 1/V_{IN}$ can ease the feedback-loop design.

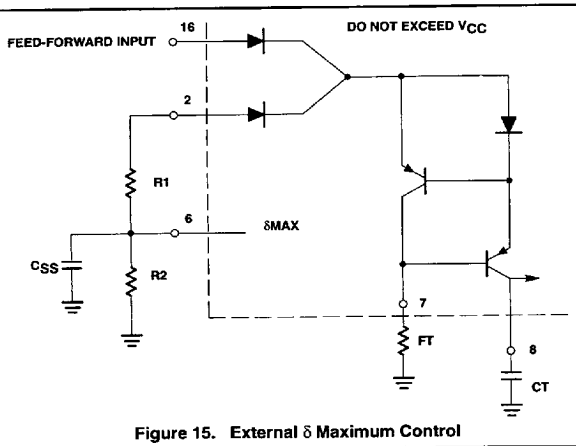


Figure 15. External δ Maximum Control

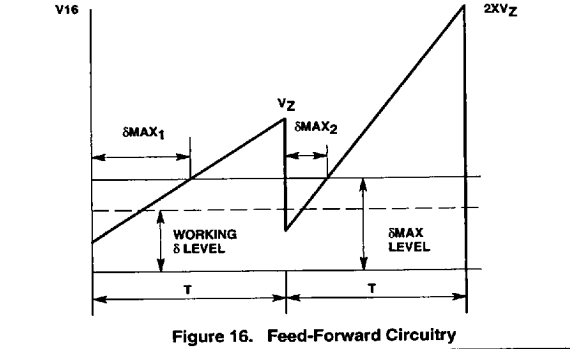


Figure 16. Feed-Forward Circuitry

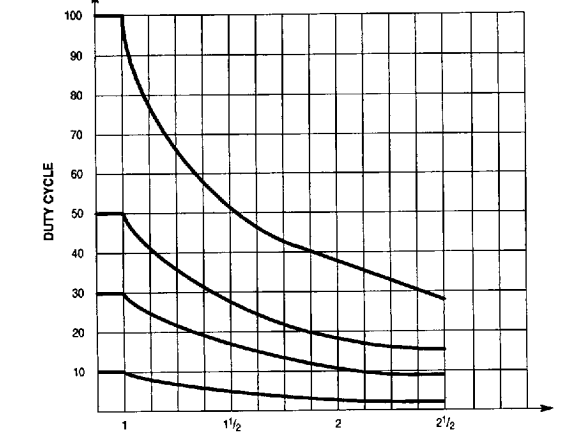


Figure 17. Feed-Forward Regulation

This loop now only has to regulate for load variations, which require only a low feedback gain in the normal operation area. The transformer of a forward converter must be designed in such a way that it does not saturate, even under transient conditions, where the max. inductance is determined by $\delta_{MAX} \times V_{IN}$ max. A regulation of $\delta_{MAX} \sim 1/V_{IN}$ will allow for a considerable reduction or simplification of the transformer. The function of $\delta \sim 1/V_{IN}$ can be realized by using Pin 16 of the 5560.

Figure 15 shows the electrical realization. When the voltage at Pin 16 exceeds the stabilized voltage V_Z (Pin 2), it will increase the charging current for the timing capacitor on Pin 8.

The operating frequency is not affected, because the upper trip level for sawtooth increases also. Note that the δ_{MAX} voltage on Pin 6 remains constant because it is set via V_Z. Figure 16 visualizes the effect on δ_{MAX} and the normal operating duty cycle δ. For $V_{16} = 2 \times V_Z$ these duty cycles have halved. The graph for $\delta = f(V_{16})$ is given in Figure 17. (Note: V_{16} must be less than Pin 1 voltage.)

APPLICATIONS

5560 Push-Pull Regulator

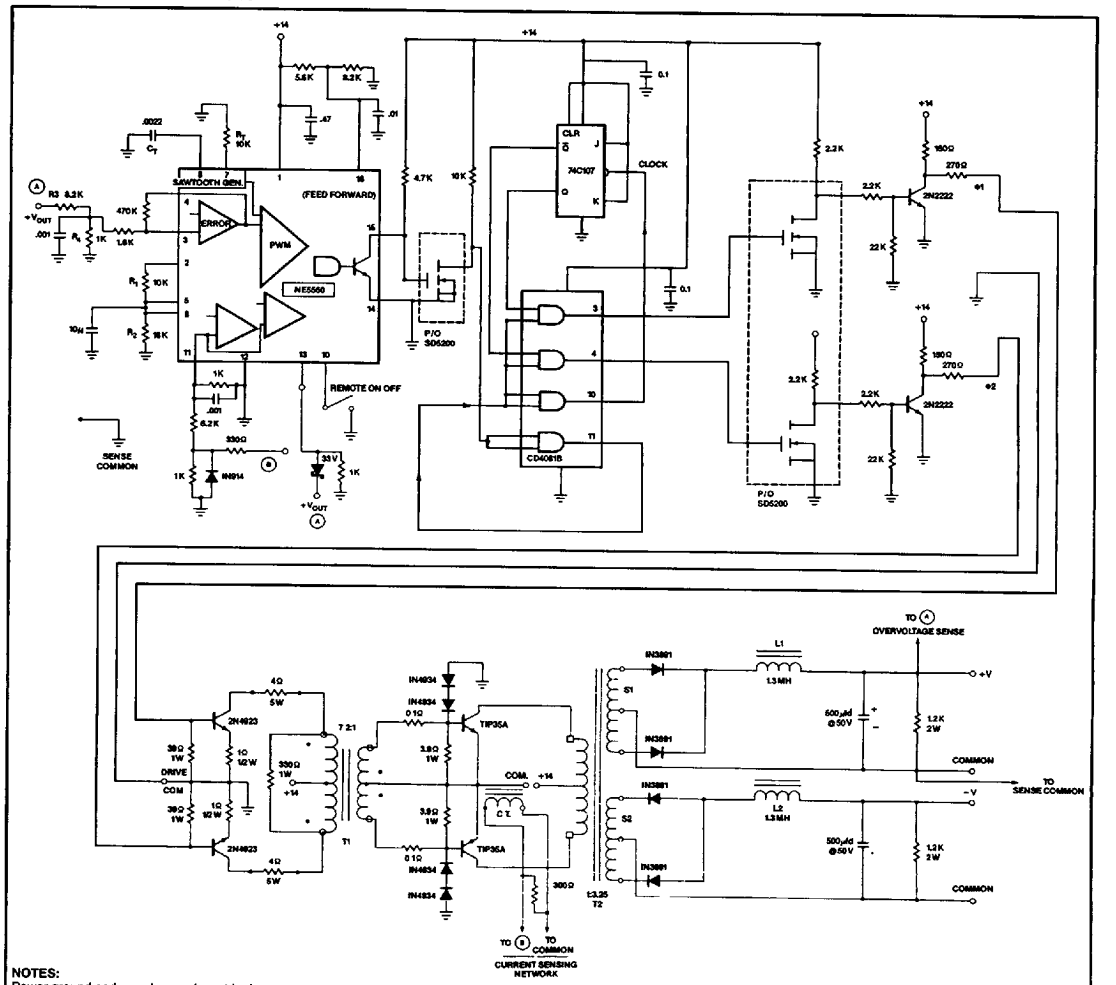
This application describes the use of the Philips Semiconductors 5560 adapted to function as a push-pull switched mode regulator, as shown in Figures 18 and 19.

Input voltage range is +12 to +18V for a nominal output of +30 and -30V at a max. load current of 1A with an average efficiency of 81%.

Features include feed-forward input compensation, cycle-to-cycle drive current protection and other voltage sensing, line (to positive output) regulation < 1% for an input range of +13 to +18V and load regulation to positive output of < 3% for $\Delta I_L(+)$ of 0.1 to 1A.

The main pulse width modulator operates to 48kHz with power switching at 24kHz.

TYPICAL APPLICATION

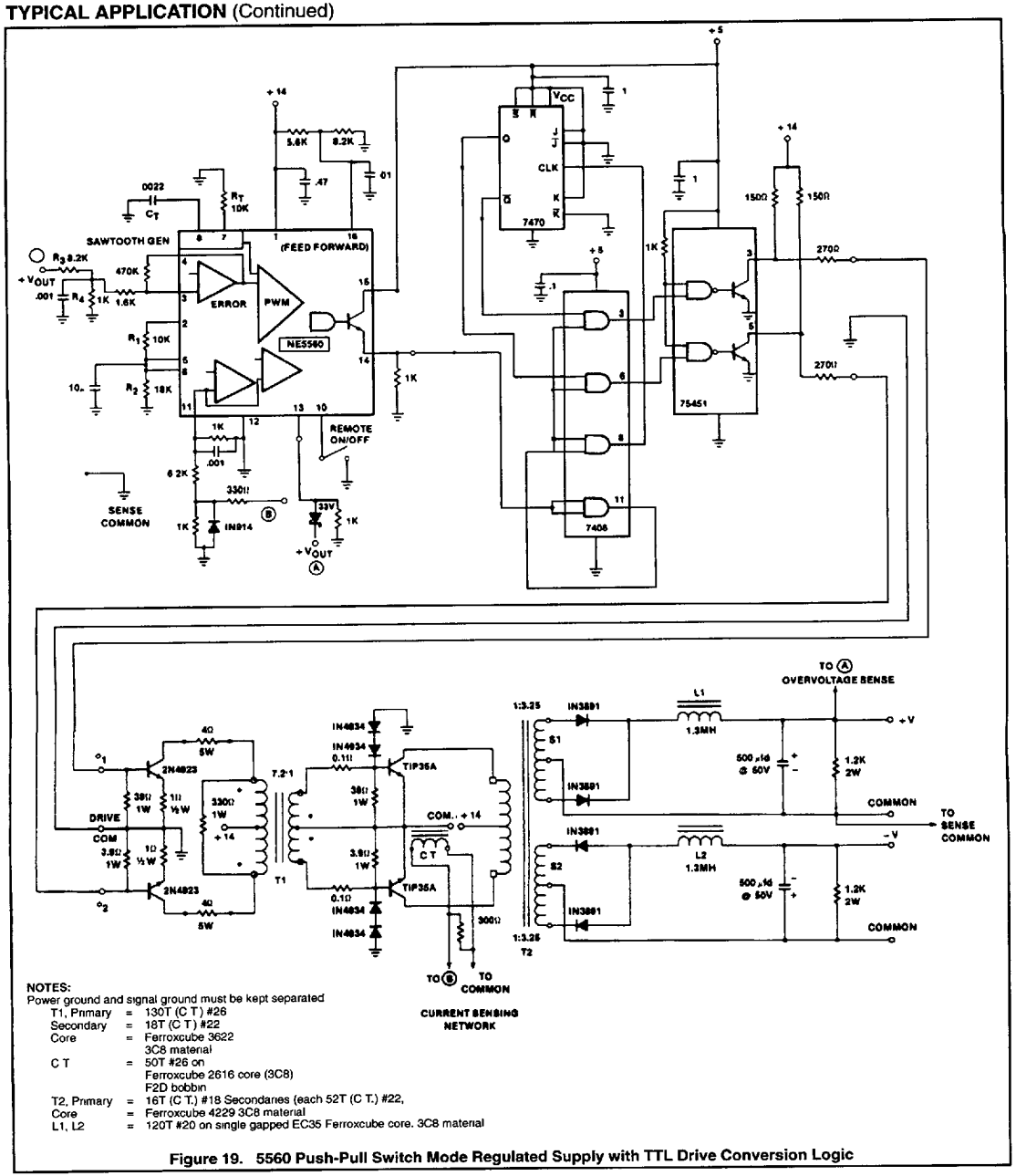


NOTES:
Power ground and signal ground must be kept separated

T1, Primary	=	130T (C T) #26
Secondary	=	18T (C T) #22
Core	=	Ferroxcube 3622 3C8 material
C T	=	50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin
T2, Primary	=	16T (C T) #18 Secondaries (each 52T (C T) #22,
Core	=	Ferroxcube 4229 3C8 material
L1, L2	=	120T #20 on single gapped EC35 Ferroxcube core 3C8 material

Figure 18. 5560 Push-Pull Switch Mode Regulated Supply with CMOS Drive Conversion Logic

TYPICAL APPLICATION (Continued)



NOTES:
Power ground and signal ground must be kept separated

T1, Primary	=	130T (C T) #26
Secondary	=	18T (C T) #22
Core	=	Ferroxcube 3622 3C8 material
C T	=	50T #26 on Ferroxcube 2616 core (3C8) F2D bobbin
T2, Primary	=	16T (C T.) #18 Secondaries (each 52T (C T.) #22,
Core	=	Ferroxcube 4229 3C8 material
L1, L2	=	120T #20 on single gapped EC35 Ferroxcube core. 3C8 material

Figure 19. 5560 Push-Pull Switch Mode Regulated Supply with TTL Drive Conversion Logic