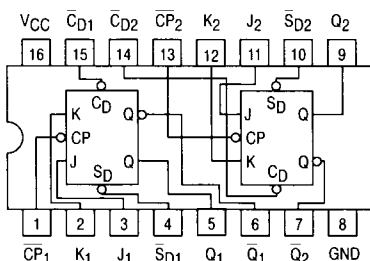




DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

The MC74F112 contains two independent, high-speed JK flip-flops with Direct Set and Clear inputs. Synchronous state changes are initiated by the falling edge of the clock. Triggering occurs at a voltage level of the clock and is not directly related to the transition time. The J and K inputs can change when the clock is in either state without affecting the flip-flop, provided that they are in the desired state during the recommended setup and hold times relative to the falling edge of the clock. A LOW signal on $\overline{S_D}$ or $\overline{C_D}$ prevents clocking and forces Q or $\overline{Q}$ HIGH, respectively. Simultaneous LOW signals on $\overline{S_D}$ and $\overline{C_D}$ force both Q and $\overline{Q}$ HIGH.

CONNECTION DIAGRAM



FUNCTION TABLE (Each Half)

Inputs		Output
@ t_n		@ $t_n + 1$
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\overline{Q}_n$

Asynchronous Inputs:

LOW Input to $\overline{S_D}$ sets Q to HIGH level

LOW Input to $\overline{C_D}$ sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on $\overline{C_D}$ and $\overline{S_D}$ makes both Q and $\overline{Q}$ HIGH

H = HIGH Voltage Level

L = LOW Voltage Level

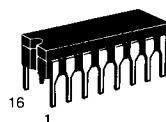
t_n = Bit time before clock pulse

$t_n + 1$ = Bit time after clock pulse

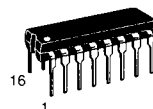
MC74F112

DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

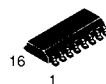
FAST™ SCHOTTKY TTL



J SUFFIX
CERAMIC
CASE 620-09



N SUFFIX
PLASTIC
CASE 648-08

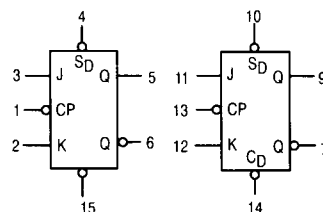


D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

MC74FXXXJ Ceramic
MC74FXXXN Plastic
MC74FXXXD SOIC

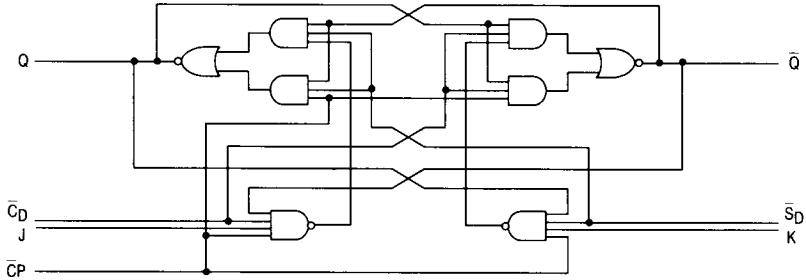
LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

MC74F112

LOGIC DIAGRAM (one half shown)



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	74	4.5	5.0	5.5	V
T _A	Operating Ambient Temperature Range	74	0	25	70	°C
I _{OH}	Output Current — High	74			–1.0	mA
I _{OL}	Output Current — Low	74			20	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage
V _{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage
V _{IK}	Input Clamp Diode Voltage			–1.2	V	I _{IN} = –18 mA V _{CC} = MIN
V _{OH}	Output HIGH Voltage	74	2.5	3.4	V	I _{OH} = –1.0 mA V _{CC} = 4.50 V
		74	2.7	3.4	V	I _{OH} = –1.0 mA V _{CC} = 4.75 V
V _{OL}	Output LOW Voltage		0.35	0.5	V	I _{OL} = 20 mA V _{CC} = MIN
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V
				100	μA	V _{CC} = MAX, V _{IN} = 7.0 V
I _{IL}	Input LOW Current (J and K Inputs)			–0.6	mA	V _{CC} = MAX, V _{IN} = 0.5 V
	(C _P Inputs)			–2.4	mA	
	(C _D and S _D Inputs)			–3.0	mA	
I _{OS}	Output Short Circuit Current (Note 2)	–60		–150	mA	V _{CC} = MAX, V _{OUT} = 0 V
I _{CC}	Power Supply Current		12	19	mA	V _{CC} = MAX, V _{CP} = 0 V

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- Not more than one output should be shorted at a time, nor for more than 1 second.

MC74F112

AC CHARACTERISTICS

Symbol	Parameter	74F		74F		Unit
		T _A = +25°C V _{CC} = +5.0 V C _L = 50 pF		T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10% C _L = 50 pF		
		Min	Max	Min	Max	
		Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	110				MHz
t _{PLH}	Propagation Delay	2.0	6.5	2.0	7.5	ns
t _{PHL}	$\overline{CP}_n$ to Q _n or $\overline{Q}_n$	2.0	6.5	2.0	7.5	
t _{PLH}	Propagation Delay	2.0	6.5	2.0	7.5	ns
t _{PHL}	$\overline{CD}_n$ or $\overline{SD}_n$ to Q _n or $\overline{Q}_n$	2.0	6.5	2.0	7.5	

AC OPERATING REQUIREMENTS

Symbol	Parameter	74F			74F		Unit
		T _A = +25°C V _{CC} = +5.0 V			T _A = 0°C to +70°C V _{CC} = 5.0 V ± 10%		
		Min	Typ	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	4.0			4.0		ns
t _S (L)	J _N or K _N to $\overline{CP}_N$	3.0			3.0		
t _H (H)	Hold Time, HIGH or LOW	0			0		
t _H (L)	J _N or K _N to $\overline{CP}_N$	0			0		ns
t _w (H)	$\overline{CP}_N$ Pulse Width, HIGH	4.5			4.5		
t _w (L)	or LOW	4.5			4.5		ns
t _w (L)	$\overline{CD}_N$ or $\overline{SD}_N$ Pulse Width, LOW	4.5			4.5		ns
t _{rec}	Recovery Time $\overline{CD}_N$ or $\overline{SD}_N$ to CP	4.0			5.0		ns