iPLD610
FAST 16-MACROCELL CMOS PLD

Function, Pin, and JEDEC Compatible with EP600, EP610, EP610A, EP630, PALCE610, 85C060 and 5C060 PLDs

- t_{PD} 10 ns, 100 MHz Counter Frequency (w/Internal Feedback)
- I_{CC} = 105 mA max. @ 1 MHz
- Programmable Low-Power Option for "Standby" Operation; 20 μA Typ. in Standby Mode
- Clocking Speed Same as −7 ns PAL* (74 MHz w/External Feedback)
- 16 Macrocells with Programmable I/O Architecture (Register/Combinatorial). Registers Configurable as D/T/JK/RS Types
- Up to 20 Inputs (4 Dedicated and 16 I/O)
- 8 P-Terms, Selectable SOP Invert, Clear and OE P-Terms for Each Macrocell
- Programmable Clock System with 2 Synchronous Clocks and Asynchronous Clocking Option on all Registers
- Extensive Software and Programming Support via Intel and Third Party Tools
- 1-Micron CMOS* III-E EPROM Technology
- Programmable "Security Bit" Allows Total Protection of Proprietary Designs
- 100% Generically Tested Logic Array
- Available in 300-mil 24-Pin PDIP, CerDIP and 28-Pin PLCC Packages

  (See Packaging Specifications Order Number #240800-001, Package Type N and P)

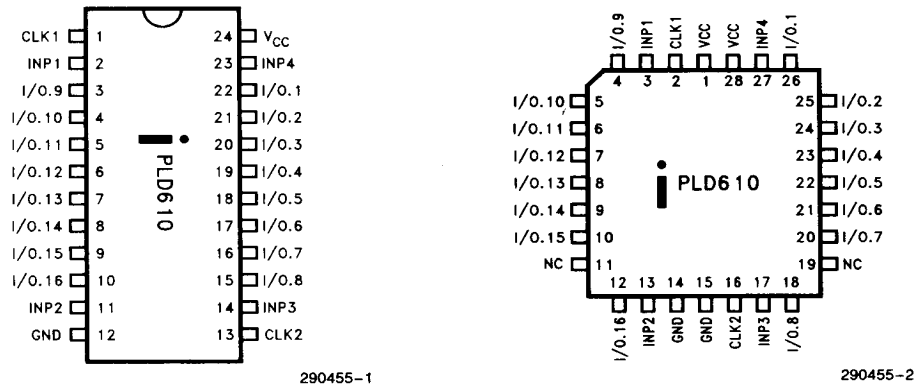


Figure 1. iPLD610 Pin Configurations

*PAL is a registered trademark of Advanced Micro Devices, Inc.

October 1993
Order Number: 290455-002

INTRODUCTION

The iPLD610 is a high-performance, high-integration, general-purpose CMOS PLD. The iPLD610 PLD (Programmable Logic Device) accommodates logic functions with up to 20 inputs and 16 I/O macrocells. Each I/O macrocell includes 8 product-terms (p-terms) for input, a separate clear p-term, and an output enable/asynchronous clock p-term. The iPLD610 is function-, pin-, and JEDEC-compatible with the EP600, EP610, EP610A, EP630, PALCE610, 85C060 and 5C060 PLDs. With a clocking speed of 74 MHz (w/external feedback) the iPLD610 offers a higher integration, lower power alternative to registered −7 ns PALs/GALs.

The iPLD610 uses CMOS EPROM (floating gate) cells as logic control elements instead of fuses. The CMOS EPROM technology reduces power consumption in comparison to bipolar devices without sacrificing speed performance. In addition, Intel's advanced CMOS III-E EPROM process technology enables higher logic densities to be achieved with superior speed and low-power performance over other comparable devices. Intel's µPLDs add the benefits of "zero" stand-by power not available on other programmable logic devices. EPROM technology allows these devices to be 100% factory tested by programming and erasing all the EPROM logic control elements.

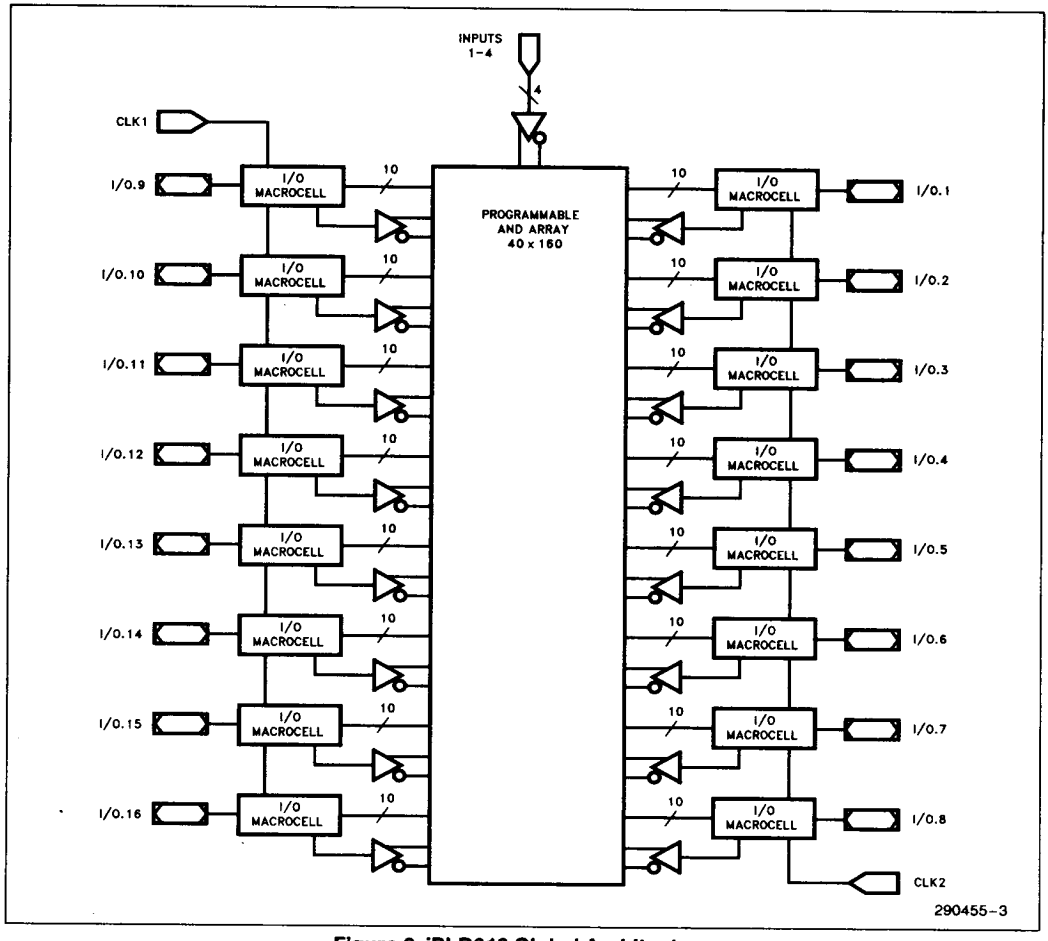


Figure 2. iPLD610 Global Architecture

The architecture of the iPLD610 is based on the "Sum of Products" PLA (Programmable Logic Array) structure with a programmable AND array feeding into a fixed OR array. The device accommodates combinational and sequential logic functions. A programmable I/O architecture provides individual selection of either combinatorial or registered output and feedback signals all with selectable polarity.

A feature unique to the iPLD610 is the ability to individually program the output registers as a D-, T-, SR-, or JK-type Flip-Flop without sacrificing the utilization of programmable AND logic. Each output register can be individually clocked from any of the input or feedback paths available within the AND array. With these features, a wide variety of logic functions can be simultaneously implemented–all on the same device.

ARCHITECTURE DESCRIPTION

Externally, the iPLD610 has 4 dedicated data input pins, 16 I/O pins that may be configured for input, output, or bidirectional operations, and 2 synchronous clock inputs. The iPLD610 is contained in a 24-pin ceramic windowed or OTP plastic (300 mils) or 28-lead OTP J-leaded chip carrier package.

The basic Macrocell architecture for the iPLD610 is shown in Figure 3. The iPLD610 has 16 of these Macrocells (one for each I/O pin). The Macrocell is organized in the familiar sum-of-products structure with a programmable AND array attached to a fixed OR term. The inputs to the programmable AND array originate from the true and complement signals from each of the dedicated input pins and each of the I/O control blocks. The 40-input AND array of the iPLD610 feeds 160 AND gates (product terms) which are distributed among the 16 Macrocells in the device.

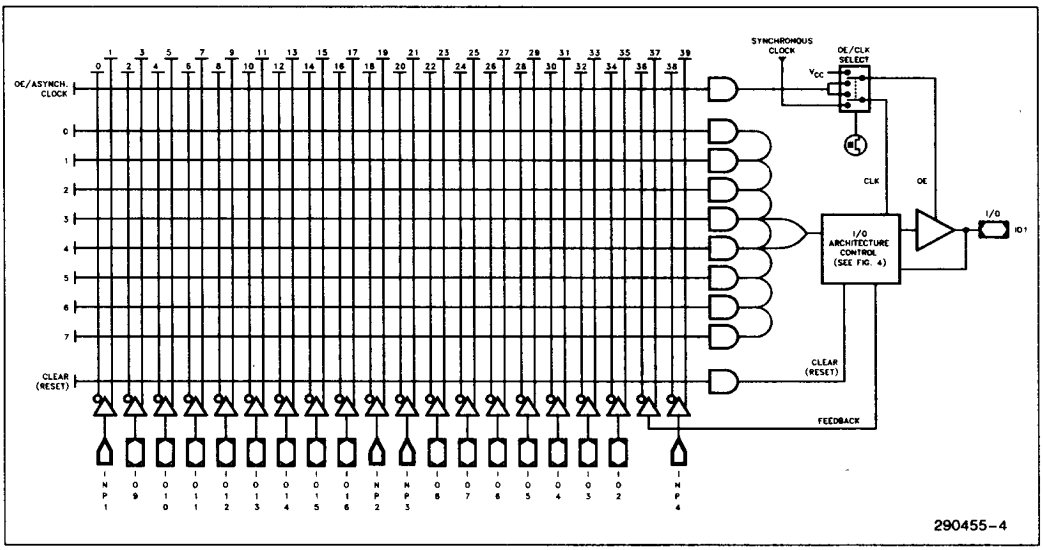


Figure 3. iPLD610 Macrocell Architecture

Each Macrocell contains ten product terms. Eight of the ten product terms (AND gates) are dedicated for the SOP logic implementation. One product term on each Macrocell is used for RESET control to the output register associated with the Macrocell. The final product term is used for OE/Asynchronous Clock implementation.

Within the AND array, there is an EPROM connection at every intersection of an input signal (true and complement) and a product term to a given Macrocell. Before programming an erased device, every EPROM connection is made at every intersection. But during the programming process, these connections are opened so that only the desired connections remain. Therefore, the true or complement of any input signal can be connected to any product term. If both the true and complement connections of any signal are left intact, a logical false results on the output of the AND gate. However, if both the true and complement connections are open, then a logic "don't care" results on the AND gate. Lastly, if all the inputs of a product term are programmed open, then a logical true results on the output of the AND gate.

The iPLD610 has two dedicated clock inputs to provide synchronous clock signals to the internal registers. Each of the clock signals controls half the total registers within the given device. For example, CLK1 provides synchronous clocking to the registers in Macrocells in the left half of the array while CLK2 controls the registers associated with Macrocells in the right half of the array. The advanced I/O architecture allows for any number of the registers to be synchronously clocked (from none to all). Both of the dedicated clock inputs latch the data into a given register when triggered on a positive edge.

MACROCELL ARCHITECTURE SELECTION

The iPLD610 architecture provides each Macrocell with over 50 different possible I/O register configurations. Each I/O pin can be configured for combinatorial or registered output (true or complement) with feedback. In addition, four different types of output registers can be implemented on I/O pin without any additional logic requirements. The feedback mechanism for each register back into the AND array can be programmed to provide for either registered feedback from the Macrocell or input feedback (treating the pin as an input). Another advantage of the advanced I/O capability of the iPLD610 is the ability to individually clock each internal register from asynchronous clock signals.

Invert Select EPROM Bit

The Invert Select EPROM bit is used to invert the product term input into the register. This applies to all inputs including double inputs on the JK and SR registers.

REGISTER SELECTION

The advanced I/O architecture of the iPLD610 allows four different register types along with combinatorial output as illustrated in Figure 4a. The register types include a T, D, JK, or SR Flip-Flop and each Macrocell I/O structure may be independently configured. In addition, all registers have an individual asynchronous RESET control from a dedicated product term derived in the AND array. When this dedicated product term is a logical one, the Macrocell register is immediately cleared to a logical zero independent of the register clock. The RESET function occurs automatically on power-up.

Output Register Configuration

The four different register types shown in Figure 4b–4e are described below.

D- or T-type Flip-Flops

When either a D- or T-type Flip-Flop is configured as part of the I/O structure, all eight of the product terms into the Macrocell are ORed together and fed into the register input.

JK or SR Registers

When either a JK or SR register is configured, the eight product terms are shared among two OR gates (one for the J or S input and the other for the K or R input). The allocation for these product terms for each of the register inputs is optimized by the PLDshell Plus software.

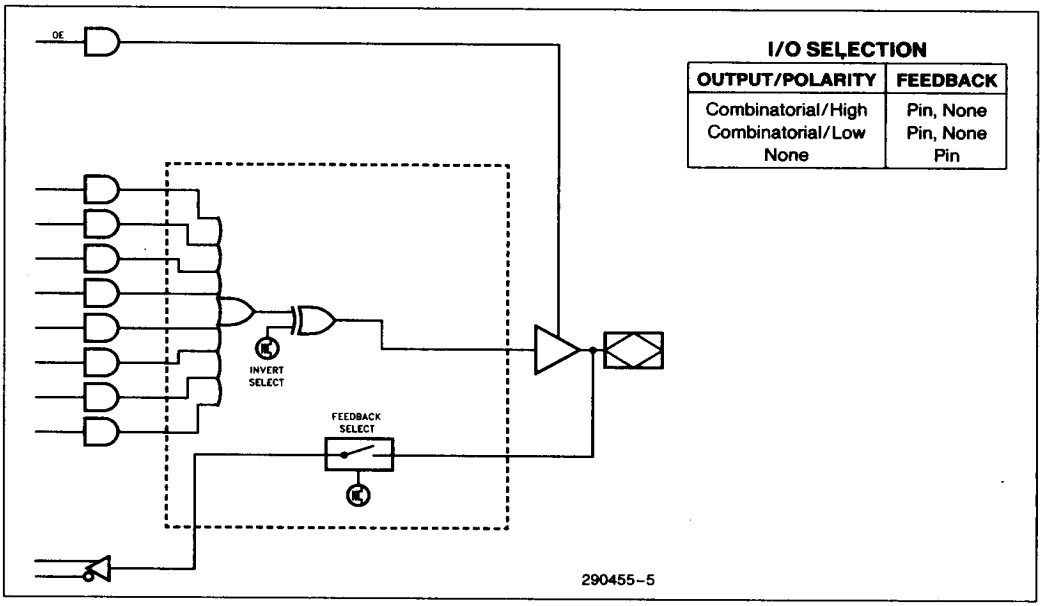
OUTPUT/FEEDBACK

The Output Select Multiplexer allows for either registered, combinatorial or no output.

The Feedback Select Multiplexer EPROM bit enables registered, I/O (using the pin for bidirectional input or just input), or no feedback to the AND array.

The Feedback Select is also important for building equations with more than 8 product terms. The 8-product product term of a Macrocell can be fed back into the AND array and combined with still more signals to create a much larger product term (of more than 8-inputs). If the feedback term is not to be used as an output, the associated Macrocell pin should be left floating (no connect) when assembled onto a circuit board.

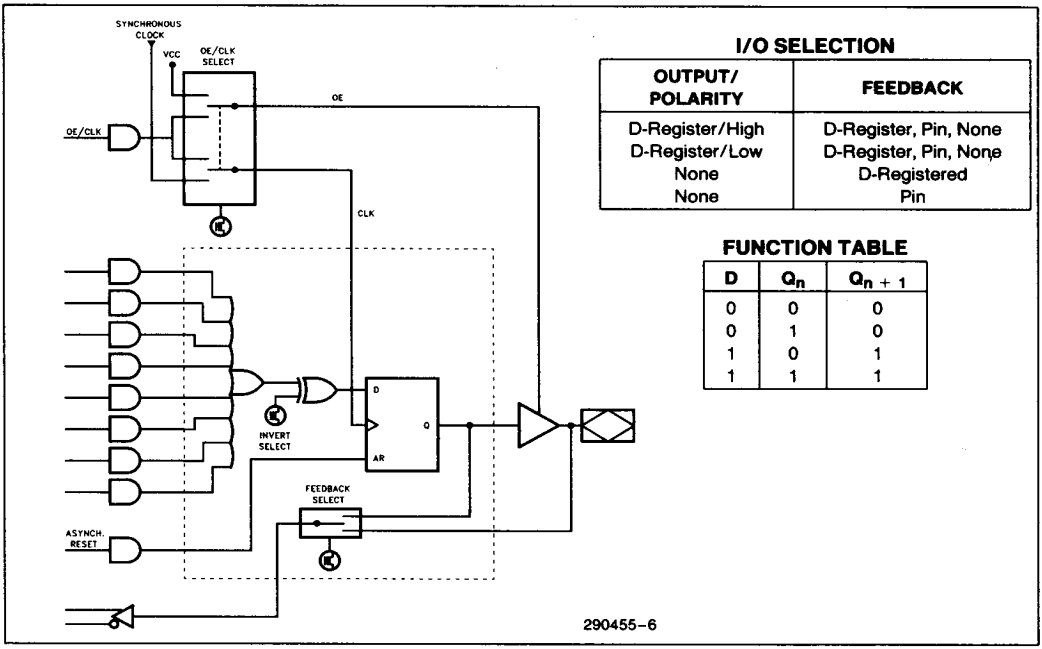
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback through the appropriate multiplexers.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinatorial/High	Pin, None
Combinatorial/Low	Pin, None
None	Pin

Figure 4a. Combinatorial I/O Configuration



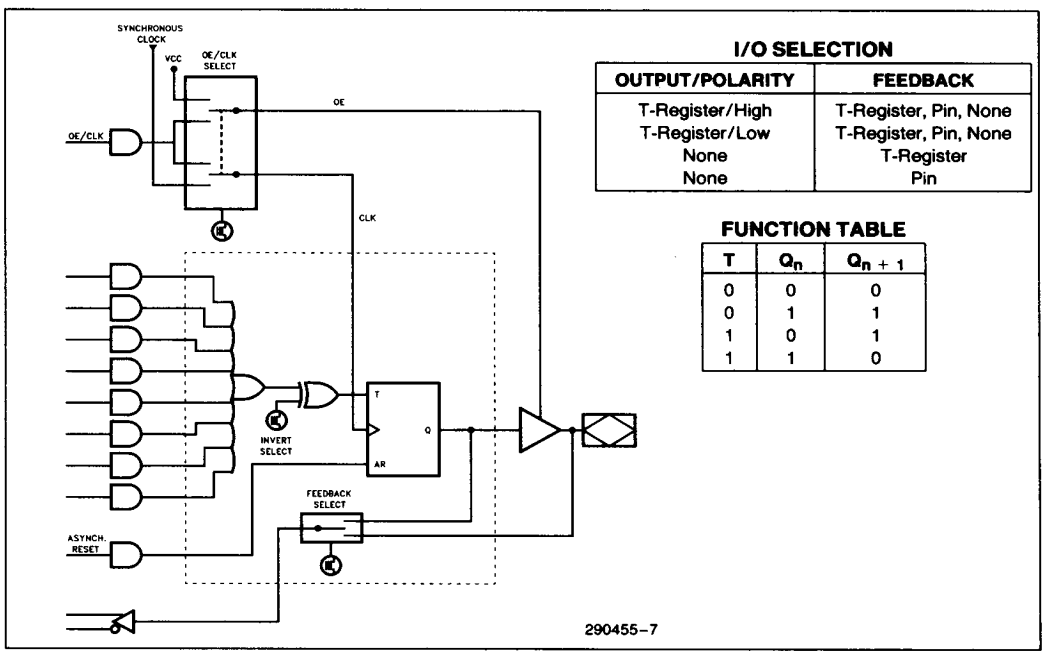
I/O SELECTION

OUTPUT/ POLARITY	FEEDBACK
D-Register/High	D-Register, Pin, None
D-Register/Low	D-Register, Pin, None
None	D-Registered
None	Pin

FUNCTION TABLE

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

Figure 4b. D-Type Flip-Flop Register Configuration



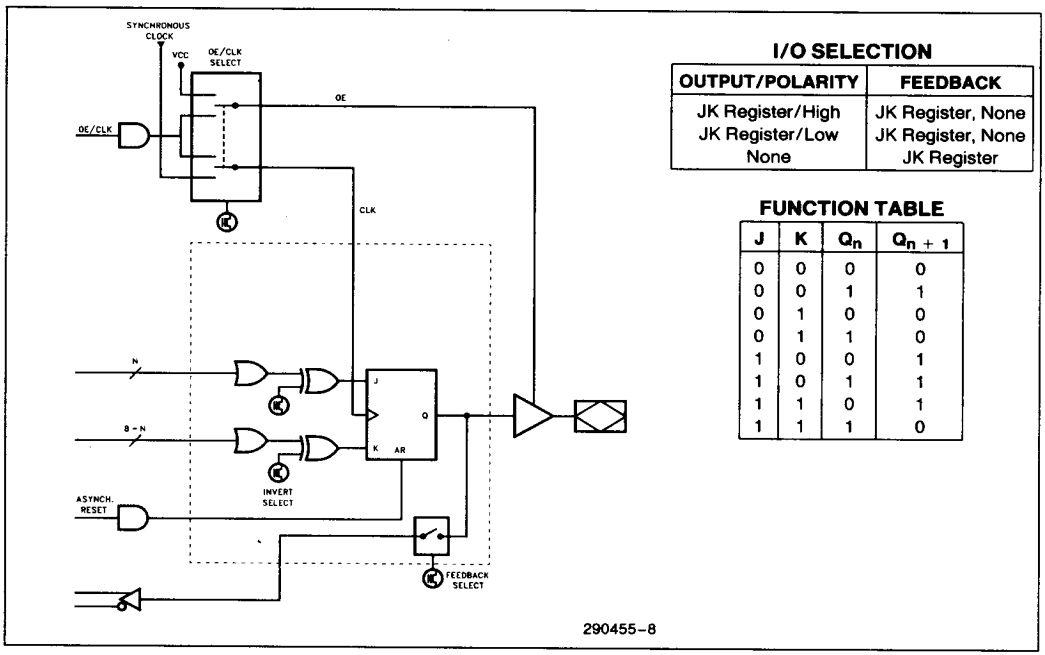
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T-Register/High	T-Register, Pin, None
T-Register/Low	T-Register, Pin, None
None	T-Register
None	Pin

FUNCTION TABLE

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Figure 4c. Toggle Flip-Flop Register Configuration



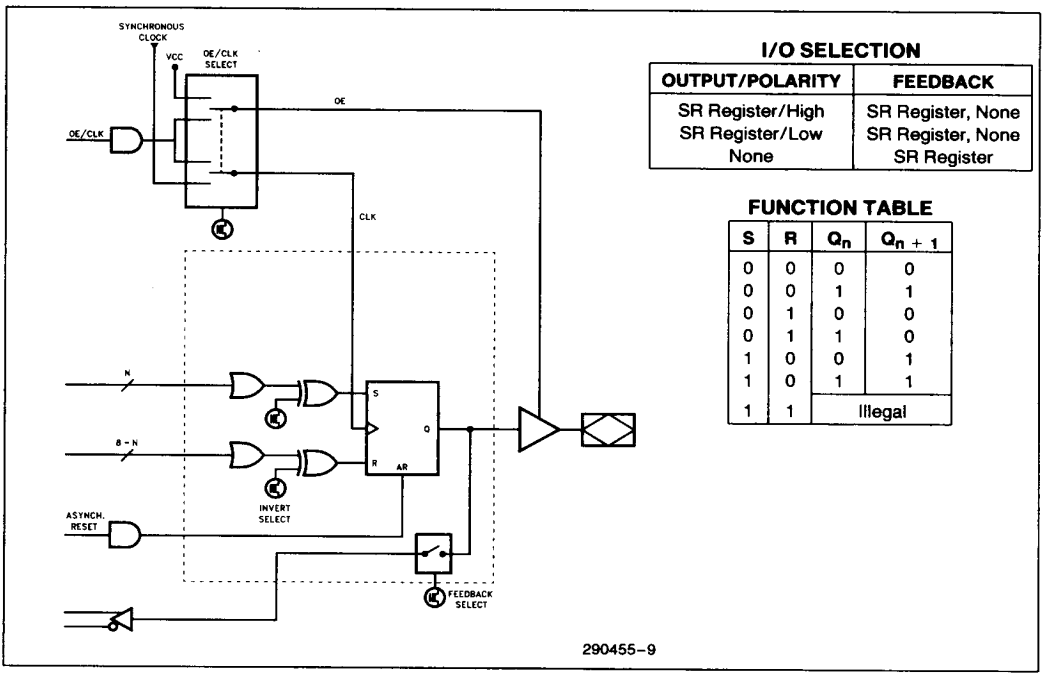
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
JK Register/High	JK Register, None
JK Register/Low	JK Register, None
None	JK Register

FUNCTION TABLE

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Figure 4d. JK Flip-Flop Register Configuration



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/High	SR Register, None
SR Register/Low	SR Register, None
None	SR Register

FUNCTION TABLE

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Illegal	

Figure 4e. SR Flip-Flop Register Configuration

Output Enable (OE)/Clock Selection

Two modes of operation are provided by the OE/CLK Select Multiplexer as a part of each Macrocell. One mode provides for three-state buffering of outputs while in the other mode, the outputs are always enabled. The operation of the OE/CLK Select Multiplexer sets the mode within a given Macrocell. Therefore, the output mode can be selected individually on every output. Figure 5 illustrates the two modes of OE/CLK operation.

MODE 0: THREE-STATE BUFFERING

In Mode 0, the three-state output buffer is controlled by a single product term originating from the AND array. The output is enabled when the product term is a logical true. Conversely, the output appears as high impedance when the product term is a logical false as shown in Table 1. In Mode 0, the Macrocell Flip-Flop is connected to its associated synchronous clock (either CLK1 or CLK2 depending upon the Macrocell's location within the device). Thus, the Macrocell Flip-Flop may be clocked by its respective synchronous clock but its output will not become valid until the output is enabled.

Table 1. Mode 0 Output Selection

Product Term	Output Buffer
FALSE	Three-State
TRUE	Enabled

MODE 1: OUTPUT BUFFER ENABLED

In Mode 1, the Output Buffer is always enabled. In addition, the Macrocell Flip-Flop is connected to the AND array. The Macrocell Flip-Flop may now be triggered from an asynchronous clock signal generated by the AND array logic to the OE/CLK multiplexable term. Mode 1 allows the Macrocell Flip-Flops to be individually clocked from any of the available signals in the AND array. Since both true and complement values appear in the AND array, the Flip-Flop may be clocked by any positive- or negative-going signals at any input pin. Gated clock structures can be created since the Flip-Flop clock is created by a product term.

AUTOMATIC STAND-BY MODE

The iPLD610 contains a programmable bit, the Turbo Bit, that optimizes operation for speed or for power savings. When the Turbo Bit is programmed (TURBO = ON), the device is optimized for maximum speed. When the Turbo Bit is not programmed (TURBO = OFF), the device is optimized for power savings by entering standby mode during periods of inactivity.

Figure 6 shows the device entering standby mode approximately 100 ns after the last input transition. When the next input transition is detected, the device returns to active mode. Wakeup time adds an additional 25 ns to the propagation delay through the device as measured from the first input. No delay will occur if an output is dependent on more than one input and the last of the inputs changes after the device has returned to active mode.

After erasure, the Turbo Bit is unprogrammed (OFF); automatic standby mode is enabled. When the Turbo Bit is programmed (ON), the device never enters standby mode.

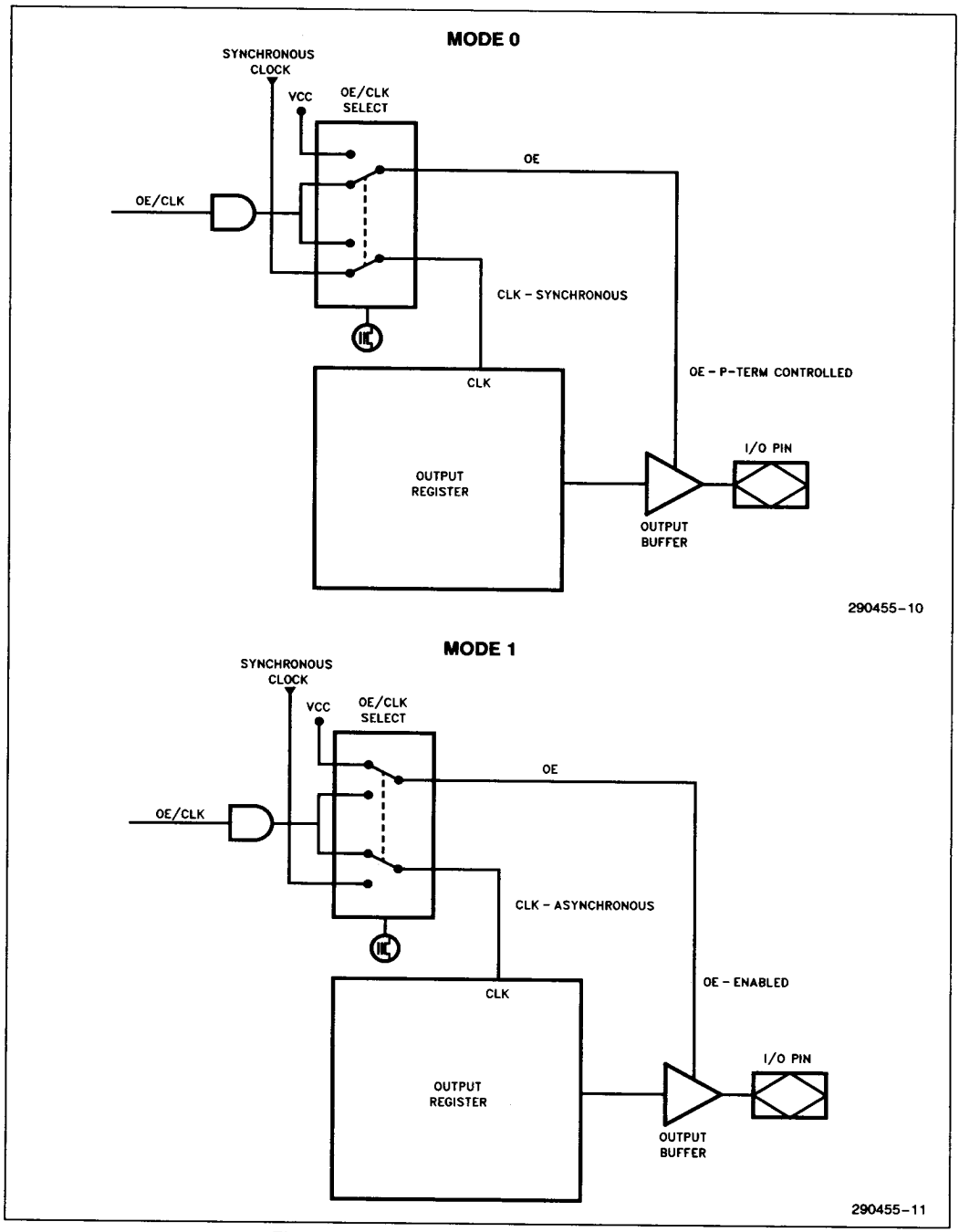


Figure 5. Output Enable/Clock Configuration

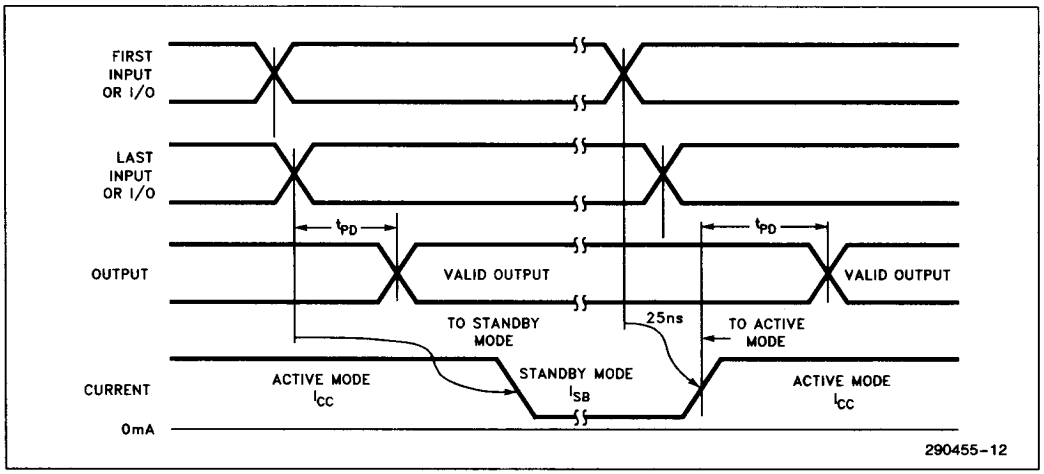


Figure 6. iPLD610 Standby and Active Mode Transitions

Erased-State Configuration

Prior to programming, the I/O structure is configured for combinatorial active low output with input (pin) feedback.

PROGRAMMING CHARACTERISTICS

Initially, all the EPROM control bits of the iPLD610 are connected (in the "1" state). Each of the connected control bits are selectively disconnected by programming the EPROM cells into their "0" state. Programming voltage and waveform specifications are available by request from Intel to support programming of the iPLD610.

Intelligent Programming Algorithm

The iPLD610 supports the Intelligent Programming Algorithm which rapidly programs Intel PLDs using an efficient and reliable method. This method ensures reliability as the incremental program margin of each bit is continually monitored to determine when the bit has been successfully programmed.

FUNCTIONAL TESTING

Since the logical operation of the iPLD610 is controlled by EPROM elements, the device is completely testable. Each programmable EPROM bit controlling the internal logic is tested using application-independent test program patterns. After testing, the devices are erased before shipment to customers. No post-programming tests of the EPROM array are required.

The testability and reliability of EPROM-based programmable logic devices is an important feature over similar devices based on fuse technology. Fuse-based programmable logic devices require a user to perform post-programming tests to insure proper programming. These tests must be done at the device level because of the cummulative error effect. For example, a board containing ten devices each possessing a 2% device fallout translates into an 18% fallout at the board level (it should be noted that programming fallout of fuse-based programmable logic devices is typically 2% or higher).

DESIGN RECOMMENDATIONS

For proper operation, it is recommended that all input and output pins be constrained to the voltage range GND $<$ (V_{IN} or V_{OUT}) $<$ V_{CC}. Unused inputs and I/Os should be tied to V_{CC} or GND to minimize device power consumption. Reserved pins (as indicated in the logic compiler REPORT file) should be left floating (no connect) so that the pin can attain the appropriate logic level. A power supply decoupling capacitor of at least 0.2 μF must be connected directly between V_{CC} and GND pins of the device.

As with all CMOS devices, ESD handling procedures should be used with the iPLD610 to prevent damage to the device during programming, assembly, and test.

DESIGN SECURITY

A single EPROM bit provides a programmable design security feature that controls the access to the data programmed into the device. If this bit is set, a proprietary design within the device cannot be copied. This EPROM security bit enables a higher degree of design security than fused-based devices since programmed data within EPROM cells is invisible even to microscopic evaluation. The EPROM security bit, along with all the other EPROM control bits, will be reset by erasing the device.

LATCH-UP IMMUNITY

All of the input, I/O, and clock pins of the iPLD610 have been designed to resist latch-up which is inherent in inferior CMOS structures. The iPLD610 is designed with Intel's proprietary CMOS II-E EPROM process. Thus, each of the pins will not experience latch-up with currents up to ±100 mA and voltages ranging from $-1V$ to $(V_{CC} + 1V)$. Furthermore, the programming pin is designed to resist latch-up to the 13.5V maximum device limit.

DEVELOPMENT SOFTWARE

Third Party Support

The iPLD610 is supported by third-party logic compilers such as ABEL*, CUPL*, PLDesigner*, Log/IC, etc. Programming support is provided by third-party programmer companies such as Data I/O, Logical Devices, STAG, etc. Please refer to the "Third-Party Support" lists in the *Programmable Logic* handbook for complete information and vendor contacts.

Full logic compilation and functional simulation for the iPLD610 is supported by PLDshell Plus software.

PLDshell Plus

PLDshell Plus design software is Intel's user-friendly design tool for PLD design. PLDshell Plus allows user's to incorporate their prefered text editor, programming software, and additional design tools into a easy-to-use, menued design environment that includes Intel's PLDasm logic compiler and simulation software along with disassembly, conversion, and translation utilities. The PLDasm compiler and simulator software accepts industry-standard PDS source files that express designs as Boolean equations, truth tables, or state machines. On-line help, datasheet briefs, technical notes, and error message information, along with waveform viewing/printing capability make the design task as easy as possible. PLDshell Plus software is available from Intel Literature channels or from your local Intel sales representative.

Tools that support schematic capture and timing simulation for the iPLD610 are available. Please refer to the "Development Tools" section of the Programmable Logic handbook.

*ABEL is a trademark of Data I/O Corp. CUPL is a trademark of Logical Devices, Inc. PLDesigner is a trademark of MINC, Inc. Log/IC is a trademark of ISDATA, Corporation.

ADF PRIMITIVES SUPPORTED

The following ADF primitives are supported by this device:

INP	JOJF
CONF	JONF
COIF	SONF
RONF	SOSF
RORF	TOIF
ROIF	TONF
NORF	TOTF
NOJF	CLKB
NOSF	
NOTF	

ORDERING INFORMATION

f_{CNT1} (MHz)	f_{CNT2} (MHz)	t_{PD} (ns)	Order Code	Package	Operating Range
74	100	10	P PLD610-10	PDIP	Commercial
			N PLD610-10	PLCC	Commercial
			DPLD610-10	*CerDIP	Commercial
50	66	15	P PLD610-15	PDIP	Commercial
			N PLD610-15	PLCC	Commercial
			DPLD610-15	*CerDIP	Commercial
			TDPLD610-15	*CerDIP	Industrial
			TNPLD610-15	PLCC	Industrial
40	40	25	P PLD610-25	PDIP	Commercial
			N PLD610-25	PLCC	Commercial
			DPLD610-25	*CerDIP	Commercial

*Windowed CerDIP package allows UV erase.

ABSOLUTE MAXIMUM RATINGS*

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage(1)	−2.0	7.0	V
V_{PP}	Programming Supply Voltage(1)	−2.0	13.5	V
V_I	DC Input Voltage(1)(2)	−0.5	V_{CC} + 0.5	V
t_{stg}	Storage Temperature	−65	+150	°C
t_{amb}	Ambient Temperature(3)	−10	+85	°C

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

NOTES:
1. Voltages with respect to ground.
2. Minimum DC input is −0.5V. During transitions, the inputs may undershoot to −2.0V or overshoot to +7.0V for periods less than 20 ns under no load conditions.
3. Under bias. Extended temperature versions are also available.

RECOMMENDED OPERATING CONDITIONS

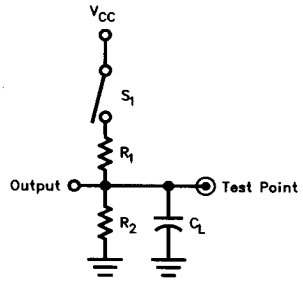
Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.75	5.25	V
V_{IN}	Input Voltage	0	V_{CC}	V
V_O	Output Voltage	0	V_{CC}	V
T_A	Operating Temperature	0	+70	°C
t_R	Input Rise Time		500	ns
t_F	Input Fall Time		500	ns

D.C. CHARACTERISTICS T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IH}(4)	HIGH Level Input Voltage	2.0		V_{CC} + 0.3	V	
V_{IL}(4)	LOW Level Input Voltage	−0.3		0.8	V	
V_{OH}	HIGH Level Output Voltage	2.4			V	I_O = −4.0 mA DC, V_{CC} = Min.
V_{OL}(5)	LOW Level Output Voltage			0.45	V	I_O = 12.0 mA DC, V_{CC} = Min.
I_I	Input Leakage Current	−10		10	µA	V_{CC} = Max., GND < V_{IN} < V_{CC}
I_{OZ}	Output Leakage Current	−10		10	µA	V_{CC} = Max., GND < V_{OUT} < V_{CC}
I_{SC}(6)	Output Short Circuit Current	−30		−120	mA	V_{CC} = Max., V_{OUT} = 0.5V
I_{SB}(7)	Standby Current		20	150	µA	V_{CC} = Max., V_{IN} = V_{CC} or GND, Standby Mode
I_{CC}	Power Supply Current (See I_{CC} vs. Freq. Graph)		3	8	mA	V_{CC} = Max, V_{IN} = V_{CC} or GND, No Load, f_{IN} = 1 MHz, Device Prog. as 16-Bit Counter, Turbo = Off
			65	105	mA	Turbo = On, f_{IN} = 1 MHz
I_{CCI}	Industrial Temperature Power Supply Current			150	mA	Turbo = On, f_{IN} = 1 MHz

NOTES:
4. Absolute values with respect to device GND; all over and undershoots due to system or tester noise are included.
5. Maximum DC I_{OL} for the device is 64 mA for CLK1 group I/O. 1–I/O.8 and 64 mA for CLK2 group I/O.9–I/O16.
6. Not more than 1 output should be tested at a time. Duration of that test must not exceed 1 second.
7. In Non-Turbo Mode (TURBO = OFF), device enters standby mode approximately 75 ns after the last input transition. I_{SB} is measured with the window covered (CerDIP).

SWITCHING TEST CIRCUIT



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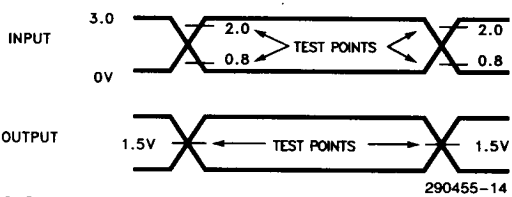
Specification	S_1	C_L	Commercial		Measured Output Value
			R_1	R_2	
t_{PD}	Closed	30 pF	200Ω	330Ω	1.5V
t_{PZX}	Z → H: Open Z → L: Closed				1.5V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} − 0.5V L → Z: V_{OL} + 0.5V

A.C. TESTING INPUT, OUTPUT WAVEFORM



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A.C. Testing: Inputs are Driven at 3.0V for a Logic "1" and 0V for a Logic "0". Timing Measurements are made at 2.0V for a Logic "1" and 0.8V for a Logic "0" on inputs. Outputs are measured at a 1.5V point. Device input rise and fall times are less than 3 ns.

CAPACITANCE (T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%)(8)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
C_{IN}	Input Capacitance		5	8	pF	V_{IN} = 0V, f = 1.0 MHz
C_{IO}	I/OCapacitance		6	8	pF	V_{OUT} = 0V, f = 1.0 MHz
C_{CLK}	CLK Capacitance		8	10	pF	V_{IN} = 0V, f = 1.0 MHz
C_{VPP}	V_{PP} Pin Capacitance		10	12	pF	V_{PP} on CLK2, f = 1.0 MHz

NOTE:
8. These values are evaluated during initial characterization and whenever design modifications occur that may affect capacitance.

COMBINATORIAL MODE A.C. CHARACTERISTICS

(T_A = 0°C to +70°C, V_{CC} = 5.0V ±5%)[9]

Symbol	Parameter	iPLD610-10			iPLD610-15			iPLD610-25			Non-Turbo[10] Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
t_{PD1}[11]	Input to Output Valid			10			15			25	+25	ns
t_{PD2}[11]	I/O to Output Valid			10			15			25	+25	ns
t_{PZX}[12]	Input or I/O to Output Enable			15			18			25	+25	ns
t_{PXZ}[12]	Input or I/O to Output Disable			13			18			25	+25	ns
t_{CLR}	Input or I/O to Asynch. Reset			13			18			25	+25	ns

NOTES:
9. Typical values are at T_A = 25°C, V_{CC} = 5V, Active Mode.
10. If device is operated in Non-Turbo Mode (TURBO = OFF), and the device is inactive for approx. 75 ns, increase time by amount shown.
11. Measured with eight outputs switching. See t_{PD} vs. Number of Outputs Switching graph.
12. t_{PZX} and t_{PXZ} are measured at ±0.5V from steady state voltage as driven by spec. output load.
13. Measured with device configured as a 16-bit counter.

REGISTER MODE—SYNCHRONOUS CLOCK A.C. CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%[9]

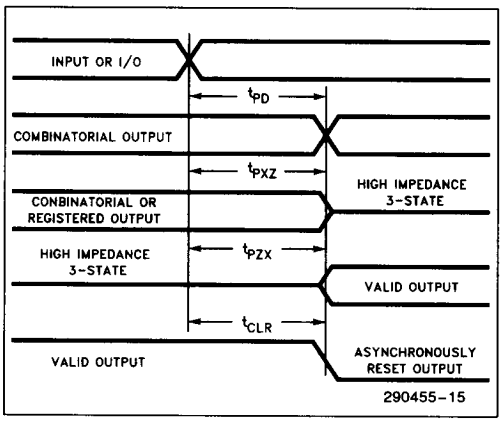
Symbol	Parameter	iPLD610-10			iPLD610-15			iPLD610-25			Non-Turbo[10] Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{CNT1}[13]	Max. Counter Frequency $1/(t_{SU} + t_{CO1})$—Ext. Feedback	74	85		50	66		40	50			MHz
f_{CNT2}[13]	Max. Counter Frequency $1/(t_{CNT})$—Internal Feedback	100	111		66	75		40	66			MHz
f_{MAX}	Max. Frequecy (Pipelined) $1/(t_{CP})$—No Feedback	111	120		83.3	100		66	80			MHz
t_{SU}	Input or I/O Setup Time to CLK	7			12			15			+25	ns
t_H	Input or I/O Hold Time from CLK	0			0			0				ns
t_{CO1}[13]	CLK High to Output Valid			6.5			8			10		ns
t_{CO2}	CLK High to Output Valid Fed through Comb. Macrocell			14			20			30	+25	ns
t_{CNT}[13]	Macrocell Output Feedback to Macrocell Input—Internal Path			10			15			25	+25	ns
t_{CL}	CLK Low Time	4			5			6				ns
t_{CH}	CLK High Time	4			5			6				ns
t_{CP}	CLK Period	9			12			15				ns

REGISTER MODE—ASYNCHRONOUS CLOCK A.C. CHARACTERISTICS

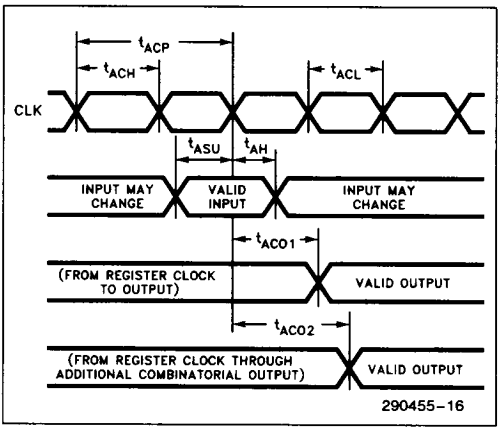
T_A = 0°C to 70°C, V_{CC} = 5.0V ±5%(9)

Symbol	Parameter	iPLD610-10			iPLD610-15			iPLD610-25			Non-Turbo(10) Mode	Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{ACNT1}(13)	Max. Counter Frequency $1/(t_{ASU} + t_{ACO1})$—Ext. Feedback	71.4	80		50	66		33.3	40			MHz
f_{ACNT2}(13)	Max. Counter Frequency $1/(t_{ACNT})$—Internal Feedback	100	111		66	75		40	50			MHz
f_{AMAX}	Max. Frequency (Pipelined) $1/(t_{ACP})$—No Feedback	100	111		66	75		50	66			MHz
t_{ASU}	Input or I/O Setup Time to Asynch. CLK	2			4			5			+25	ns
t_{AH}	Input or I/O Hold Time from Asynch. CLK	3			6			8				ns
t_{ACO1}(13)	Asynch. CLK High to Output Valid			12			16			25	+25	ns
t_{ACO2}	Asynch. CLK High to Output Valid Fed through Comb. Macrocell			20			30			45	+25	ns
t_{ACNT}	Macrocell Output Feedback to Macrocell Input—Internal Path			10			15			25	+25	ns
t_{ACL}	Asynch. CLK Low Time	4			6			7				ns
t_{ACH}	Asynch. CLK High Time	4			6			7				ns
t_{ACP}	Asynch. CLK Period	10			15			20				ns

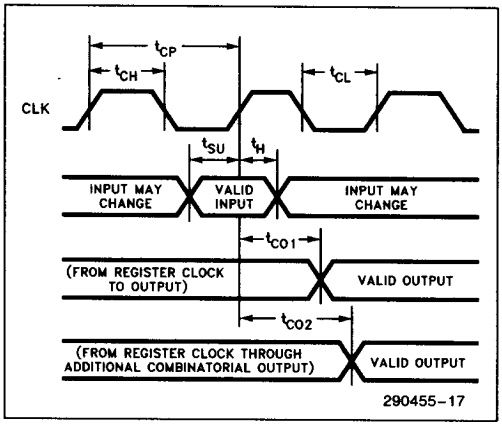
COMBINATORIAL MODE

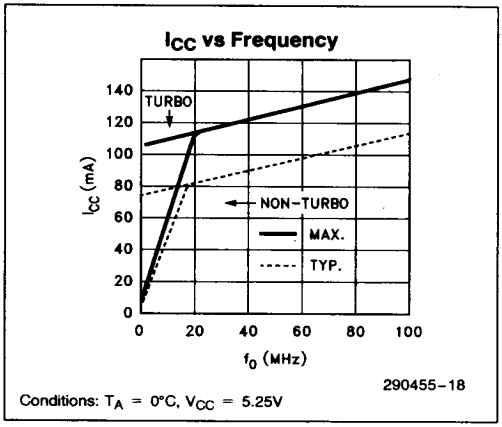


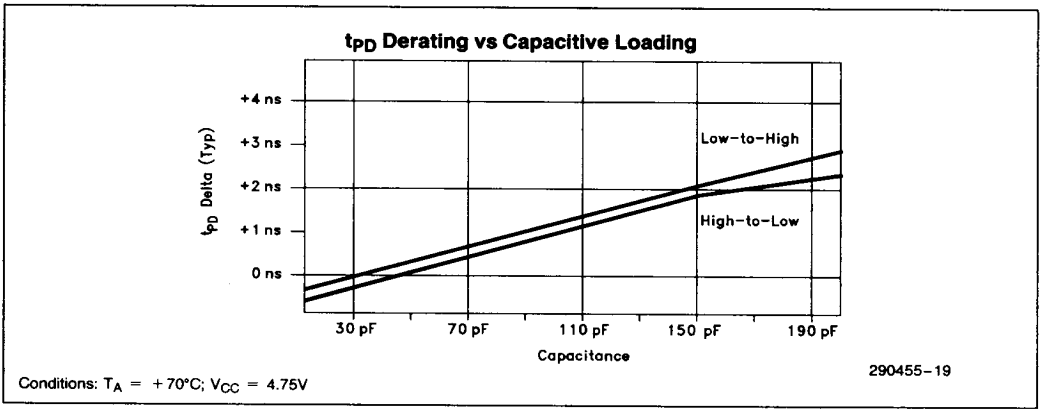
ASYNCHRONOUS REGISTERED MODE



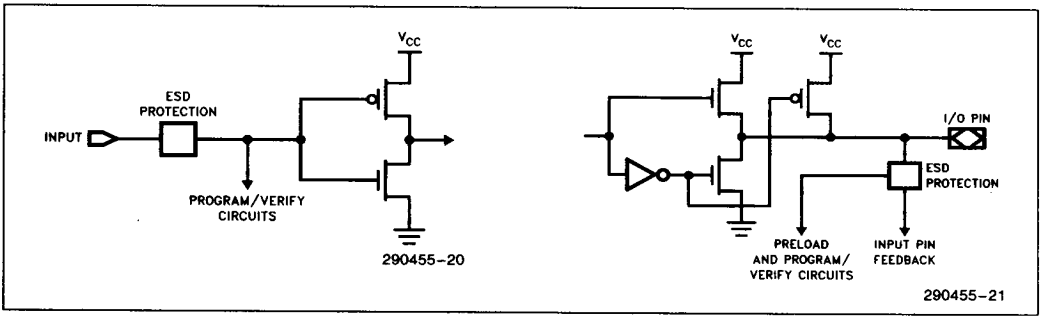
SYNCHRONOUS REGISTERED MODE



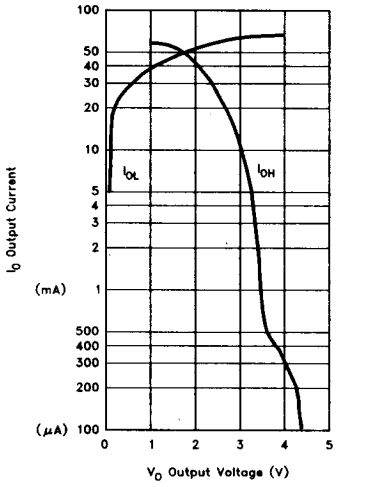




INPUT/OUTPUT EQUIVALENT SCHEMATICS



iPLD610 Output Current in Relation to Voltage



290455-22

CONDITIONS:
T_A = +80°C
V_{CC} = 4.75V

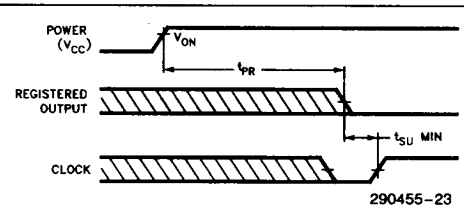
Power-Up Reset

Internal power-up reset circuits ensure that all flip-flops will be reset to a logic 0 after the device has powered up. Because V_{CC} rise can vary significantly from one application to another, V_{CC} rise must be monotonic.

POWER-UP RESET CHARACTERISTICS

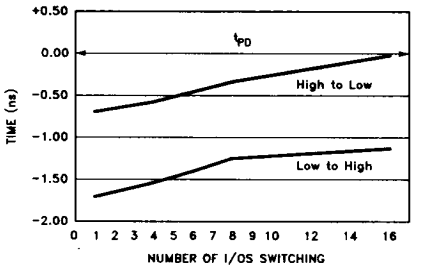
Symbol	Parameter	Value
t_{PR}	Power-Up Reset	1000 ns Max.
V_{ON}	Turn-On Voltage	4.75V

POWER-UP RESET



290455-23

iPLD610 t_{PD} vs No. of Outputs Switching



290455-24

CONDITIONS:
T_A = 70°C, V_{CC} = 4.75V, C_L = 30 pF

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