



## P-Channel 60-V (D-S) MOSFET

### CHARACTERISTICS

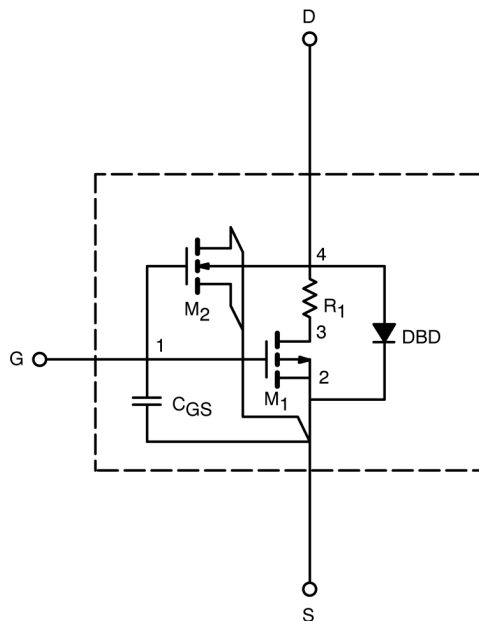
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the  $-55$  to  $125^{\circ}\text{C}$  Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit mode is extracted and optimized over the  $-55$  to  $125^{\circ}\text{C}$  temperature ranges under the pulsed 0-to-10V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### SUBCIRCUIT MODEL SCHEMATIC



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

# SPICE Device Model Si7415DN

Vishay Siliconix



SPECIFICATIONS (T <sub>J</sub> = 25°C UNLESS OTHERWISE NOTED)					
Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
<b>Static</b>					
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = – 250μA	2.1		V
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> < – 5V, V <sub>GS</sub> = – 10V	88		A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = – 10V, I <sub>D</sub> = – 5.7A	0.053	0.054	Ω
		V <sub>GS</sub> = – 4.5V, I <sub>D</sub> = – 4.4A	0.084	0.090	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = – 15V, I <sub>D</sub> = – 5.7A	11	11	S
Diode Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>S</sub> = – 3.2A, V <sub>GS</sub> = 0V	– 0.82	– 0.80	V
<b>Dynamic<sup>b</sup></b>					
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> = – 30V, V <sub>GS</sub> = – 10V, I <sub>D</sub> = – 5.7A	15.4	15	nC
Gate-Source Charge	Q <sub>gs</sub>		4	4	
Gate-Drain Charge	Q <sub>gd</sub>		3.2	3.2	
Turn-On Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = – 30V, R <sub>L</sub> = 30Ω I <sub>D</sub> ≅ – 1A, V <sub>GEN</sub> = – 10V, R <sub>G</sub> = 6Ω	9	12	ns
Rise Time	t <sub>r</sub>		12	12	
Turn-Off Delay Time	t <sub>d(off)</sub>		19	22	
Fall Time	t <sub>f</sub>		32	16	
Source-Drain Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = – 3.2A, di/dt = 100A/μs	31	45	

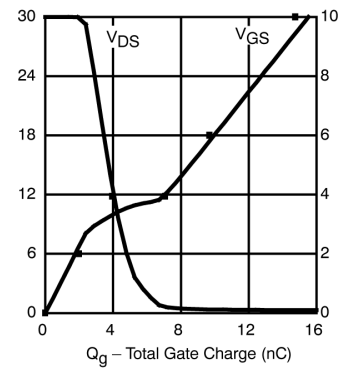
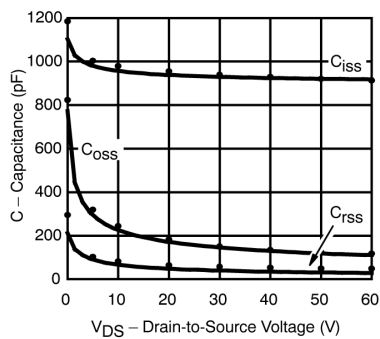
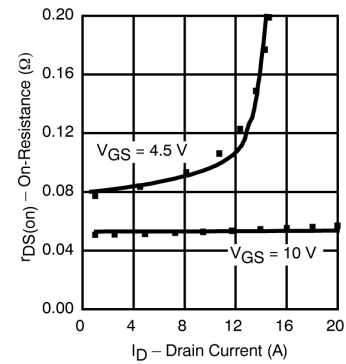
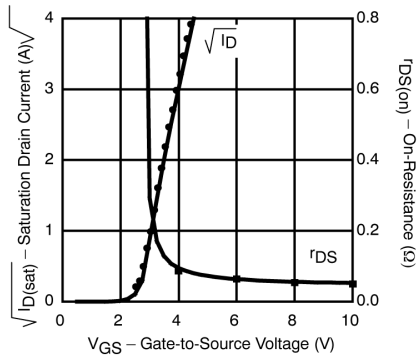
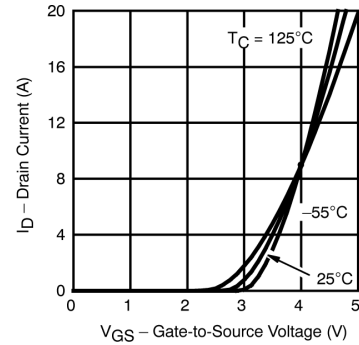
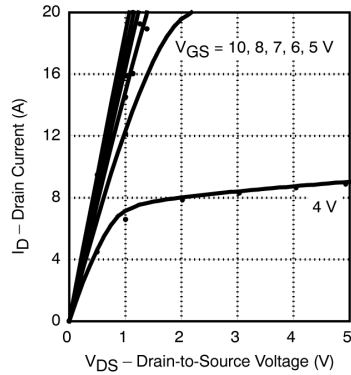
## Notes

a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

b. Guaranteed by design, not subject to production testing.



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J=25^\circ\text{C}$ UNLESS OTHERWISE NOTED)



Note: Dots and squares represent measured data.