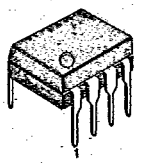
NE555C LINEAR INTEGRATED CIRCUIT

T-51-19

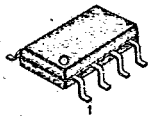
SINGLE TIMER

The NE555 is a highly stable controller capable of producing accurate timing pulses. With monostable operation, the time delay is controlled by one external and one capacitor. With astable operation, the frequency and duty cycle are accurately controlled with two external resistors and one capacitor.

8 DIP



8 SOP



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FEATURES

- **High Current Drive Capability (=200mA)**
- **Adjustable Duty Cycle**
- **Temperature Stability Of 0.005%/°C**
- **Timing From μSec To Hours**
- **Turn Off Time Less Than 2 μsec**

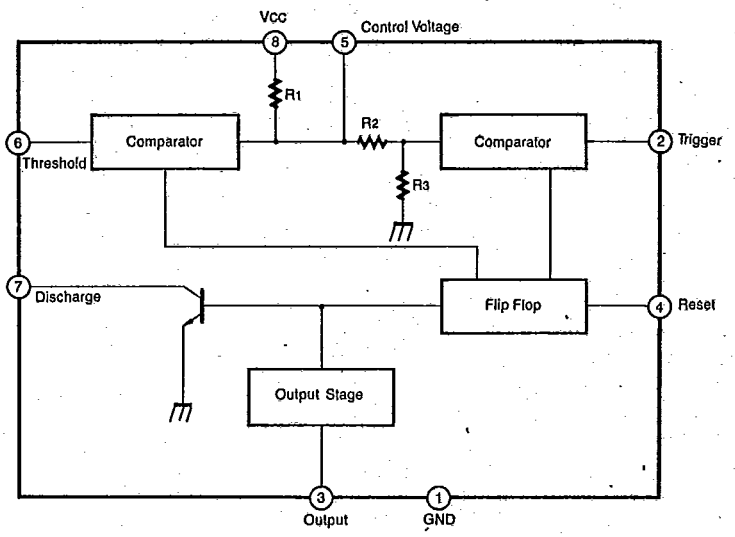
APPLICATIONS

- Precision Timing
- Pulse Generation
- Time Delay Generation
- Sequential Timing

ORDERING INFORMATION

Device	Package	Operating Temperature
NE555CN	8 DIP	0~+70°C
NE555CD	8 SOP	

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Characteristic	Symbol	Value	Unit
Supply Voltage	V_{CC}	16	V
Lead Temperature (soldering 10 sec)	T_{lead}	300	°C
Power Dissipation	P_D	600	mW
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	−65 ~ +150	°C

ELECTRICAL CHARACTERISTICS

(Ta = 25°C, V_{CC} = 5 to 15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.5		16	V
Supply Current *1(low state)	I_{CC}	V_{CC} = 5V, R_L = ∞		2.5	6	mA
		V_{CC} = 15V, R_L = ∞		7.5	15	mA
*Timing Error (Monostable) *2Initial Accurary Drift with Temperature Drift with Supply Voltage	MT_1	R_A = 1KΩ to 100KΩ C = 0.1μF		1.0 50 0.1	3.0 0.5	% ppm/°C %/V
*Timing Error (astable) *2Initial Accurary Drift with Temperature Drift with Supply Voltage	MT_2	R_A, R_B = 1K to 100KΩ C = 0.1μF V_{CC} = 15V		2.25 150 0.3		% ppm/°C %/V
Control Voltage	V_C	V_{CC} = 15V	9.0	10.0	11.0	V
		V_{CC} = 5V	2.6	3.33	4.0	V
Threshold Voltage	V_{TH}	V_{CC} = 15V		10.0		V
		V_{CC} = 5V		3.33		V
*3Threshold Current	I_{TH}			0.1	0.25	μA
Trigger Voltage	V_{TR}	V_{CC} = 5V	1.1	1.67	2.2	V
Trigger Voltage	V_{TR}	V_{CC} = 15V	4.5	5	5.6	V
Trigger Current	I_{TR}	V_T = 0V		0.01	2.0	μA
Reset Voltage	V_{RE}		0.4	0.7	1.0	V
Reset Current	I_{RE}			0.01	0.4	mA

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ELECTRICAL CHARACTERISTICS

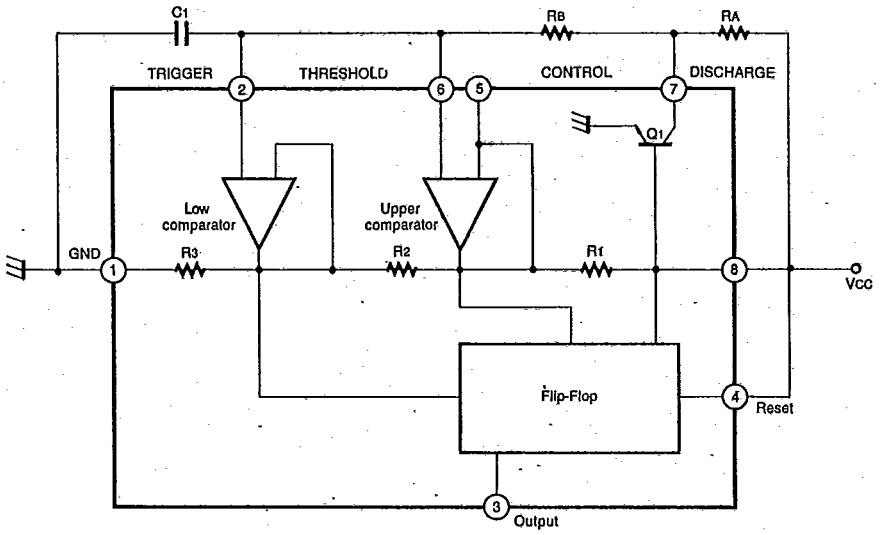
(T_a=25°C, V_{CC}=5~15V, unless otherwise specified)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Voltage (low)	V_{OL}	V_{CC}=15V I_{sink}=10mA I_{sink}=50mA		0.06 0.3	0.25 0.75	V V
		V_{CC}=5V I_{sink}=5mA		0.05	0.35	V
Output Voltage (high)	V_{OH}	V_{CC}=15V I_{source}=200mA I_{source}=100mA	 12.75	12.5 13.3		V V
		V_{CC}=5V I_{source}=100mA	2.75	3.3		V
Rise Time of Output	T_r			100		nsec
Fall Time of Output	T_f			100		nsec
Discharge Leakage Current	I_D			20	100	nA

Notes:

1. Supply current when output is high is typically 1mA less at V_{CC}=5V.
2. Tested at V_{CC}=5.0V and V_{CC}=15V
3. This will determine the maximum value of R_A+R_B for 15V operation, the max total R=20MΩ, and for 5V operation the max total R=6.7MΩ.

APPLICATION CIRCUIT (Astable Operation)



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APPLICATION NOTE

The application circuit shows astable mode.
Pin 6 (threshold) is tied to Pin 2 (trigger) and Pin 4 (reset) is tied to V_{CC} (Pin 8).
The external capacitor C_1 of Pin 6 and Pin 2 charges through R_A, R_B and discharges through R_B only.
In the internal circuit of the NE555 one input of the upper comparator is the 2/3 V_{CC} ($*R_1 = R_2 = R_3$), another input if it is connected Pin 6.
As soon as charging C_1 is higher than 2/3 V_{CC}, discharge transistor Q_1 turns on and C_1 discharges to collector of transistor Q_1.
Therefore, the flip-flop circuit is reset and output is low.
One input of lower comparator is the 1/3 V_{CC}, discharge transistor Q_1 turn off and C_1 charges through R_A and R_B.
Therefore, the flip-flop circuit is set and output is high.
So to say, when C_1 charges through R_A and R_B output is high and when C_1 discharges through R_b output is low
The charge time (output is high) T_1 is 0.693 (R_A+R_B) C_1 and the discharge time (output is low) T_2 is 0.693 $(R_B C_1)$.

$$\left(\ln \frac{V_{CC}-1/3V_{CC}}{V_{CC}-2/3V_{CC}} = 0.693\right)$$

Thus the total period time T is given by
$T=T_1+T_2=0.693\,(R_A+2R_B).C_1$.
Then the frequency of astable mode is given by

$$f=\frac{1}{T}=\frac{1.44}{(R_A+2R_B)C_1}$$

The duty cycle is given by

$$D.C=\frac{T_2}{T}=\frac{R_B}{R_A+2R_B}$$

If you make use of the NE556 you can make two astable modes.
If you want another application note, request information on our timer IC application circuit designer.