CS5171DEMO/D

Demonstration Note for CS5171/3 3.3 V to 5.0 V/ 400 mA Boost Regulator

ON Semiconductor™

DEMONSTRATION NOTE

Description

The CS5171/3 demo board is configured as a compact, low profile and efficient boost regulator. This board allows initial evaluation of the performance of the CS5171 (260 kHz) or the CS5173 (520 kHz) 1.5 A boost regulator IC. The demonstration circuit converts 3.3 V to 5.0 V with a maximum load current of 400 mA.

The high integration level of the CS5171 minimizes the external component count to 10. A high–frequency oscillator built into CS5171 allows the use of all surface mount components, greatly reducing the size and height of the circuit. Using a TTL–compatible pulse train, one can increase and synchronize the switching frequency to almost twice the built–in frequency.

This regulator can also be put into a sleep mode. The 5.0 V output is disabled and the circuit consumes minimum current. The inherent protection features of the CS5171 ensure that the power supply can survive power–on and heavy load conditions.

Features

- Current Mode Control with Pulse–By–Pulse Current Limit
- Easy External Sync Function
- Power Down Mode Consuming Maximum 50 μA
- Small Board Space Requiring Only 0.7×0.7 in.^{2}
- Low Profile with Component Height Less Than 0.1 in.
- High Energy Transfer Efficiency
- Excellent Line and Load Regulation
- Fast Transient Response
- Minimum Output Voltage Ripple
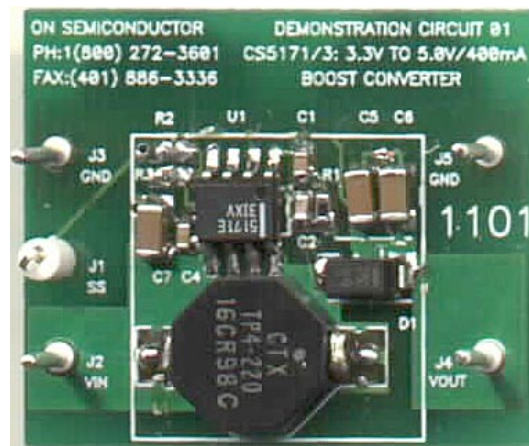- High Reliability with All Ceramic Capacitors

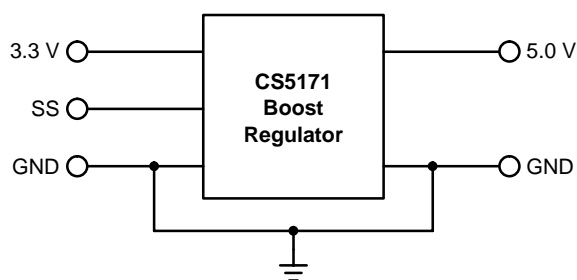**Figure 1. CS5171 Demonstration Board**

CS5171DEMO/D

Figure 2. Application Diagram

ABSOLUTE MAXIMUM RATINGS

Pin Name	Maximum Voltage	Maximum Current
3.3 V	6.3 V	3.0 A
SS	40 V	1.0 mA
5.0 V	6.3 V	400 mA

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{IN} = 3.3 V, 60 mA $\leq I_{OUT} \leq$ 400 mA; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Voltage	I_{OUT} = 60 mA I_{OUT} = 400 mA	– –	4.966 4.963	– –	V V
Frequency	–	235	260	290	kHz
Duty Cycle	I_{OUT} = 60 mA I_{OUT} = 400 mA	– –	34 48	– –	% %
Efficiency	I_{OUT} = 60 mA I_{OUT} = 400 mA	– –	82 78	– –	% %
Line Regulation	3.0 V < V_{IN} < 4.0 V	–	1.5	–	mV/V
Shutdown Current	V_C < 0.8 V, V_{SS} = 0 V	–	12	50	μA
Startup Time	From V_{CC} = 1.0 V to I_{OUT} = 400 mA	–	5.6	–	ms
Transient Response Time	From I_{OUT} = 200 mA to I_{OUT} = 400 mA, V_O at Steady State	–	85	–	μs
Sync Range	–	280	–	500	kHz
Sync Pulse Transition Threshold	Rise Time = 20 ns	2.5	–	–	V
SS Bias Current	SS = 0 V SS = 3.3 V	– –	–3.0 3.0	–10 10	μA μA
Shutdown Threshold	–	0.6	1.3	2.0	V
Shutdown Delay	SS = 5.0 V to 0 V, V_C < 0.8 V	–	80	300	μs

PIN DESCRIPTION

| Pin Name	Description
3.3 V	Input voltage pin. Connect this pin to a 3.3 V supply. The maximum voltage rating on this pin is determined by the rating of the input capacitor.
5.0 V	Output voltage pin. The maximum current drawn from this pin is 400 mA, limited by the inductor. The maximum voltage rating on this pin is determined by the rating of the output capacitors.
SS	This is a multi–function pin. Apply a TTL pulse train to this pin to sync the switching frequency up to almost twice the inherent frequency. Pull this pin below 1.2 V to disable the output voltage and leave the board in sleep mode.
GND	Ground pin. There are two ground pins for input and output.
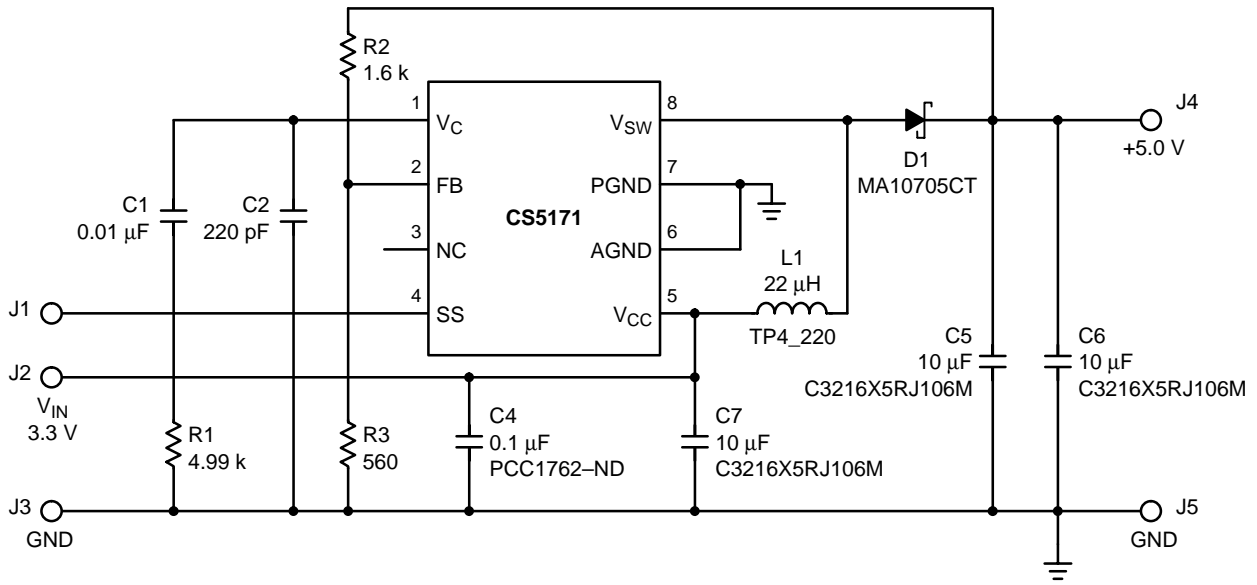
Figure 3. Schematic

OPERATION GUIDELINES

- The +3.3 V (J2) and GND (J3) input terminals are located on the left side of the board. Simple alligator or banana clip connections are needed to power up the demo board.

- The SS input terminal (J1) is also located on the left side of the board. Similar connections are required to input this TTL–compatible logic signal.

- The +5.0 V (J4) and GND (J5) output terminals are located on the right side of the board. Connect the load between these two terminals. Never short these terminals since the IC has no way to protect against a short in a boost regulator. Place the probe right on the anode of D1 to examine the output voltage.

- To examine start–up, lift the SS pin above shutdown threshold. This signal will turn on the IC and enable the output. The duty cycle and switching frequency are best observed at the V_{SW} pin.

Figure 4. Efficiency vs. Current

THEORY OF OPERATION

Current Mode Control

The CS5171 incorporates a current mode control scheme, in which the PWM ramp signal is derived from the power switch current. This ramp signal is compared to the output of the error amplifier to control the on–time of the power switch. The oscillator is only used here as a fixed frequency clock to ensure a constant operational frequency. At the beginning of each switching cycle, the clock signal turns on the internal power switch and the V_{SW} pin voltage is equal to the saturation voltage of the switch. Since the V_{SW} pin voltage is applied across the inductor, its current increases linearly. The current is sensed through an emitter resistor within the IC. When the current signal reaches the error amplifier output at the V_C pin, the power switch turns off and inductor current starts to fall. The catch diode D1 is forward–biased to conduct inductor current. The V_{SW} pin voltage is now equal to the output voltage plus the diode forward voltage. Upon the arrival of the next switching cycle, the power switch turns on again to repeat the same operation.

This control scheme features several advantages over the conventional voltage mode controller. First, derived directly from the inductor, the ramp signal responds immediately to variations in line voltage, reducing the response time caused by the output filter and error amplifier delay found in voltage mode control. The second benefit comes from inherent pulse–by–pulse current limit by merely clamping the peak switching current. Finally, since current mode commands an output current rather than voltage, the filter offers only a single pole to the feedback loop. This allows both simple compensation and high bandwidth.

Without discrediting its apparent merits, current mode control also comes with its own peculiar problems, namely, subharmonic oscillation at duty cycles over 50%. The
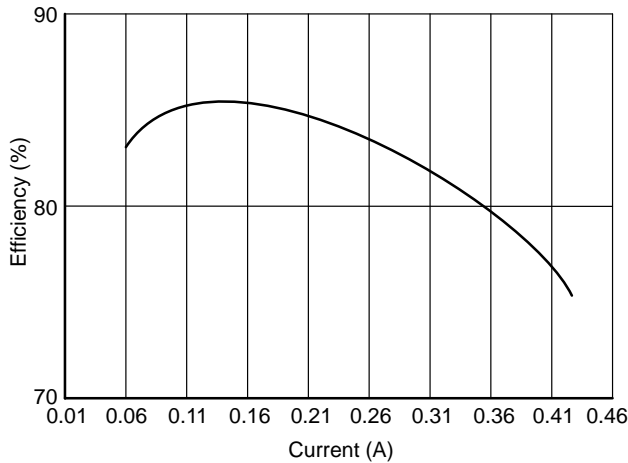
CS5171 solves this problem with internal slope compensation, which adds an artificial ramp to the current signal. A proper slope is selected to improve circuit stability without sacrificing the advantages of current mode control.

Short Circuit Condition

When a short circuit condition occurs in a boost circuit, the IC runs at minimum duty cycle and the diode conducts for most of the switching period. Since there is no way to balance the flux of the inductor the inductor current will eventually saturate, causing excessive current to be drawn from the input power supply. Since control ICs do not have the means to limit output current, an external current limit circuit, such as a fuse or relay, should be added to protect the IC, inductor and catch diode.

Start Up

The boost regulator experiences start up transition on either powering up the V_{CC} pin or pulling up the SS pin. The difference is that the former generates a high initial current, which quickly charges the output capacitors to the input voltage. The start up waveform shown in Figure 5 was recorded after the 3.3 V input supply was turned on. These waveforms clearly show the various phases in this power up transition.
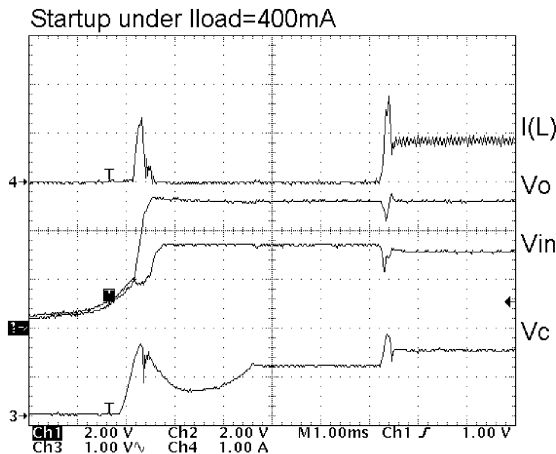
Figure 5. Startup Waveforms

When the V_{CC} voltage is below the minimum supply voltage, the V_{SW} pin is in high impedance. Therefore, current conducts directly from the input power source to the output through the inductor and diode. Once V_{CC} reaches approximately 1.5 V, the internal power switch briefly turns on. This is a part of the CS5171's normal operation. The turn–on of the power switch accounts for the initial current swing.

When the V_C pin voltage rises above the threshold, the internal power switch starts to switch and a voltage pulse can be seen at the V_{SW} pin. Detecting a low output voltage at the FB pin, the built–in frequency shift feature reduces the

switching frequency to a fraction of its nominal value, reducing the minimum duty cycle, which is otherwise limited by the minimum on time of the switch. The peak current during this phase is clamped by the internal current limit.

When the FB pin voltage rises above 0.4 V, the frequency increases to its nominal value, and the peak current begins to decrease as the output approaches the regulation voltage. The overshoot of the output voltage is prevented by the active pull–on, by which the sink current of the error amplifier is increased once an overvoltage condition is detected. The overvoltage condition is defined as when the FB pin voltage is 50 mV greater than the reference voltage.

Sync and Shutdown

A TTL–compatible logic input at the S/S pin is capable of synchronizing the CS5171 up to 500 kHz. As shown in Figure 6, a rising edge on the SS pin voltage turns on the power switch, and also resets the oscillator. The duty cycle of the sync pulse can vary from 10% to 90% without altering the function. A logic low sustained for typically 80 μs at the SS pin shuts down the IC and reduces the supply current to about 30 μA. When the pin is not used, leave it floating.
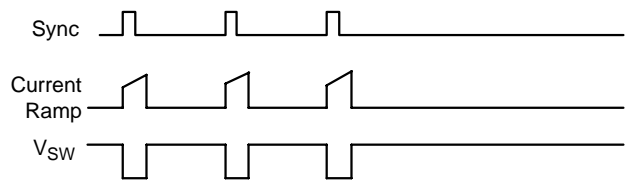

Figure 6. Timing Diagram of Sync and Shutdown

DESIGN GUIDELINES

Design Specifications

V_{IN} = 3.3 V ± 10%
V_O = 5.0 V ± 5.0%
Maximum Load = 400 mA
Switching Frequency = 260 kHz

Design Output Filter

The resonant frequency of the output filter should be less than $f_{SW}/50$, in order to effectively filter out the switching frequency. The inductor value is selected to keep the current ripple low according to the equation in Table 1. For the purposes of this demonstration board, we will select the maximum ripple current to be 200 mA. Therefore, we choose an inductor that is 22 μH. Allowing a 5% tolerance on the output voltage, the maximum output voltage ripple is 25 mV. Using the equation for output voltage ripple and neglecting the ESR term, the capacitor must be at least 10 μF. Select the output capacitor to be 20 μF.

The resonant frequency is equal to:

$$f_O = \frac{1}{2\pi \sqrt{(L)(C)}} = 7.0 \text{ kHz}$$

Table 1. Formulas for Calculation of Electrical Parameters in a Boost Regulator (Assuming Continuous Conduction Mode)

Parameter	Symbol	Formula
Duty Cycle	D	$\dfrac{V_O + V_F - V_{IN}}{V_O + V_F - V_{SAT}}$
Input Current	I_{IN}	$\dfrac{I_{LOAD}}{1-D}$
Average Inductor Current	$I_{L(AVE)}$	I_{IN}
Inductor Current Ripple	$I_{L(RP)}$	$\dfrac{V_{IN} - V_{SAT}}{L}\dfrac{D}{f_{SW}}$
Peak Inductor Current	$I_{L(PK)}$	$\dfrac{I_{LOAD(MAX)}}{1 - D_{MAX}} + \dfrac{I_{L(RP)}}{2}$
Average Switch Current	$I_{SW(AVE)}$	$\dfrac{I_{LOAD} \times D}{1-D}$
Peak Switch Current	$I_{SW(PK)}$	$I_{L(PK)}$
Open Switch Voltage	V_{SW}	$V_O + V_F$
Average Diode Current	$I_{D(AVE)}$	I_{LOAD}
Peak Diode Current	$I_{D(PK)}$	$I_{L(PK)}$
Diode Reverse Voltage	V_R	$V_O - V_{SAT}$
Output Ripple Voltage	$V_{O(RP)}$	$I_{LOAD}\left(\dfrac{V_O - V_{IN}}{V_O} \times \dfrac{1}{f_{SW} \times C_O} + \dfrac{V_O}{V_{IN}} \times ESR\right)$
Output Capacitor RMS Current	$I_{C(RMS)}$	$I_{LOAD} \times \sqrt{\dfrac{V_O - V_{IN}}{V_{IN}}}$

V_O = Output Voltage
V_{IN} = Input Voltage
I_{LOAD} = Load Current
C_O = Output Capacitance
ESR = Output Capacitor's Equivalent Series Resistance
f_{SW} = Switching Frequency 260 kHz
V_{SAT} = Power Switch Saturation Voltage (0.6 V typical)
V_F = Diode Forward Voltage, 0.5 V for Schottky Diodes and 0.8 V for Ultrafast Recovery Diodes

Knowing the inductor value, we can calculate the following parameters using the formulas in Table 1:
D_{MAX} = 50%;
D_{MIN} = 37.4%;
Maximum I_{IN} = 800 mA;
Maximum $I_{L(AVE)}$ = 800 mA;
$I_{L(RP)}$ = 190 mA;
Maximum $I_{L(PK)}$ = 990 mA.

The inductor's saturation current rating shall be higher than $I_{L(PK)}$. If ripple current is small, $I_{L(AVE)}$ is approximately equal to the RMS current and shall be less than inductor's RMS current rating. Coiltronics' THIN–PAC inductor is selected for its low profile and its toroidal core for low EMI. The saturation current is 1.1 A and RMS current rating is 1.0 A.

In a boost converter, the output capacitor sees pulsed current, which causes significant output ripple on the ESR of the output capacitor. Ceramic capacitors have the lowest ESR compared with electrolytic and tantalum capacitors, at the expense of high cost. Here two 10 μF ceramic capacitors are used in parallel to double the capacitance. The ESR of these capacitors is negligible, so the output ripple comes almost entirely from the charging/discharging of the output capacitance, as shown in Figure 7. The output ripple is calculated using the equation in Table 1.
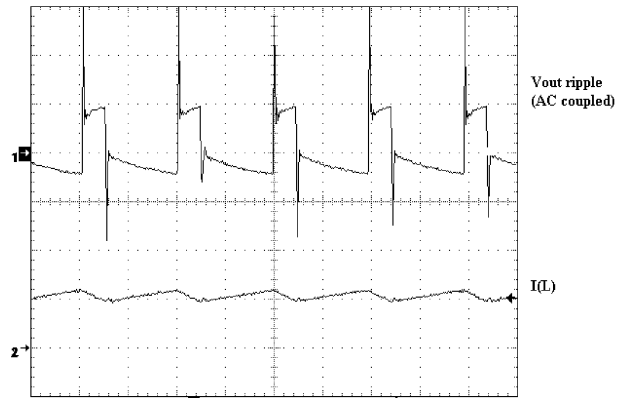
$V_{O(RP)}$ = 48 mV.

Figure 7. Output Voltage Ripple and Inductor Current

Select Diode

The diode in a boost converter conducts when the power switch is turned off. The average diode current is equal to the load current. The peak reverse voltage of the diode is equal to the output voltage. Schottky diodes have fast switching speed and low forward voltage. The diode selected for this design has a 1.5 A DC current rating and reverse breakdown voltage of 30 V. An ultra–fast diode is recommended for high temperature application.

Compensate the Error Amplifier

The goal of frequency compensation is to achieve the best transient response and DC regulation while ensuring the stability of the system. A typical compensation network, as shown in Figure 8, provides a two pole, one zero frequency characteristic. This is further illustrated in the Bode plot shown in Figure 9.

The DC gain of a transconductance error amplifier can be calculated as follows:

$$Gain_{DC} = G_m \times R_O$$

where:
G_m = error amplifier transconductance;
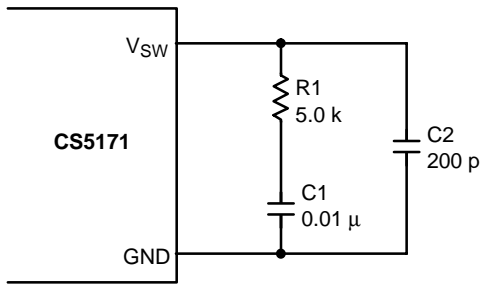R_O = error amplifier output resistance ≈ 1.0 MΩ

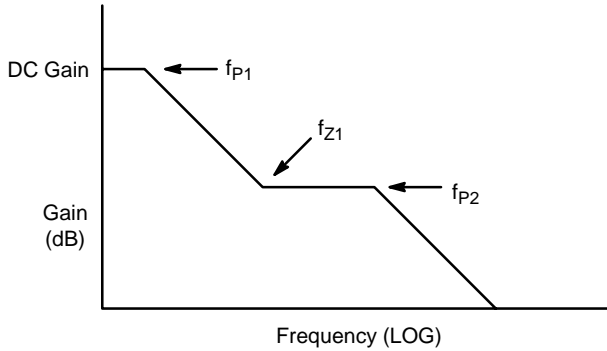**Figure 8. Typical Compensation Network**

Figure 9. Frequency Response of Typical Compensation Network

A high DC gain is desirable for achieving accurate line and load regulation. The CS5171 has DC gain of about 60 dB.

The next step is to pick the crossover frequency of the open loop frequency response. This frequency is typically set between $f_{SW}/10$ and $f_{SW}/20$. We use the 10 kHz as the crossover frequency in this design. The output capacitors and load create a pole whose frequency is determined by:

$$f_{Z1} = \frac{1}{2\pi CR_L} = \frac{1}{2\pi \times 20\,\mu \times 12.5} = 637 \text{ Hz}$$

At 10 kHz, this pole generates –31 dB gain on the power stage. In order to make the loop crossover at 10 kHz, the error amplifier must provide 31 dB gain. Knowing this, we can then determine the value of the resistor R1 in Figure 8.

$$R1 = \frac{31\text{ dB}}{G_m} \approx 5.0\text{ k}$$

C1 and R1 create a zero to provide adequate phase margin on the crossover frequency. Here we used 0.01μF capacitor such that the zero is located at:

$$f_{Z1} = \frac{1}{2\pi C1R1} = 3.2 \text{ kHz}$$

This frequency is low enough to provide over 45° of phase lead at 10 kHz to ensure stability. At the same time, the time constant of C1 × R1 = 51 μs is not too slow to degrade transient performance. The response of the converter to a load step can be observed in the "Typical Performance Characteristics" section in Figure 15.

The low frequency pole, f_{P1}, is determined by the error amplifier output resistance and C1:

$$f_{Z1} = \frac{1}{2\pi C1R_O} = 15 \text{ Hz}$$

The second pole, f_{P2}, located in the high frequency range, can be placed at the output filter's ESR zero or at half the switching frequency. Selection of the second pole below the switching frequency will help to filter out the switching noises. Here we use 200 pF such that this pole, determined by C2 and R1, is at:

$$f_{Z2} = \frac{1}{2\pi C2R1} = 160 \text{ kHz}$$

Select Input Capacitors

In boost circuits, the inductor becomes part of the input filter. In continuous conduction mode, the input current waveform is triangular and does not contain a large pulsed current. This reduces the requirements imposed on the input capacitor selection. The product of this inductor ripple current and the input capacitor's ESR determines the V_{IN} ripple. In this design, a 0.1 μF ceramic cap is used in parallel with a 10 μF ceramic cap, providing a total capacitance of 10.1 μF. As discussed earlier, the ESR of these capacitors is negligible, so the V_{IN} ripple is almost entirely due to the charging and discharging of the capacitors, as shown in Figure 10.
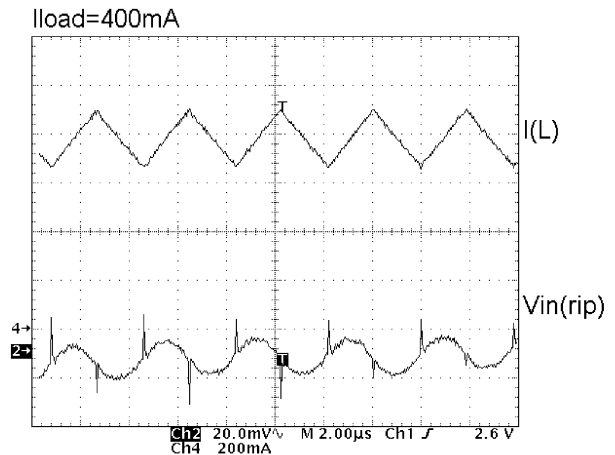
Figure 10. Full Load Input Ripple Voltage Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

Iload=400mA, D=48%
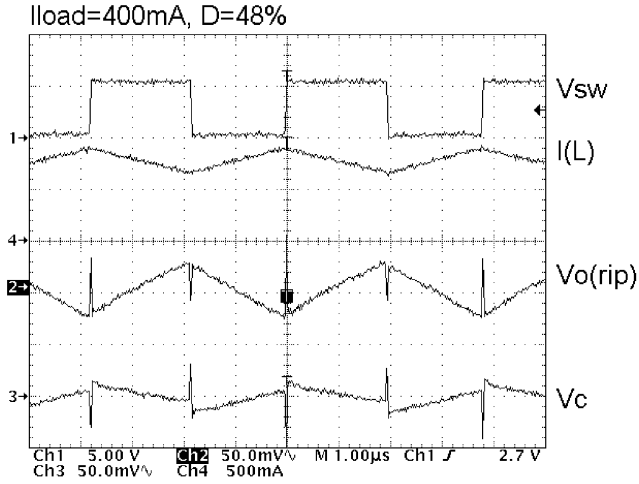
Figure 11. Full Load Operating Waveforms

Iload=60mA, D=38%
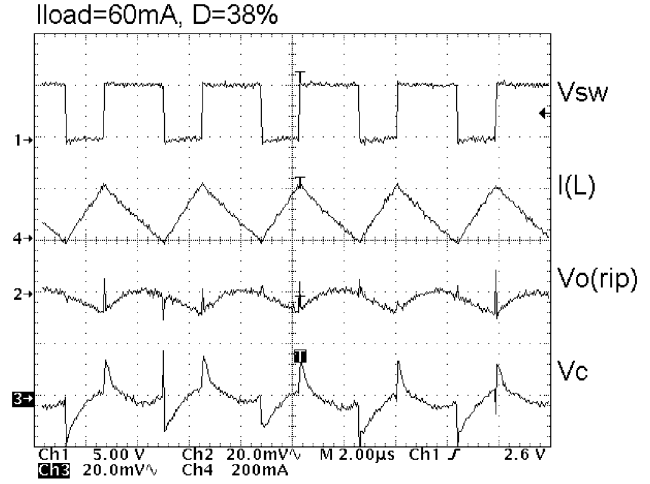
Figure 12. Minimum Load Operating Waveforms

Iload=400mA, D=50%
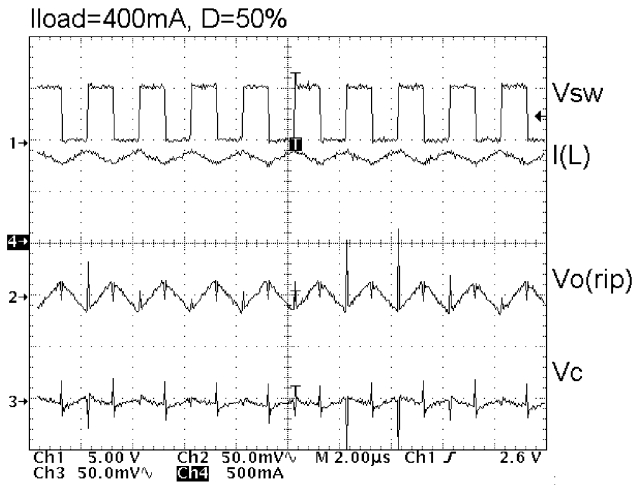
Figure 13. Full Load 500 kHz Operating Waveforms

Iload=60mA, D=40%
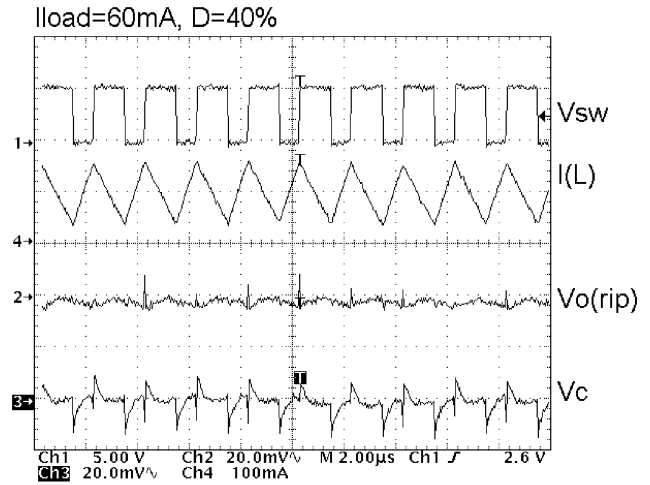
Figure 14. Minimum Load 500 kHz Operating Waveforms

Load Step from 200 to 400mA
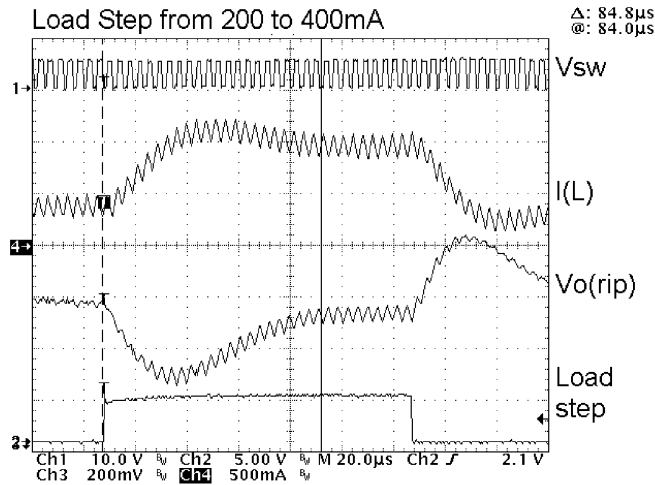
Figure 15. Transient Load

BILL OF MATERIALS

Ref. Des.	Vendor	Part Number	Type	PC/Board	Value
C1	Digikey	PCC1750–ND	Ceramic Cap	1	0.01 μF
C2	Digikey	PCC221ACVCT–ND	Ceramic Cap	1	220 pF
C4	Digikey	PCC1762–ND	Ceramic Cap	1	0.1 μF
C5–C7	TDK	C3216X5RJ106M	Ceramic Cap	3	10 μF
J1	Digikey	5002K–ND	Test Point	1	N/A
J2–J5	Digikey	V1055	Test Point	4	N/A
L1	Coiltronics	TP4_220	Inductor	1	22 μH
R1	Digikey	P4.99KHCT–ND	Resistor	1	4.99 k
R2	Digikey	P1.6KGCT–ND	Resistor	1	1.6 k
R3	Digikey	P560GCT–ND	Resistor	1	560
D1	Digikey	MA10705CT–ND	Schottky Diode	1	N/A
U1	**ON Semiconductor**	**CS5171/3**	**Controller**	**1**	**N/A**