REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15																			

REV STATUS OF SHEETS	REV													
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
92-03-16

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, FAST, 9-BIT BUFFERED NON-INVERTING LATCH, THREE-STATE OUTPUT, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-89758
A	67268	

SHEET 1 OF 15

1

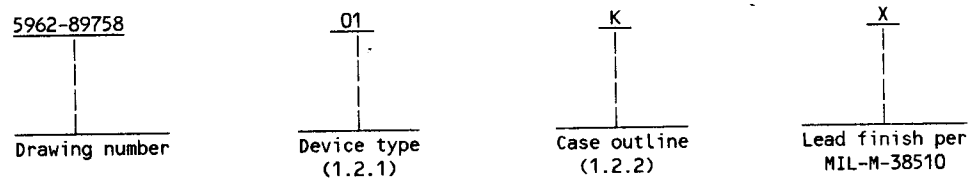
DESC FORM 193
JUL 91

5962-E517-92

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part or Identifying Number (PIN). The complete PIN shall be as shown in the following example:



1.2.1 Device type(s). The device type(S) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54FCT843A	9-bit buffered non-inverting latch, with three-state output, TTL compatible
02	54FCT843B	9-bit buffered non-inverting latch, with three-state output, TTL compatible
03	54FCT843C	9-bit buffered non-inverting latch, with three-state output, TTL compatible

1.2.2 Case outline(s). The case outline(s) shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
K	F-6 (24 lead, .640" x .420" x .090"), flat package
L	D-9 (24 lead, 1.280" x .310" x .200"), dual-in-line package
3	C-4 (28-terminal, .460" x .460" x .100"), square chip carrier package

1.3 Absolute maximum ratings. 1/

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 2/
Output voltage range	-0.5 V dc to V_{CC} + 0.5 V dc 2/
DC input diode current (I_{IK})	-20 mA
DC output diode current (I_{OK})	-0.5 mA
DC output current	±100 mA
Maximum power dissipation (P_D) 3/	500 mW
Thermal resistance, junction to case (Θ_{JC})	See MIL-M-38510, appendix C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C
Lead temperature (soldering, 10 seconds)	+300°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	0.0 V dc to V_{CC}
Maximum low level input voltage (V_{IL})	0.8 V dc
Minimum high level input voltage (V_{IH})	2.0 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ All voltages referenced to GND.
2/ For V_{CC} greater than 6.5 V dc, the input voltage range shall not exceed V_{CC}.
3/ Must withstand the added P_D due to short circuit test; e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standard, and bulletin. Unless otherwise specified, the following specification, standard, and bulletin of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

(Copies of the specification, standard, and bulletin required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.4 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103 (see 6.6 herein).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OH} = -300 µA	All	1, 2, 3	4.3		V
			I_{OH} = -15 mA	All	1, 2, 3	2.4		
Low level output voltage	V_{OL}	V_{CC} = 4.5 V, V_{IL} = 0.8 V, V_{IH} = 2.0 V	I_{OL} = 300 µA	All	1, 2, 3		0.2	V
			I_{OL} = 32 mA	All	1, 2, 3		0.5	
Input clamp voltage	V_{IK}	V_{CC} = 4.5 V, I_{IN} = -18 mA		All	1, 2, 3		-1.2	V
High level input current	I_{IH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		All	1, 2, 3		5.0	µA
Low level input current	I_{IL}	V_{CC} = 5.5 V, V_{IN} = GND		All	1, 2, 3		-5.0	µA
High impedence output current	I_{OZH}	V_{CC} = 5.5 V, V_{IN} = 5.5 V		All	1, 2, 3		10	µA
	I_{OZL}	V_{CC} = 5.5 V, V_{IN} = GND		All	1, 2, 3		-10	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V 1/ V_{OUT} = GND		All	1, 2, 3	-75		mA
Quiescent power supply current (CMOS inputs)	I_{CCQ}	$V_{IN} \le 0.2$ V or $V_{IN} \ge 5.3$ V, V_{CC} = 5.5 V, f_I = 0 MHz		All	1, 2, 3		1.5	mA
Quiescent power supply current (TTL inputs)	delta I_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V 2/		All	1, 2, 3		2.0	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified		Device type	Group A subgroups	Limits		Unit
						Min	Max	
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, $\overline{OE}$ = GND, One bit toggling 50% duty cycle, $V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V, Outputs open, LE = V_{CC} 3/		All	1, 2, 3		0.25	mA/ MHz
Total power supply current	I_{CC}	V_{CC} = 5.5 V, outputs open, f_I = 10 MHz, 50% duty cycle, One bit toggling, $\overline{OE}$ = GND, LE = V_{CC} 4/	$V_{IN} \ge 5.3$ V or $V_{IN} \le 0.2$ V	All	1, 2, 3		4.0	mA
			$V_{IN} \ge 3.4$ V or V_{IN} = GND	All	1, 2, 3		5.0	mA
Input capacitance	C_{IN}	See 4.3.1c		All	4		10	pF
Output capacitance	C_{OUT}	See 4.3.1c		All	4		12	pF
Functional tests		See 4.3.1d		All	7, 8			
Propagation delay time Dn to Yn, LE = High	t_{PLH1}, t_{PHL1}	C_L = 50 pF minimum R_L = 500Ω 5/ See figure 4		01	9,10,11	1.5	10.0	ns
				02		1.5	7.5	
				03		1.5	6.3	
Propagation delay time LE to Yn	t_{PLH2}, t_{PHL2}			01	9,10,11	1.5	13.0	ns
				02		1.5	10.5	
				03		1.5	6.8	
Propagation delay time PRE to Yn	t_{PLH3},			01	9,10,11	1.5	14.0	ns
				02		1.5	10.0	
				03		1.5	9.0	
Propagation delay time CLR to Yn	t_{PHL3},			01	9,10,11	1.5	14.0	ns
				02		1.5	11.0	
				03		1.5	10.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Output enable time, OE to Yn 5/	t_{PZH}, t_{PZL}	R_L = 500Ω, C_L = 50 pF minimum, See figure 4	01	9,10,11	1.5	13.0	ns
			02		1.5	8.5	
			03		1.5	7.3	
Output disable time, OE to Yn 5/	t_{PHZ}, t_{PLZ}		01	9,10,11	1.5	10.0	ns
			02		1.5	7.5	
			03		1.5	6.3	
Setup time, Dn to LE	t_s		01	9,10,11	2.5		ns
			02		2.5		
			03		2.5		
Hold time, Dn to LE	t_h		01	9,10,11	3.0		ns
			02		2.5		
			03		2.5		
Recovery time, PRE to Yn	t_{REC1}		01	9,10,11	17.0		ns
			02		13.0		
			03		12.0		
Recovery time, CLR to Yn	t_{REC2}		01	9,10,11	17.0		ns
			02		10.0		
			03		9.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V dc ±10% unless otherwise specified	Device type	Group A subgroups	Limits		Unit
					Min	Max	
Pulse width, LE	t_{w1}	C_L = 50 pF minimum, R_L = 500Ω, See figure 4	01	9,10,11	5.0		ns
			02		4.0		
			03		4.0		
Pulse width, $\overline{PRE}$	t_{w2}		01	9,10,11	7.0		ns
			02		4.0		
			03		4.0		
Pulse width, $\overline{CLR}$	t_{w3}		01	9,10,11	5.0		ns
			02		4.0		
			03		4.0		

1/ Not more than one output should be shorted at one time, and the duration of the short circuit condition should not exceed 1 second.

2/ TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.

3/ This parameter is not directly testable, but is derived for use in total power supply calculations.

4/ $I_{CC} = I_{CCQ} + (\text{delta } I_{CC} \times D_H \times N_T) + (I_{CCD} \times f_I \times N_I)$ where:

D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs at D_H
f_I = Input frequency in MHZ
N_I = Number of inputs at f_I

5/ The minimum limits are guaranteed, if not tested, to the limits specified in table I.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.6 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Test all applicable pins on five devices with zero failures.

d. Subgroups 7 and 8 tests shall verify the truth table as specified on figure 2.

Device types	01, 02 and 03	
Case outlines	L and K	3
Terminal number	Terminal symbol	
1	$\overline{OE}$	NC
2	D0	$\overline{OE}$
3	D1	D0
4	D2	D1
5	D3	D2
6	D4	D3
7	D5	D4
8	D6	NC
9	D7	D5
10	$\overline{D8}$	D6
11	$\overline{CLR}$	D7
12	GND	$\overline{D8}$
13	$\overline{LE}$	$\overline{CLR}$
14	$\overline{PRE}$	GND
15	Y8	NC
16	Y7	$\overline{LE}$
17	Y6	$\overline{PRE}$
18	Y5	Y8
19	Y4	Y7
20	Y3	Y6
21	Y2	Y5
22	Y1	NC
23	Y0	Y4
24	V_{CC}	Y3
25	---	Y2
26	---	Y1
27	---	Y0
28	---	V_{CC}

PIN DESCRIPTION

$\overline{CLR}$ - When $\overline{CLR}$ is low, the outputs are low if $\overline{OE}$ is low.
- When CLR is high, data can be entered into the latch.
Dn - The latch data inputs.
LE - The latch enable input. The latches are transparent when LE is high. Input data is latched on the high-to-low transition.
Yn - The three-state latch outputs.
$\overline{OE}$ - The output enable control. When $\overline{OE}$ is low, the outputs ar enabled. When OE is high, the outputs (Yn) are in the high impedance (off) state.
$\overline{PRE}$ - Preset line. When $\overline{PRE}$ is low, the outputs are high if $\overline{OE}$ is low. Preset overrides CLR.

FIGURE 1. Terminal connections.

INPUTS					OUTPUTS	FUNCTION
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	Dn	Yn	
H	H	H	X	X	Z	High Z
H	H	H	H	L	Z	High Z
H	H	H	H	H	Z	High Z
H	H	H	L	X	Z	Latched (High Z)
H	H	L	H	L	L	Transparent
H	H	L	H	H	H	Transparent
H	H	L	L	X	NC	Latched
H	L	L	X	X	H	Preset
L	H	L	X	X	L	Clear
L	L	L	X	X	H	Preset
L	H	H	L	X	Z	Latched (High Z)
H	L	H	L	X	Z	Latched (High Z)

H = High voltage level
L = Low voltage level
X = Irrelevant
Z = High impedence
NC = No Change

FIGURE 2. Truth table.

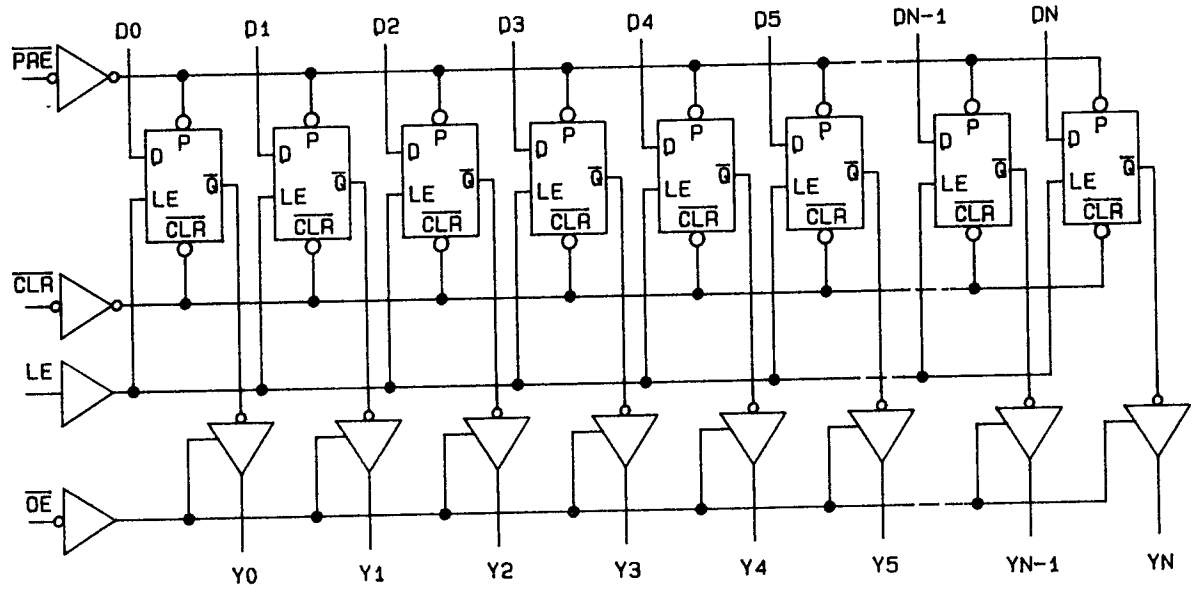
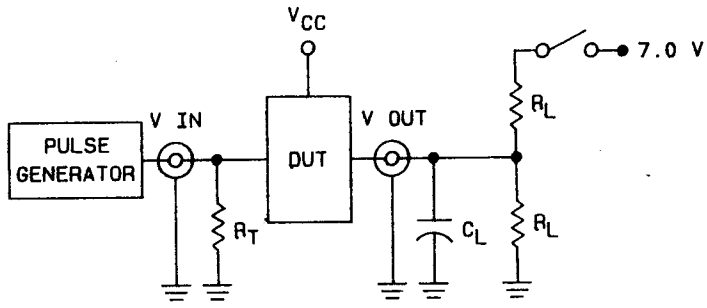


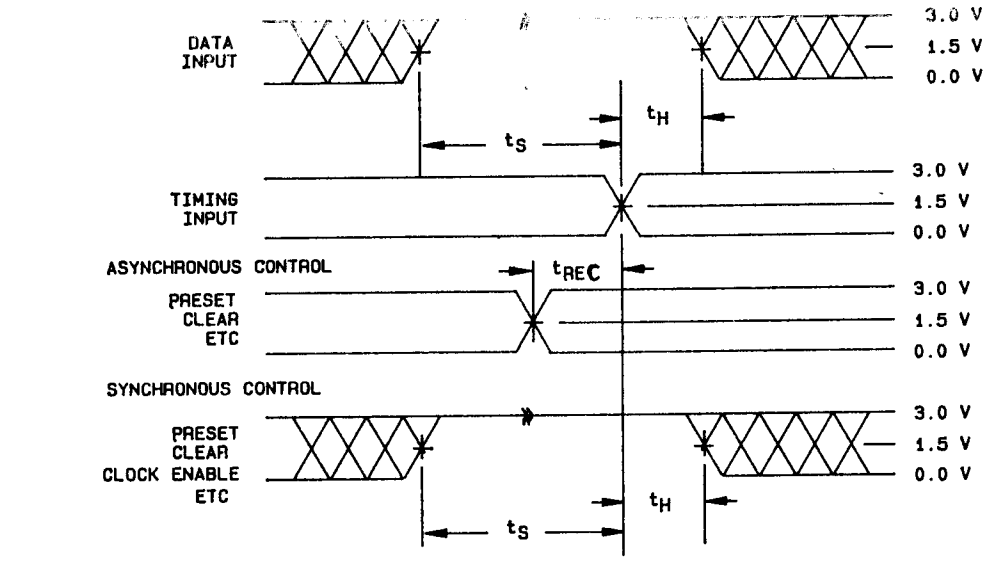
FIGURE 3. Logic diagram.

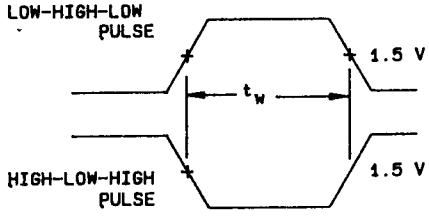


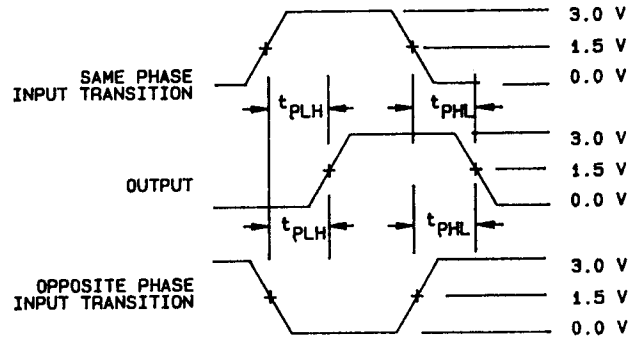
NOTES:
1. R_L = Load resistor, 500Ω or equivalent.
2. C_L = Load capacitance, 50 pF minimum, includes probe and jig capacitance.
3. R_T = Termination resistance; should be equal to Z_{OUT} of pulse generator.

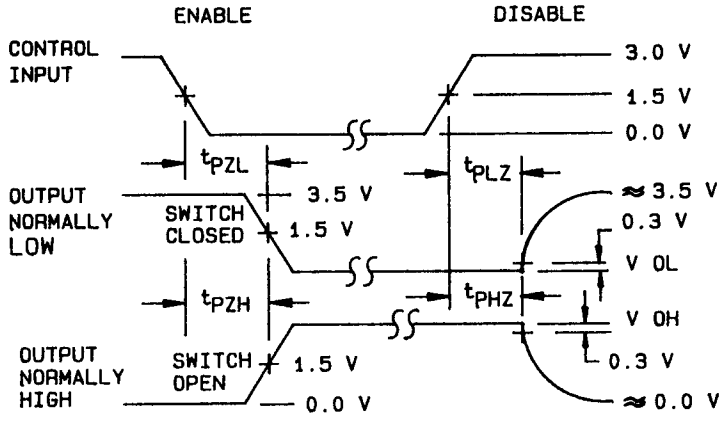
SWITCH POSITION	
Test	Switch
Open drain	Closed
t_{PLZ}	Closed
t_{PZL}	Closed
All other outputs	Open

FIGURE 4. Test circuit and switching waveforms.









NOTES:
1. Diagram shown for input control enable - low and input control disable - high
2. Pulse generator for all pulses: $t_f \leq 2.5$ ns; $t_r \leq 2.5$ ns.

FIGURE 4. Test circuit and switching waveforms - Continued.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*, 2, 3, 7 8, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4, 7, 8, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3

* PDA applies to subgroup 1.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.6 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.4 Record of users. Military and industry users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of the drawing covering microelectronics devices (FSC 5962) should contact DESC-ECS, telephone (513)296-6022).

6.5 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone (513) 296-5375.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-ECS.