2Mx64 3.3V Simultaneous Operation Flash Multi-Chip Package

**Preliminary*

FEATURES

- Access Times of 100, 120, 150ns
- Packaging
  - 159 PBGA, 13x22mm - 1.27mm pitch
- 1,000,000 Erase/Program Cycles
- Sector Architecture
  - Bank 1 (8Mb): eight 4K word, fifteen 32K word
  - Bank 2 (24Mb): forty-eight 32K word
- Bottom boot block
- Zero Power Operation
- Organized as 2Mx64 or 2x2Mx32
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt for Read and Write Operations
- Simultaneous Read/Write Operation:
  - Data can be continuously read from one bank while executing erase/program functions in another bank
  - Zero latency between read and write operations
- Erase Suspend/Resume
  - Suspends erase operations to allow programming in same bank
- $\overline{\text{Data}}$ Polling and Toggle Bits
  - Provides a software method of detecting the status of program or erase cycles
- Unlock Bypass Program command
  - Reduces overall programming time when issuing multiple program command sequences
- Ready/$\overline{\text{Busy}}$ output (RY/$\overline{\text{BY}}$)
  - Hardware method for detecting program or erase cycle completion
- Hardware reset pin ($\overline{\text{RESET}}$)
  - Hardware method of resetting the internal state machine to the read mode
- $\overline{\text{WP}}$/ACC input pin
  - Write protect ($\overline{\text{WP}}$) function allows protection of two outermost boot sectors, regardless of sector protect status
  - Acceleration (ACC) function accelerates program timing
- Sector Protection
  - Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - Temporary Sector Unprotect allows changing data in protected sectors in-system

Note: For programming information refer to Flash Programming W72M64V-XBX Application Note.

** Preliminary datasheet. This datasheet describes a product that is not characterized or qualified and is subject to change without notice.*

FIG 1: PIN CONFIGURATION FOR W72M64V-XBX

TOP VIEW

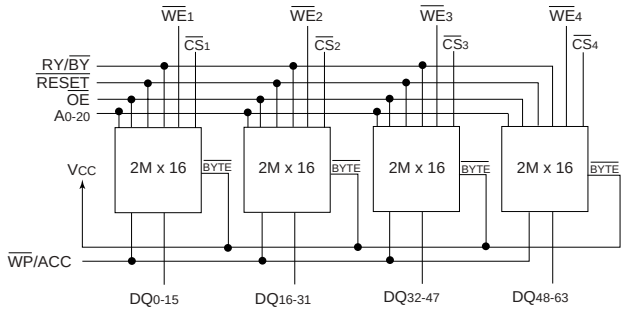
	1	2	3	4	5	6	7	8	9	10
A		GND	GND	GND	VCC	VCC	GND	GND	GND	VCC
B	VCC	GND	DQ41	$\overline{WE3}$	VCC	DQ57	DNU	$\overline{WE4}$	VCC	VCC
C	VCC	DQ33	DQ43	DQ45	DQ47	DQ49	DQ59	DQ61	DQ63	VCC
D	VCC	DQ40	DQ35	DQ37	DQ39	DQ56	DQ51	DQ53	DQ55	VCC
E	VCC	DQ32	DQ42	DQ44	DQ46	DQ48	DQ58	DQ60	DQ62	VCC
F	GND	$\overline{CS3}$	DQ34	DQ36	DQ38	$\overline{CS4}$	DQ50	DQ52	DQ54	GND
G	GND	$\overline{OE}$	A0	DNU	VCC	A12	A16	DNU*	A20	GND
H	GND	A2	$\overline{WP/ACC}$	A11	GND	VCC	A7	A10	A15	GND
J	GND	A3	A6	A9	VCC	GND	A1	$\overline{RESET}$	A13	GND
K	GND	A4	A17	RY/$\overline{BY}$	GND	A14	A5	A18	A8	GND
L	GND	DQ17	$\overline{WE2}$	DQ29	DNU	DQ9	DQ4	$\overline{WE1}$	A19	GND
M	VCC	DQ24	DQ19	DQ21	DQ31	DQ1	DQ11	DQ6	DQ15	VCC
N	VCC	DQ16	DQ26	DQ28	DQ23	DQ8	DQ3	DQ13	DQ7	VCC
P	VCC	$\overline{CS2}$	DQ18	DQ20	DQ30	DQ0	DQ10	DQ5	DQ14	VCC
R	VCC	VCC	DQ25	DQ27	DQ22	$\overline{CS1}$	DQ2	DQ12	GND	VCC
T	VCC	GND	GND	GND	VCC	VCC	GND	GND	GND	VCC

** Ball G8 is DNU on this device and will become A21 on the W74M64V-XBX*

PIN DESCRIPTION

DQ0-63	Data Inputs/Outputs
A0-20	Address Inputs
$\overline{WE}$1-4	Write Enables
$\overline{CS}$1-4	Chip Selects
$\overline{OE}$	Output Enable
$\overline{RESET}$	Hardware Reset
$\overline{WP}$/ACC	Hardware Write Protect/Acceleration
RY/$\overline{BY}$	Ready/Busy Output
VCC	Power Supply
GND	Ground
DNU	Do Not Use

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameter		Unit
Operating Temperature	-55 to +125	°C
Supply Voltage Range (V_{CC})	-0.5 to +4.0	V
Signal Voltage Range	-0.5 to Vcc +0.5	V
Storage Temperature Range	-55 to +150	°C
Endurance (write/erase cycles)	1,000,000 min.	cycles

NOTES:

1. Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

CAPACITANCE

(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{WE}_{1-4}$ capacitance	C_{WE}	V_{IN} = 0 V, f = 1.0 MHz	25	pF
$\overline{CS}_{1-4}$ capacitance	C_{CS}	V_{IN} = 0 V, f = 1.0 MHz	25	pF
Data I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V, f = 1.0 MHz	12	pF
Address input capacitance	C_{AD}	V_{IN} = 0 V, f = 1.0 MHz	25	pF
$\overline{RESET}$ capacitance	C_{RS}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
RY/$\overline{BY}$ capacitance	C_{RB}	V_{IN} = 0 V, f = 1.0 MHz	20	pF
$\overline{WP}$/ACC capacitance	C_{WA}	V_{IN} = 0 V, f = 1.0 MHz	30	pF

This parameter is guaranteed by design but not tested.

DATA RETENTION

Parameter	Test Conditions	Min	Unit
Pattern Data	150°C	10	Years
Retention Time	125°C	20	Years

DC CHARACTERISTICS - CMOS COMPATIBLE

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Symbol	Conditions	Min	Max	Unit
Input Leakage Current	I_{LI}	V_{CC} = 3.6V, V_{IN} = GND to V_{CC}	-10	10	µA
Output Leakage Current	I_{LO}	V_{CC} = 3.6V, V_{OUT} = GND to V_{CC}	-10	10	µA
V_{CC} Active Current for Read (1)	I_{CC1}	$\overline{CS}$ = $\overline{V_{IL}}$, OE = V_{IH}, f = 5MHz		65	mA
V_{CC} Active Current for Program or Erase (2,3)	I_{CC2}	$\overline{CS}$ = $\overline{V_{IL}}$, OE = V_{IH}, $\overline{WE}$ = V_{IL}		120	mA
V_{CC} Standby Current (2)	I_{CC3}	$\overline{CS}$ = $\overline{RESET}$ = V_{CC} ± 0.3V		20	µA
V_{CC} Reset Current (2)	I_{CC4}	$\overline{RESET}$ = V_{SS} ± 0.3V		20	µA
Automatic Sleep Mode (2,4)	I_{CC5}	V_{IH} = V_{CC} ± 0.3V; V_{IL} = V_{SS} ± 0.3V		20	µA
V_{CC} Active Read-While-Program Current (1,2)	I_{CC6}	$\overline{CS}$ = $\overline{V_{IL}}$, OE = V_{IH}		180	mA
V_{CC} Active Program-While-Erase Current (1,2)	I_{CC7}	$\overline{CS}$ = $\overline{V_{IL}}$, OE = V_{IH}		180	mA
V_{CC} Active Program-While-Erase-Suspended Current (2,5)	I_{CC8}	$\overline{CS}$ = $\overline{V_{IL}}$, OE = V_{IH}		140	mA
ACC Accelerated Program Current	I_{ACC}	$\overline{CS}$ = $\overline{V_{IL}}$, OE = V_{IH} — ACC Pin		40	mA
		$\overline{CS}$ = $\overline{V_{IL}}$, OE = V_{IH} — V_{CC} Pin		120	mA
Input Low Voltage	V_{IL}		-0.5	0.8	V
Input High Voltage	V_{IH}		0.7 x Vcc	Vcc + 0.3	V
Voltage for $\overline{WP}$/ACC Sector Protect/Unprotect and Program Acceleration	V_{HH}	Vcc = 3.0V + 0.3V	8.5	9.5	V
Voltage for Autoselect and Temporary Sector Unprotect	V_{ID}	Vcc = 3.0V + 0.3V	8.5	12.5	V
Output Low Voltage	V_{OL}	I_{OL} = 4.0 mA, V_{CC} = 3.0V		0.45	V
Output High Voltage	V_{OH1}	I_{OH} = -2.0 mA, V_{CC} = 3.0V	0.85 x V_{CC}		V
Low V_{CC} Lock-Out Voltage (5)	V_{LKO}		2.3	2.5	V

NOTES:

1. *The I_{CC} current listed includes both the DC operating current and the frequency dependent component (at 5 MHz). The frequency component typically is less than 8 mA/MHz, with $\overline{OE}$ at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with V_{CC} = V_{CC} MAX*
3. *I_{CC} active while Embedded Algorithm (program or erase) is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30ns.*
5. *Not 100% tested.*

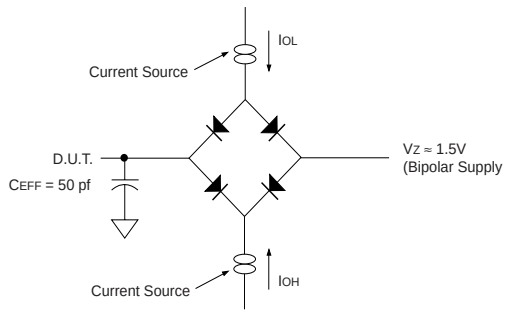
AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{CS}$ CONTROLLED

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Write Enable Setup Time	t_{WLEL}	t_{WS}	0		0		0		ns
Chip Select Pulse Width	t_{ELEH}	t_{CP}	45		50		50		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVEH}	t_{DS}	45		50		50		ns
Data Hold Time	t_{EHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{ELAX}	t_{AH}	45		50		50		ns
Chip Select Pulse Width High	t_{EHEL}	t_{CPH}	30		30		30		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}			300		300		300	µs
Sector Erase Time (2)	t_{WHWH2}			15		15		15	sec
Read Recovery Time Before Write (3)	t_{GHEL}		0		0		0		ns
Chip Programming Time (4)				108		108		108	sec

1. Typical value for t_{WHWH1} is 7µs.
2. Typical value for t_{WHWH2} is 0.7 sec.
3. Guaranteed by design, but not tested.
4. Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.

FIG 2: AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 2.5	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

AC CHARACTERISTICS – WRITE/ERASE/PROGRAM OPERATIONS - $\overline{WE}$ CONTROLLED

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter	Symbol		-100		-120		-150		Unit
			Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{AVAV}	t_{WC}	100		120		150		ns
Chip Select Setup Time	t_{ELWL}	t_{CS}	0		0		0		ns
Write Enable Pulse Width	t_{WLWH}	t_{WP}	50		50		65		ns
Address Setup Time	t_{AVWL}	t_{AS}	0		0		0		ns
Data Setup Time	t_{DVWH}	t_{DS}	50		50		65		ns
Data Hold Time	t_{WHDX}	t_{DH}	0		0		0		ns
Address Hold Time	t_{WLAX}	t_{AH}	50		50		65		ns
Write Enable Pulse Width High	t_{WHWL}	t_{WPH}	30		30		35		ns
Duration of Byte Programming Operation (1)	t_{WHWH1}		300		300			300	µs
Sector Erase (2)	t_{WHWH2}		15		15			15	sec
Read Recovery Time before Write (3)	t_{GHWL}		0		0		0		ns
VCC Setup Time	t_{VCS}		50		50		50		µs
Chip Programming Time (4)				108		108		108	sec
Address Setup Time to $\overline{OE}$ low during toggle bit polling		t_{ASO}	15		15		15		ns
Address Hold Time From $\overline{CS}$ or $\overline{OE}$ high during toggle		t_{AHT}	0		0		0		ns
Output Enable High during toggle bit polling		t_{OEPH}	20		20		20		ns
Latency Between Read and Write Operations		$t_{SR/W}$	0		0		0		ns
Write Recovery Time from RY/$\overline{BY}$		t_{RB}	0		0		0		ns
Program/Erase Valid to RY/$\overline{BY}$		t_{BUSY}	90		90		90		ns

1. *Typical value for t_{WHWH1} is 7µs.*
2. *Typical value for t_{WHWH2} is 0.7 sec.*
3. *Guaranteed by design, but not tested.*
4. *Typical value is 36 sec. The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*

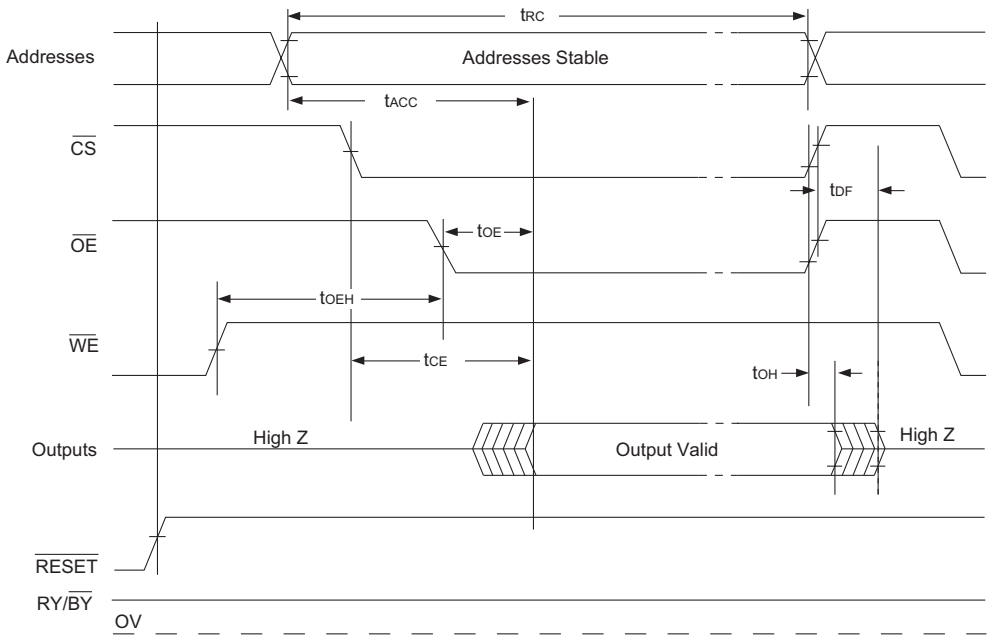
AC CHARACTERISTICS – READ-ONLY OPERATIONS

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

Parameter		Symbol		-100		-120		-150		Unit
				Min	Max	Min	Max	Min	Max	
Read Cycle Time		t_{AVAV}	t_{RC}	100		120		150		ns
Address Access Time		t_{AVQV}	t_{ACC}		100		120		150	ns
Chip Select Access Time		t_{ELQV}	t_{CE}		100		120		150	ns
Output Enable to Output Valid		t_{GLQV}	t_{OE}		40		50		55	ns
Chip Select High to Output High Z (1)		t_{EHQZ}	t_{DF}		20		20		20	ns
Output Enable High to Output High Z (1)		t_{GHQZ}	t_{DF}		20		20		20	ns
Output Hold from Addresses, $\overline{CS}$ or $\overline{OE}$ Change, Whichever occurs first		t_{AXQX}	t_{OH}	0		0		0		ns
Output Enable Hold Time (1)	Read		t_{OEH}	0		0		0		
	Toggle and Data Polling			10		10		10		

1. *Guaranteed by design, not tested.*

FIG 3: AC WAVEFORMS FOR READ OPERATIONS



AC CHARACTERISTICS – HARDWARE RESET ($\overline{RESET}$)

Parameter	Symbol	-100		-120		-150		Unit
		Min	Max	Min	Max	Min	Max	
$\overline{RESET}$ Pin Low (During Embedded Algorithms) to Read Mode (See Note)	t_{ready}		20		20		20	µs
$\overline{RESET}$ Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	t_{ready}		500		500		500	ns
$\overline{RESET}$ Pulse Width	t_{RP}	500		500		500		ns
$\overline{RESET}$ High Time Before Read (See Note)	t_{RH}	50		50		50		ns
$\overline{RESET}$ Low to Standby Mode	t_{RPD}	20		20		20		µs
RY/$\overline{BY}$ Recovery Time	t_{RB}	0		0		0		ns

Note: Not tested.

FIG 4: RESET TIMINGS NOT DURING EMBEDDED ALGORITHMS

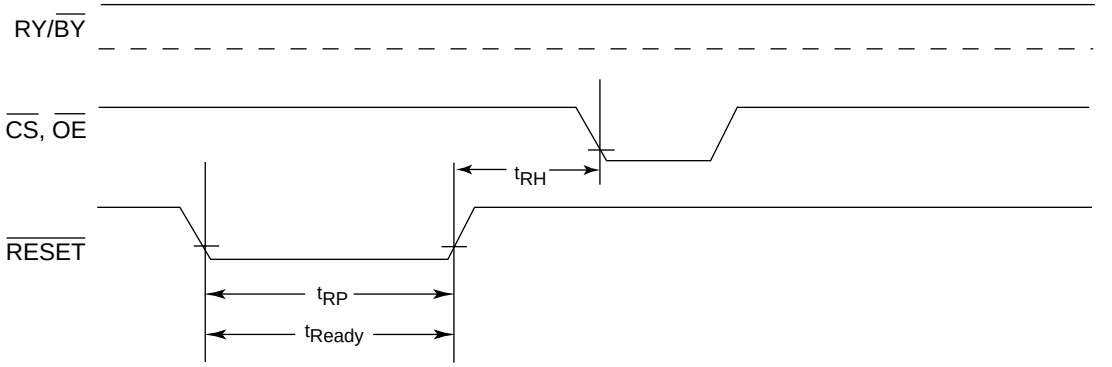


FIG 5: RESET TIMINGS DURING EMBEDDED ALGORITHMS

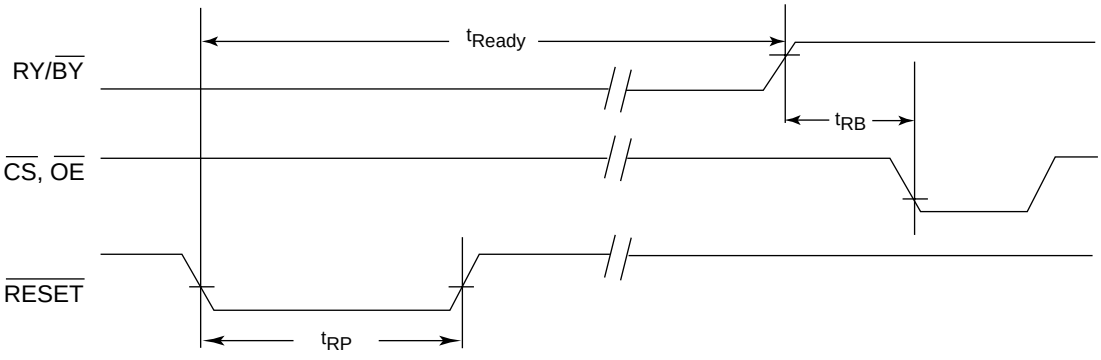
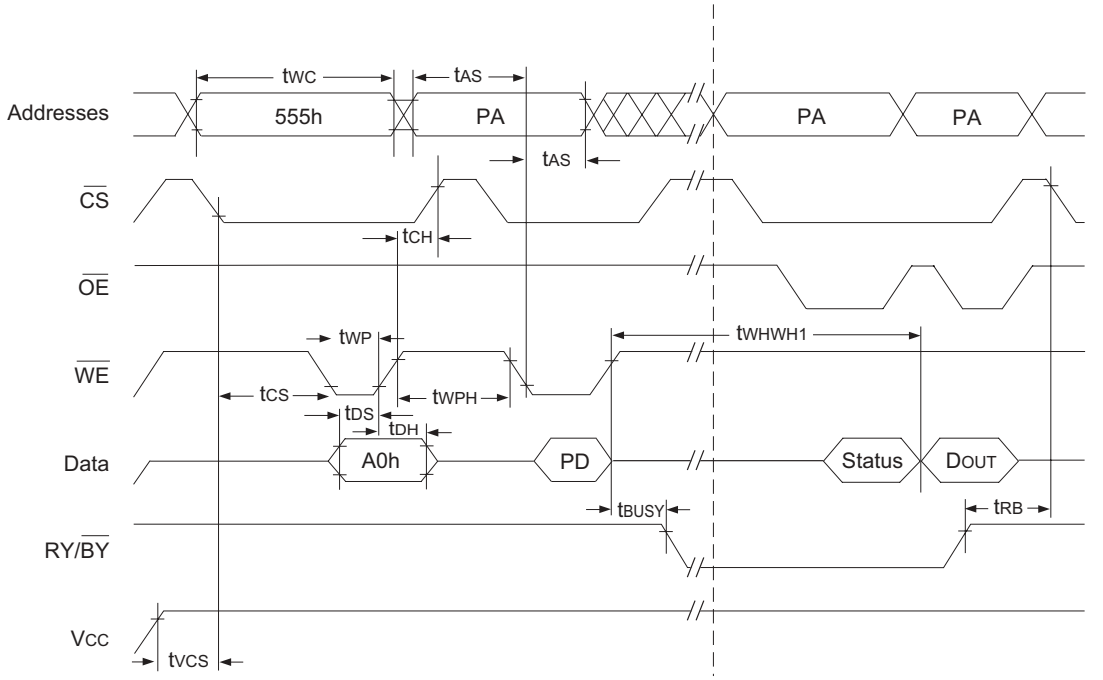


FIG 6: PROGRAM OPERATION

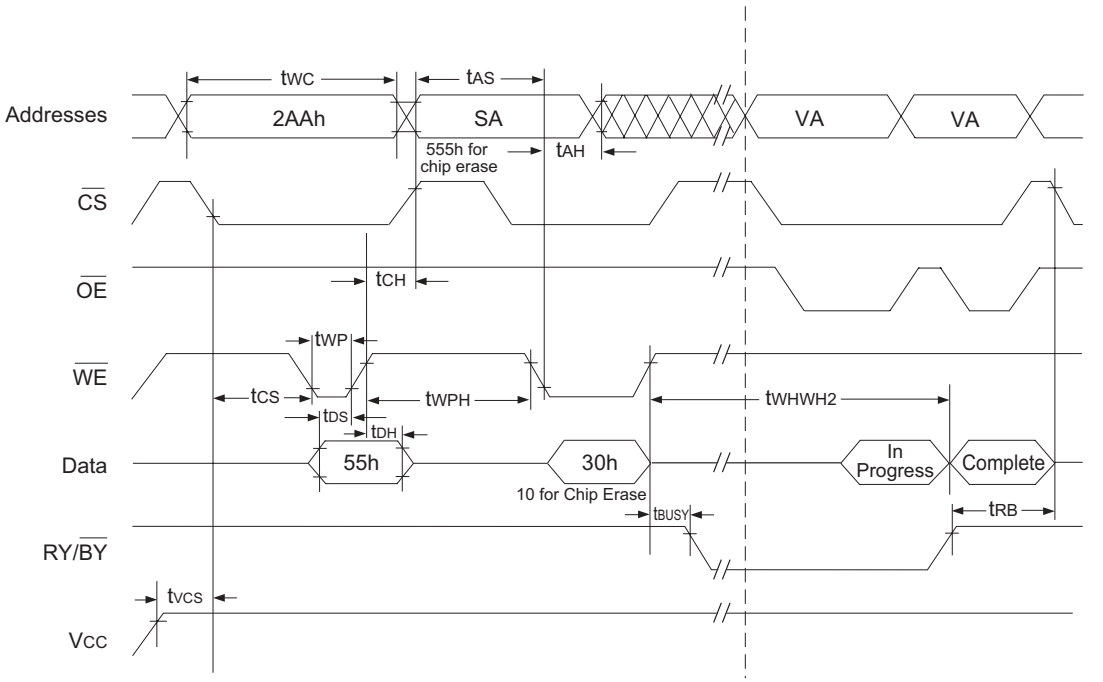


NOTES:

1. *PA is the address of the memory location to be programmed.*
2. *PD is the data to be programmed at byte address.*
3. *DOUT is the output of the data written to the device.*
4. *Figure indicates last two bus cycles of four bus cycle sequence.*

FIG 7: ACCELERATED PROGRAM TIMING DIAGRAM

FIG 8: CHIP/SECTOR ERASE OPERATION TIMINGS



Notes:

1. *SA = Sector Address (for Sector Erase), VA = Valid Address for reading status data*

FIG 9: BACK TO BACK READ/WRITE CYCLE TIMINGS

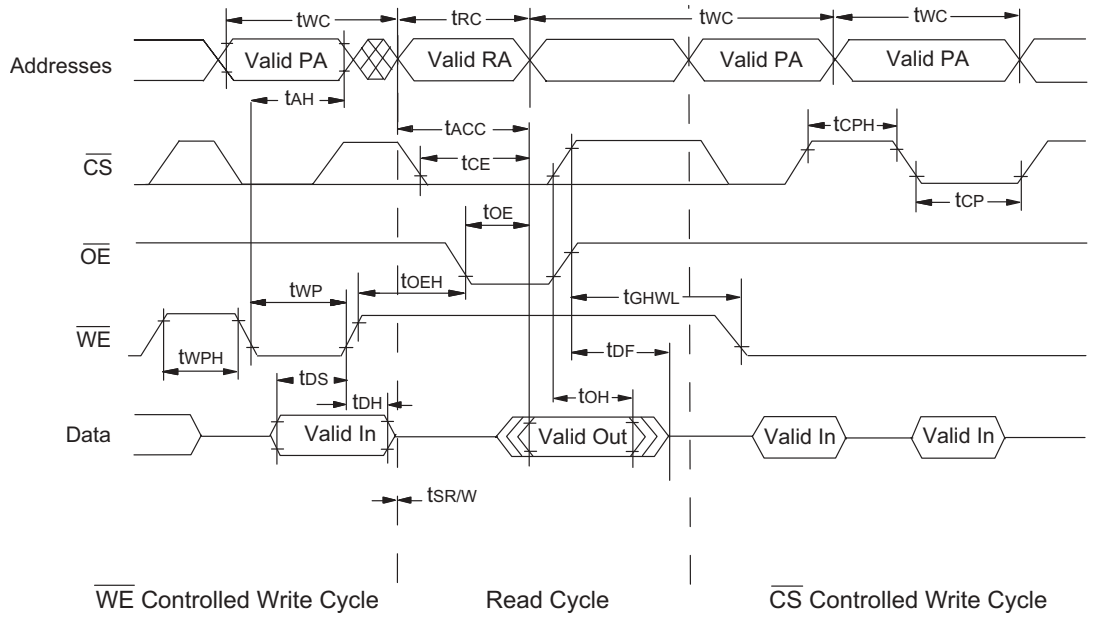
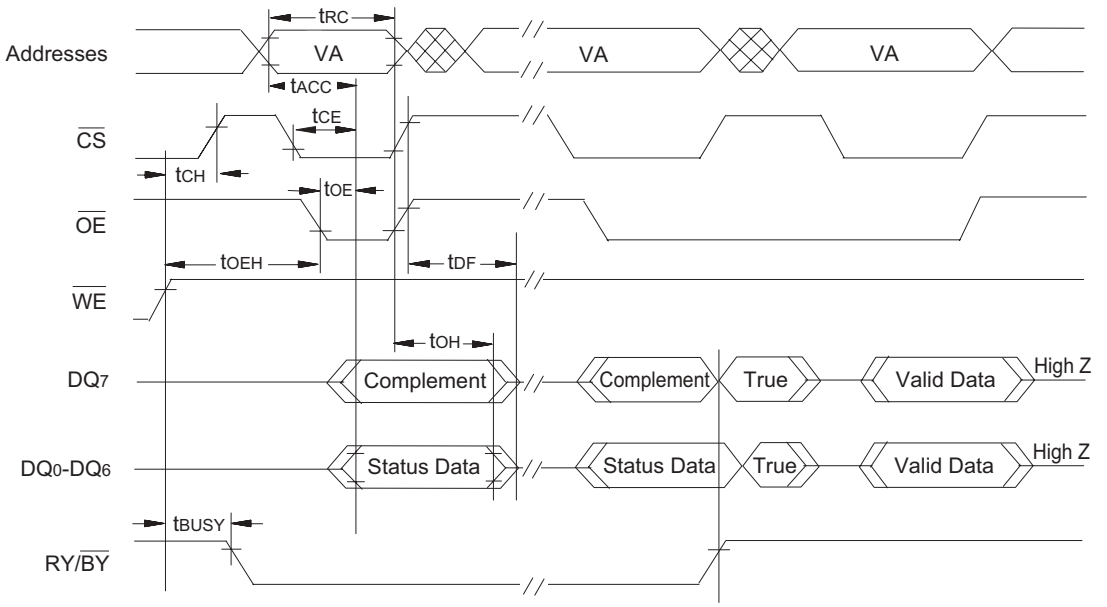
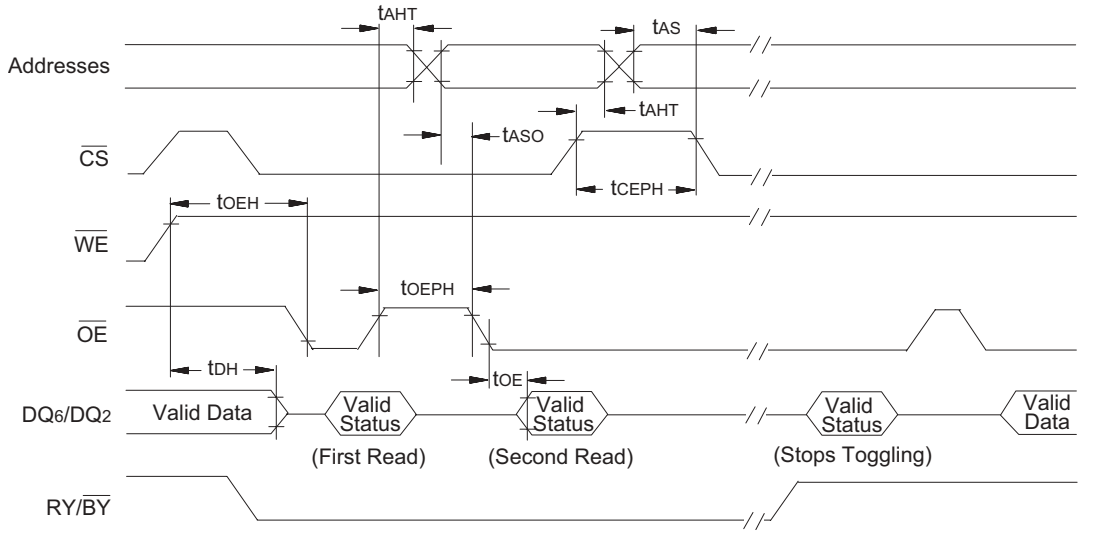


FIG. 10: DATA POLLING TIMINGS (DURING EMBEDDED ALGORITHMS)



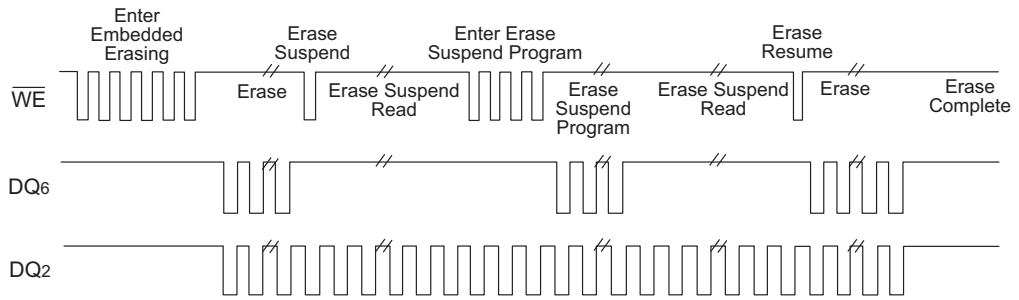
NOTE: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

FIG 11: TOGGLE BIT TIMINGS (DURING EMBEDDED ALGORITHMS)



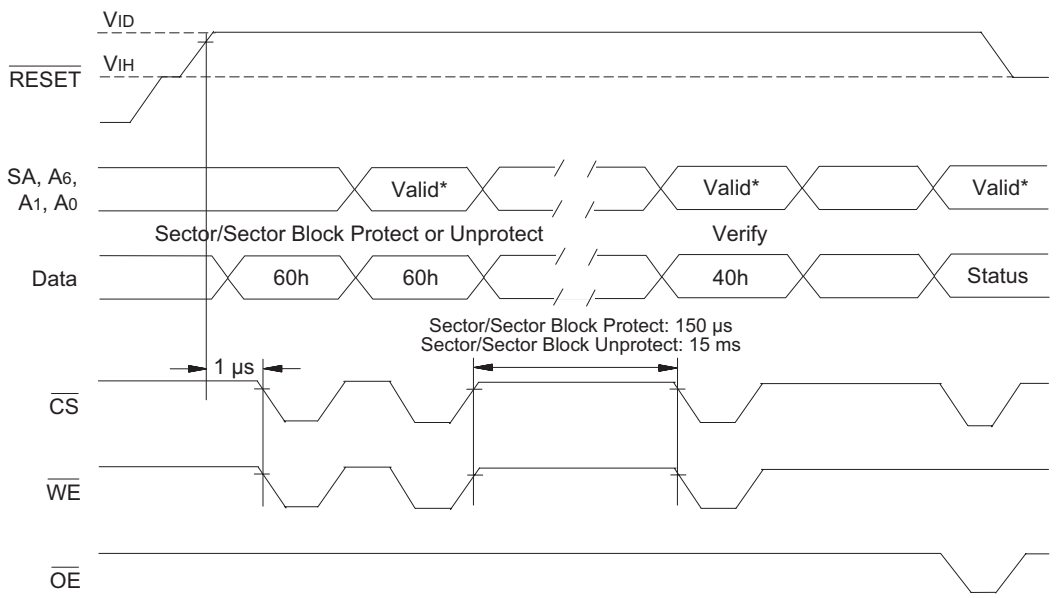
NOTE: *VA = Valid address, not required for DQ_6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

FIG 12: DQ2 VS. DQ6



NOTE: *DQ_2 toggles only when read at an address within an erase-suspended sector. The system may use $\overline{OE}$ or $\overline{CS}$ to toggle DQ_2 and DQ_6.*

FIG 13: SECTOR/SECTOR BLOCK PROTECT AND UNPROTECT TIMING DIAGRAM



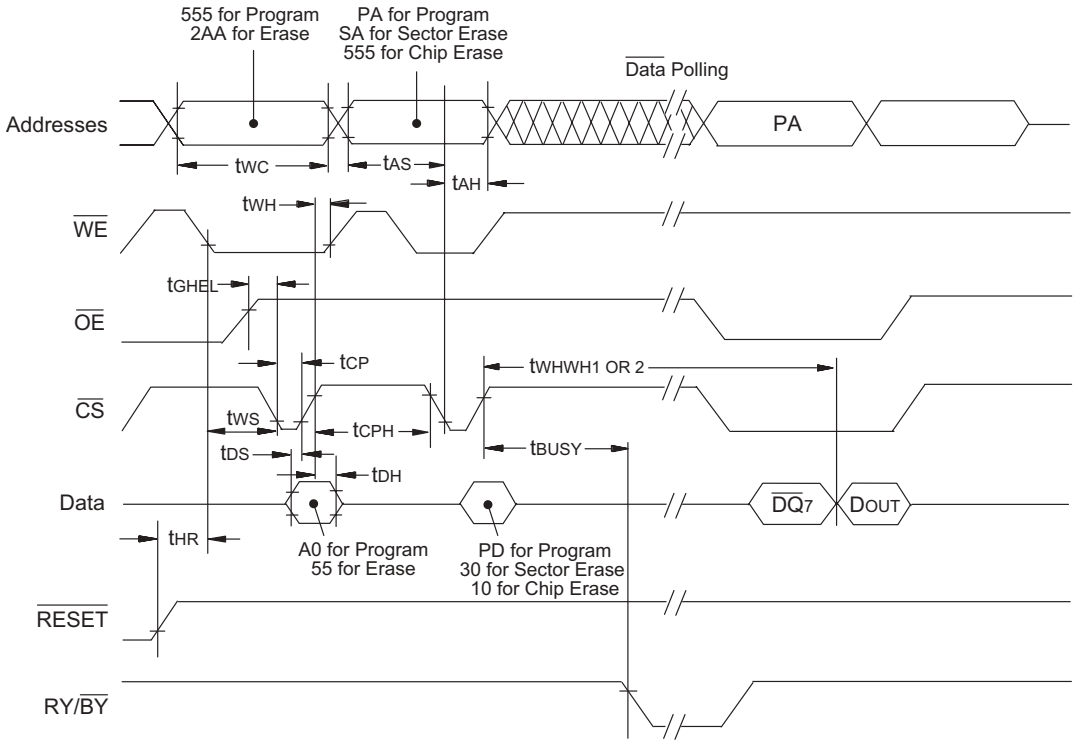
NOTES:
For sector protect, $A_6 = 0$, $A_1 = 1$, $A_0 = 0$. For sector unprotect, $A_6 = 1$, $A_1 = 1$, $A_0 = 0$.

AC CHARACTERISTICS – ALTERNATE $\overline{CS}$ CONTROLLED ERASE AND PROGRAM OPERATIONS

Parameter					Speed Options			
JEDEC	Std	Description			100	120	150	Unit
t_{AVAV}	t_{WC}	Write Cycle Time (1)		Min	90	120	150	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	0	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	50	50	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45	50	50	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	0	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write ($\overline{OE}$ High to $\overline{WE}$ Low)		Min	0	0	0	ns
t_{WLEL}	t_{WS}	$\overline{WE}$ Setup Time		Min	0	0	0	ns
t_{EHWH}	t_{WH}	$\overline{WE}$ Hold Time		Min	0	0	0	ns
t_{ELEH}	t_{CP}	$\overline{CS}$ Pulse Width		Min	45	50	50	ns
t_{EHEL}	t_{CPH}	$\overline{CS}$ Pulse Width High		Min	30	30	30	ns
t_{WHWH1}	t_{WHWH1}	Programming Operation	Byte	Typ	9	9	9	µs
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte		Typ	7	7	7	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation		Typ	0.7	0.7	0.7	sec

NOTE:
1. Not tested.

FIG 14: ALTERNATE $\overline{CS}$ CONTROLLED WRITE (ERASE/PROGRAM) OPERATION TIMINGS

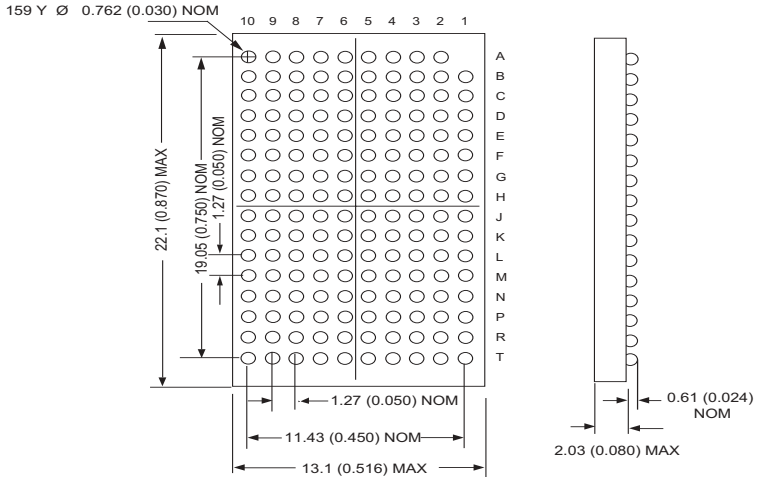


NOTES:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ_7 is the complement of the data written to the device. D_{OUT} is the data written to the device.*

PACKAGE: 159 PBGA

BOTTOM VIEW



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

ORDERING INFORMATION

W 7 2M64 V XXX B X

WHITE ELECTRONIC DESIGNS CORP.

Flash

ORGANIZATION, 2M x 64
User configurable as 2 x 2M x 32

3.3V Power supply

ACCESS TIME (ns)
100 = 100ns
120 = 120ns
150 = 150ns

PACKAGE TYPE:
B = 159 Plastic BGA, 13mm x 22mm

DEVICE GRADE:

M	=	Military Screened	-55°C to +125°C
I	=	Industrial	-40°C to +85°C
C	=	Commercial	0°C to +70°C

Document Title

2M x 64 Simultaneous Operation Flash Multi-Chip Package

Revision History

Rev #	History	Release Date	Status
Rev 0	Initial Release	November 2002	Advanced
Rev 1	Update (pg 1, 14, 15) 1.1 Change status to preliminary 1.2 Change mechanical drawing to new style	November 2003	Preliminary