■ **Structure**　　　　　　Silicon Monolithic Integrated Circuit

■ **Product Name**　　　　For DSC handshake guard, signal processing and motor driving IC

■ **Model Name**　　　　　**BH9992GU**

■ **Function**
- ・　GYROAMP 2ch
- ・　HALLAMP 2ch
- ・　R-2R type 8bit D/A converter 5ch
- ・　R-2R type 10bit D/A converter 2ch
- ・　No dead zone system PWM Driver
- ・　SAW wave oscillator
- ・　Regulator
- ・　Rail to Rail AMP

■ Absolute maximum ratings

| Item | Symbol | Standard value | Unit |
|---|---|---|---|
| Power supply voltage | VC, VDD, PVCC | 7.0 | V |
| Power dissipation (*1) | PD | 1400 | mW |
| Operation temperature range | TOPR | −10～70 | ℃ |
| Storage temperature range | TSTG | −40～125 | ℃ |
| H Bridge output current1 | IOUT1 | 300 | mA |
| H Bridge output current2 (*2) | IOUT2 | 500 | mA |

*1　Mounting board specification（Rohm standard board）　Material：The glass fabric base epoxy
　　Dimensions：50[mm]×58[mm]×1.75[mm] (8 layers)
　　When using it at Ta=25℃ or more, 14 [mW] of 1[℃] decreases.
*2　Instantaneous current（1[us] or less）

■ Operating condition

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| VC power supply voltage | VC | 3.0 (*3) | 3.3 | 5.5 | V |
| VDD power supply voltage（≦VC） | VDD | 2.5 | 3.0 | 5.5 | V |
| PVCC power supply voltage | PVCC | 3.0 | 5.0 | 5.5 | V |
| Serial clock frequency | FSCLK | — | 1.0 | 4.0 | MHz |
| DACOUT limit load capacity 1 (DAC0OUT,DAC3OUT,DAC4OUT) | CLA1 | — | — | 0.1 | μF |
| Between VDDOUT and GND, load capacity | CLVDDOUT | 1.0 | — | 30.0 | μF |

*3　When VDDOUT is used, the Min. operating condition of VC power supply voltage is 3.2[V].

・A radiation is not designed.

■ Physical Dimension

Package type nama ： VCSP85H4



Fig.1 Physical Dimension （Unit ： mm）
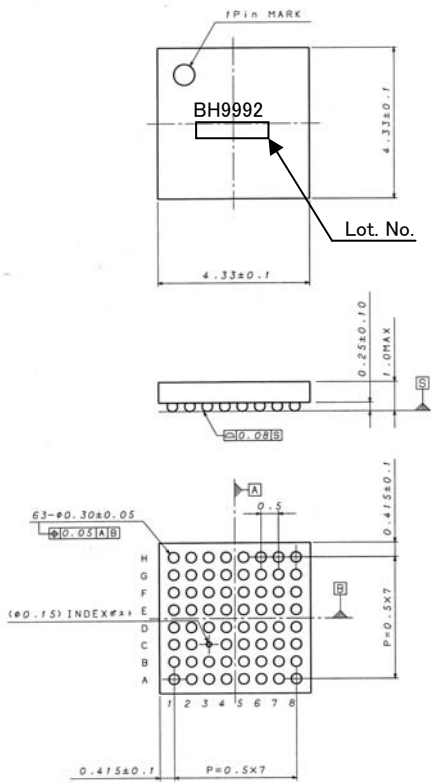
■ CHIP Backside PIN Arrangement

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 |
|---|---|---|---|---|---|---|---|---|
| H | | AMP4 +IN | AMP4 −IN | AMP3 −IN | AMP3 +IN | AGND | AMP11 +IN | |
| G | AMP9 +IN | AMP2 OUT | AMP4 OUT | AMP3 OUT | VDD2 | AMP11 OUT | AMP13 OUT | AMP13 −IN |
| F | GND1 | AMP2 −IN | AMP7 OUT | AMP1 OUT | AMP1 −IN | AMP11 −IN | VDD1 | AMP13 +IN |
| E | VDD OUT | VC1 | AMP7 −IN | DAC4 OUT | DAC0 OUT | VREF1 IN | AMP14 OUT | AMP14 −IN |
| D | AMP9 −IN | AMP9 OUT | AMP8 −IN | AMP8 OUT | DAC3 OUT | AMP12 −IN | AMP12 OUT | AMP14 +IN |
| C | AMP10 −IN | AMP10 OUT | | XSTBY | DAC6 OUT | DAC5 OUT | VC2 | AMP12 +IN |
| B | AMP10 +IN | GND3 | VC3 | LD | DATA | CLK | GND2 | PGND2 |
| A | | PGND1 | OUT1F | OUT1R | PVCC | OUT2R | OUT2F | |

Please keep open for ▊ the terminal, when you use.

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■ PIN Description

| PIN No. | Pin Name | Pin explanation |
|---|---|---|
| 1-A | — | — |
| 2-A | PGND1 | Power block ground |
| 3-A | OUT1F | CH1 forward output |
| 4-A | OUT1R | CH1 reverse output |
| 5-A | PVCC | Power block power supply |
| 6-A | OUT2R | CH2 reverse output |
| 7-A | OUT2F | CH2 forward output |
| 8-A | — | — |
| 1-B | AMP10+IN | AMP10+Input |
| 2-B | GND3 | GND |
| 3-B | VC3 | VC power supply |
| 4-B | LD | Serial data loading input |
| 5-B | DATA | Serial data input |
| 6-B | CLK | Serial clock input |
| 7-B | GND2 | GND |
| 8-B | PGND2 | Power block ground |
| 1-C | AMP10-IN | AMP10-input |
| 2-C | AMP10OUT | AMP10 output |
| 3-C | — | — |
| 4-C | XSTBY | Standby control input |
| 5-C | DAC6OUT | DAC6 output |
| 6-C | DAC5OUT | DAC5 output |
| 7-C | VC2 | VC power supply |
| 8-C | AMP12+IN | AMP12+input |
| 1-D | AMP9-IN | AMP9-input |
| 2-D | AMP9OUT | AMP9 output |
| 3-D | AMP8-IN | AMP8-input |
| 4-D | AMP8OUT | AMP8 output |
| 5-D | DAC3OUT | DAC3 output |
| 6-D | AMP12-IN | AMP12-input |
| 7-D | AMP12OUT | AMP12 output |
| 8-D | AMP14+IN | AMP14+input |

| PIN No. | Pin Name | Pin explanation |
|---|---|---|
| 1-E | VDDOUT | VDD regulator output |
| 2-E | VC1 | VC power supply |
| 3-E | AMP7-IN | AMP7-input |
| 4-E | DAC4OUT | DAC4 output |
| 5-E | DAC0OUT | DAC0 output |
| 6-E | VREF1IN | AMP reference input |
| 7-E | AMP14OUT | AMP14 output |
| 8-E | AMP14-IN | AMP14-input |
| 1-F | GND1 | GND |
| 2-F | AMP2-IN | AMP2-input |
| 3-F | AMP7OUT | AMP7 output |
| 4-F | AMP1OUT | AMP10 output |
| 5-F | AMP1-IN | AMP1-input |
| 6-F | AMP11-IN | AMP11-input |
| 7-F | VDD1 | VDD power supply |
| 8-F | AMP13+IN | AMP13+input |
| 1-G | AMP9+IN | AMP9+input |
| 2-G | AMP2OUT | AMP2 output |
| 3-G | AMP4OUT | AMP4 output |
| 4-G | AMP3OUT | AMP3 output |
| 5-G | VDD2 | VDD power supply |
| 6-G | AMP11OUT | AMP11 output |
| 7-G | AMP13OUT | AMP13 output |
| 8-G | AMP13-IN | AMP13-input |
| 1-H | — | — |
| 2-H | AMP4+IN | AMP4+input |
| 3-H | AMP4-IN | AMP4- input |
| 4-H | AMP3-IN | AMP3- input |
| 5-H | AMP3+IN | AMP3+ input |
| 6-H | AGND | Analog GND |
| 7-H | AMP11+IN | AMP11+input |
| 8-H | — | — |

■ Whole Block Diagram
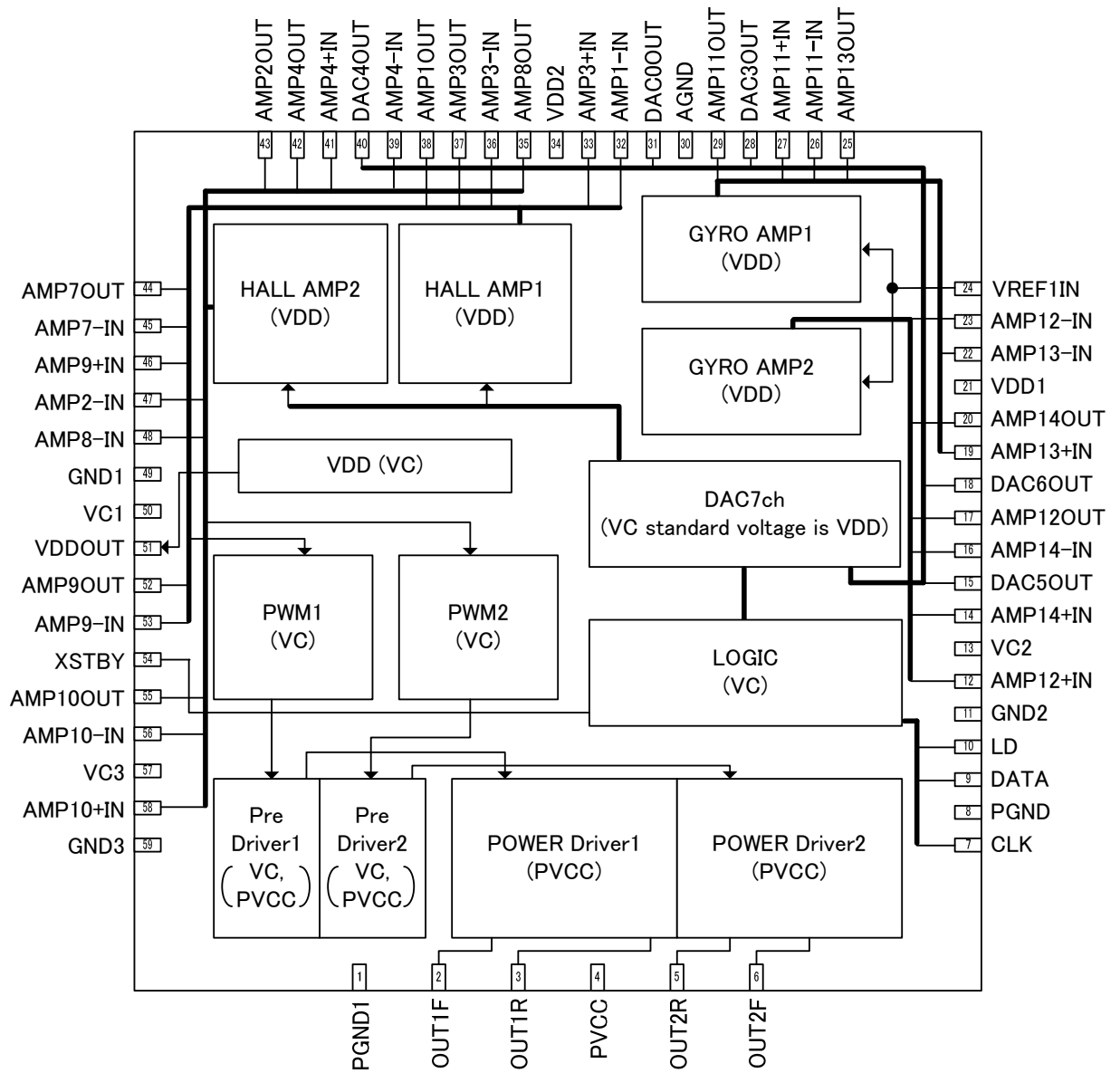


Fig.2    Whole Block Diagram

■ Electrical characteristic

◎Circuit current（VC=3.3[V], VDD=3.0[V], PVCC=5.0[V], DAC0OUT=VREF1IN, Ta=25[℃] except as otherwise noted.）

| Item | Symbol | Standard value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Current consumption 1 at standby (VC+VDD+PVCC) | ISTBY | — | 1.5 | 10 | μA | XSTBY, CLK, DI, LD=L |
| Current consumption1 when operating (VC+VDD) | ICC1 | — | 4.0 | 6.0 | mA | DAC0=080H DAC1,2,3,4,5,6=000H |
| Current consumption2 when operating (VC+VDD) | ICC2 | — | 11.0 | 16.5 | mA | DAC0=080H, DAC1,2,3,4,=0FFH DAC 5,6,=3FFH |
| Current consumption3 when operating (PVCC) | ICC3 | — | 25 | 50 | μA | XSTBY=H, POWSTBY_N="0" |

◎HALL Sensor input _AMP
（VC=3.3[V], VDD=3.0[V], PVCC=5.0[V], DAC0=080H, DAC0OUT=VREF1IN, Ta=25[℃] except as otherwise noted）

| Item | Symbol | Standard value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| 〈HALL_AMP (A1,A2)〉 | | | | | | |
| Output voltage | H1VOUT | 2.50 | — | — | V | DAC1, 2=0FFH External 500[Ω], 270[Ω] |
| Output voltage range (Hi) (Open loop) | H1VOH | 2.40 | — | — | V | DAC1, 2=0FFH Outflow current 5.0[mA], |
| Output voltage range (Low) (Open loop) | H1VOL | — | — | 0.4 | V | DAC1, 2=000H Inflow current 5.0[mA], VIN=250[mV] |

◎HALL Sensor output _AMP
（VC=3.3[V], VDD=3.0[V], PVCC=5.0[V], DAC0, DAC3, DAC4=080H, DAC0OUT=VREF1IN, Ta=25[℃] except as otherwise noted）

| Item | Symbol | Standard value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| 〈HALL_AMP (A3,A4,A9,A10)〉 | | | | | | |
| Output voltage 1 (Open loop) | H2VOUT1 | 2.9 | — | — | V | VINP=1.2[V], VINN=1.1[V] |
| Output voltage 2 (Open loop) | H2VOUT2 | — | — | 0.2 | V | VINP=1.1[V], VINN=1.2[V] |
| Voltage gain | H2GVD | 38.5 | 40.0 | 41.5 | dB | VIN=10[mVpp] (Differential voltage input) f=100[Hz] |
| Cutoff frequency | H2fc | 4.1 | 8.1 | 12.1 | kHz | −3[dB], Capa 10[pF] |
| 〈HALL_AMP (A5−A7, A6−A8)〉 | | | | | | |
| Output voltage 1 | H3VOUT1 | 2.8 | — | — | V | VINP Input=1.125, VINN Input=0.375 HALLSW1,3=ON, HALLSW2=OFF DAC0=0BFH, DAC3,4=040H |
| Output voltage 2 | H3VOUT2 | — | — | 0.2 | V | VINP Input=0.375, VINN Input=1.125 HALLSW1,3=ON, HALLSW2=OFF DAC0=040H, DAC3,4=0BFH |
| Output voltage 3 | H3VOUT3 | 2.8 | — | — | V | VINP Input=0.0[V], VINN Input=3.0[V] HALLSW2=ON, HALLSW1,3=OFF DAC3,4=0AAH |
| Output voltage 4 | H3VOUT4 | — | — | 0.2 | V | VINP Input=0.0[V], VINN Input=0.0[V] HALLSW2=ON, HALLSW1,3=OFF DAC3,4=055H |
| Voltage gain | H3GVD | −1.5 | 0 | 1.5 | dB | VIN=10[mVpp] (Differential voltage input) f=100[Hz] |
| Cutoff frequency | H3fc | 23.0 | 46.0 | 69.0 | kHz | −3[dB], Capa 33[pF] |

◎GYRO_AMP
(VC=3.3[V], VDD=3.0[V], PVCC=5.0[V], DAC0=080H, DAC0OUT=VREF1IN, Ta=25[℃] except as otherwise noted)

| Item | Symbol | Standard value | | | Unit | Notes |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| <GYRO_AMP (A11,A12)> | | | | | | |
| Output voltage 1 (Open loop) | G1VOUT1 | 2.9 | — | — | V | VINP =1.2[V], VINN =1.1[V] |
| Output voltage 2 (Open loop) | G1VOUT2 | — | — | 0.2 | V | VINP =1.1[V], VINN =1.2[V] |
| Voltage gain | G1GVD | 38.5 | 40.0 | 41.5 | dB | VIN=10[mVpp] (Differential voltage input) f=100[Hz] |
| Cutoff frequency | G1fc | 4.1 | 8.1 | 12.1 | kHz | −3[dB], Capa 33[pF] |
| <GYRO_AMP (A13,A14)> | | | | | | |
| Output voltage 1 | G2VOUT1 | 1.30 | 1.50 | 1.70 | V | GYROSW2=ON, GYROSW1, At GYROSW3=OFF, VINP=open |
| Output voltage 2 | G2VOUT2 | 1.1 | 1.50 | 1.90 | V | GYROSW1, GYROSW2=ON, At GYROSW3=OFF, VINP=open |
| Voltage gain | G2GVD | 36.3 | 37.8 | 39.3 | dB | GYROSW2=ON, At GYROSW3=OFF VIN=10[mVpp] (Differential voltage input) f=100[Hz] |
| Cutoff frequency | G2fc | 1.1 | 2.1 | 3.1 | kHz | GYROSW2=ON, At GYROSW3=OFF −3[dB], Capa 100[pF] |
| Voltage gain | G2GVD2 | 32.5 | 34.0 | 35.5 | dB | GYROSW2=ON, At GYROSW3=ON VIN=10[mVpp] (Differential voltage input) f=100[Hz] |
| Cutoff frequency | G2fc2 | 1.7 | 3.3 | 4.9 | kHz | GYROSW2=ON, At GYROSW3=ON −3[dB], Capa 100[pF] |

REV. D

■ Directions
1. Absolute maximum ratings
This IC might be destroyed when the absolute maximum ratings, such as impressed voltages (VC,PVCC,VDD) or the operating temperature range (TOPR) is exceeded, and whether the destruction is short circuit mode or open circuit mode cannot be specified. Please take into consideration the physical countermeasures for safety, such as fusing, if a particular mode that exceeds the absolute maximum rating is assumed.

2. Reverse polarity connection
Connecting the power line to the IC in reverse polarity (from that recommended) will damage the part. Please utilize the direction protection device as a diode in the supply line.

3. Power supply line
Due to switching and EMI noise generated by magnetic components (inductors and motors), using electrolytic and ceramic suppress filter capacitors close to the IC power input terminals (Vcc and GND) is recommended. Please note: the electrolytic capacitor value decreases at lower temperatures.

4. GND line
The ground line is where the lowest potential and transient voltages are connected to the IC.

5. Thermal design
Do not exceed the power dissipation (Pd) of the package specification rating under actual operation, and please design enough temperature margins. (Refer to page 10.)

6. Short circuit mode between terminals and wrong mounting
Do not mount the IC in the wrong direction and be careful about the reverse-connection of the power connector. Moreover, this IC might be destroyed when the dust short the terminals between them or GND.

7. Radiation
Strong electromagnetic radiation can cause operation failures.

8. ASO(Area of Safety Operation.)
Do not exceed the maximum ASO and the absolute maximum ratings of the output driver.

9. TSD(Thermal shut-down)
The TSD is activated when the junction temperature (Tj) reaches $175^0$C(with +/-$25^0$C hysteresis), and the output terminal is switched to Hi-z. The TSD circuit aims to intercept IC from high temperature. The guarantee and protection of IC are not purpose. Therefore, please do not use this IC after TSD circuit operates, nor use it for assumption that operates the TSD circuit.

10. Capacitor between output and GND
If a large capacitor is connected between the output and GND, this IC might be destroyed when Vcc becomes 0V or GND, because the electric charge accumulated in the capacitor flows to the output. Please set said capacitor to smaller than 0.1$\mu$F.

11. Inspection by the set circuit board

The stress might hang to IC by connecting the capacitor to the terminal with low impedance. Then, please discharge electricity in each and all process. Moreover, in the inspection process, please turn off the power before mounting the IC, and turn on after mounting the IC. In addition, please take into consideration the countermeasures for electrostatic damage, such as giving the earth in assembly process, transportation or preservation.

12. Each input terminal

This IC is a monolithic IC, and has P$^+$ isolation and P substrate for the element separation. Therefore, a parasitic PN junction is firmed in this P-layer and N-layer of each element. For instance, the resistor or the transistor is connected to the terminal as shown in the figure below. When the GND voltage potential is greater than the voltage potential at Terminals A or B, the PN junction operates as a parasitic diode. In addition, the parasitic NPN transistor is formed in said parasitic diode and the N layer of surrounding elements close to said parasitic diode. These parasitic elements are formed in the IC because of the voltage relation. The parasitic element operating causes the wrong operation and destruction. Therefore, please be careful so as not to operate the parasitic elements by impressing to input terminals lower voltage than GND(P substrate). Please do not apply the voltage to the input terminal when the power-supply voltage is not impressed. Moreover, please impress each input terminal lower than the power-supply voltage or equal to the specified range in the guaranteed voltage when the power-supply voltage is impressing.
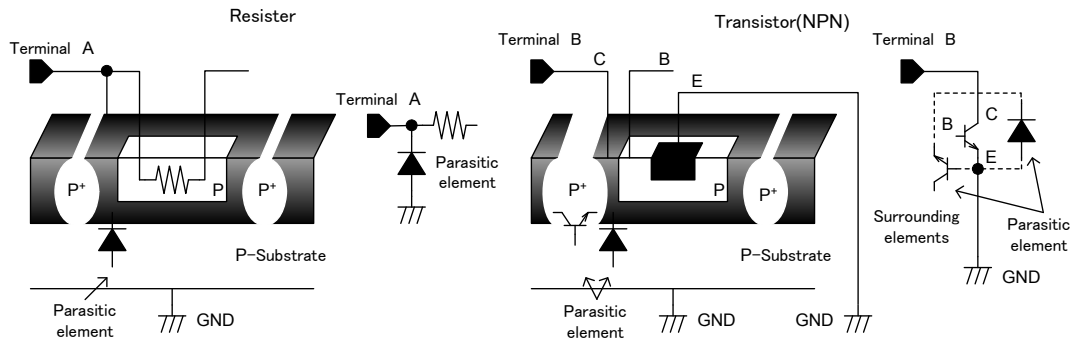
Simplified structure of IC

13. Earth wiring pattern

Use separate ground lines for control signals and high current power driver outputs. Because these high current outputs that flows to the wire impedance changes the GND voltage for control signal. Therefore, each ground terminal of IC must be connected at the one point on the set circuit board. As for GND of external parts, it is similar to the above-mentioned.

14. Reverse brake

When you do the reversal brake from the high-velocity revolution note the counter electromotive force. Moreover, confirm the output current enough and examine the rotational speed which uses the reversal brake.

15. About the capacitor between PVCC-PGND

The PVCC-PGND capacitor absorbs the change in a steep voltage and the current because of the PWM drive. As a result, there is a role to suppress the disorder of the PVCC voltage. However, the effect decreases by the influence of the wiring impedance etc. if the capacitor becomes far from IC. Arrange the PVCC-PGND capacitor near IC.

16. Bypass capacitor

Between the supply power supplies connect the bypass capacitor(0.1 $\mu$F) near the pin of this IC.

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