

74VHC257

Quad 2-Input Multiplexer with TRI-STATE® Outputs

General Description

The VHC257 is an advanced high speed CMOS Quad 2-Channel Multiplexer featuring TRI-STATE outputs. It is fabricated with silicon gate CMOS technology and achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and enable ($\overline{OE}$) inputs.

When the $\overline{OE}$ input is held to a logic HIGH, the outputs are switched to a high impedance state, allowing the outputs to interface directly with bus-oriented systems.

The SELECT decoding determines whether the I_{0x} or I_{1x} inputs get routed to their corresponding outputs.

An Input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems

and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

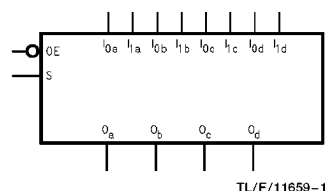
Features

- High speed
- Low power dissipation:
 $I_{CC} = 4 \mu A$ (max.) at $T_A = 25^\circ C$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min.)
- All inputs are equipped with a power down protection function
- Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- Wide operating voltage range: V_{CC} (opr) = 2V ~ 5.5V
- Low noise: $V_{OLP} = 0.8V$ (max.)
- Pin and function compatible with 74HC257

Commercial	Package Number	Package Description
74VHC257M	M16A	16-Lead Molded JEDEC SOIC
74VHC257SJ	M16D	16-Lead Molded EIAJ SOIC
74VHC257MTC	MTC16	16-Lead Molded JEDEC Type 1 TSSOP
74VHC257N	N16E	16-Lead Molded DIP

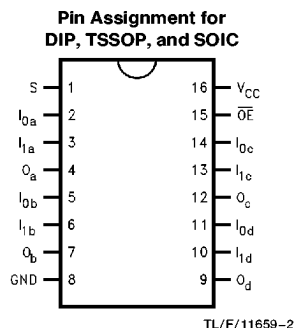
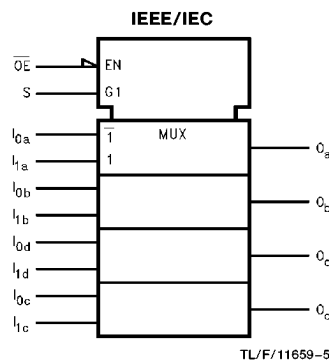
Note: Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Pin Names	Description
$I_{0a}-I_{0d}$	Source 0 Data Inputs
$I_{1a}-I_{1d}$	Source 1 Data Inputs
$\overline{OE}$	Output Enable
S	Select Input
O_a-O_d	Outputs

Connection Diagram



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Functional Description

The 'VHC257 is a quad 2-input multiplexer with TRI-STATE outputs. It selects four bits of data from two sources under the control of a Common Data Select Input. When the Select input is LOW, the I_{0x} inputs are selected and when Select is HIGH, the I_{1x} inputs are selected. The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

$$O_a = \overline{OE} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$

$$O_b = \overline{OE} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$

$$O_c = \overline{OE} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$

$$O_d = \overline{OE} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

When the Output Enabler ($\overline{OE}$) is HIGH, the outputs are forced to a high impedance state. If the outputs are tied together, all but one device must be in the high impedance state to avoid high currents that would exceed the maxi-

mum ratings. Designers should ensure the Output Enable signals to TRI-STATE devices whose outputs are tied together are designed so there is no overlap.

Truth Table

Output Enable	Select Input	Data Inputs		Outputs
$\overline{OE}$	S	I_0	I_1	O
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

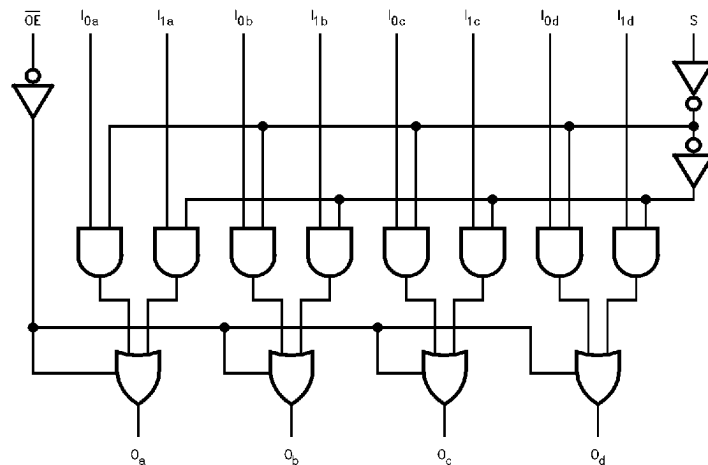
H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

Z = High Impedance

Logic Diagram



TL/F/11659-3

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−0.5V to +7.0V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Input Diode Current (I_{IK})	−20 mA
Output Diode Current (I_{OK})	±20 mA
DC Output Current (I_{OUT})	±25 mA
DC V_{CC} /GND Current (I_{CC})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Lead Temperature (T_L) (Soldering, 10 seconds)	260°C

Note 1: *Absolute Maximum Ratings* are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation outside databook specifications.

Recommended Operating Conditions

Supply Voltage (V_{CC})	2.0V to +5.5V
Input Voltage (V_{IN})	0V to +5.5V
Output Voltage (V_{OUT})	0V to V_{CC}
Operating Temperature (T_{OPR})	−40°C to +85°C
Input Rise and Fall Time (t_r, t_f)	
$V_{CC} = 3.3V \pm 0.3V$	0 ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ~ 20 ns/V

DC Characteristics for 'VHC Family Devices (Preliminary)

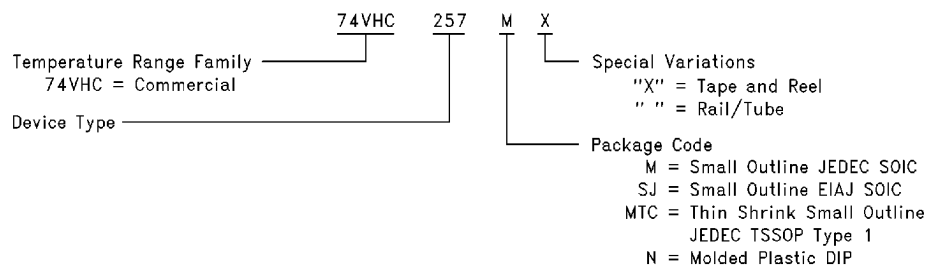
Symbol	Parameter	V _{CC} (V)	74VHC			74VHC		Units	Conditions	
			T _A = 25°C			T _A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
V _{IH}	High Level Input Voltage	2.0 3.0–5.5	1.50 0.7 V _{CC}			1.50 0.7 V _{CC}		V		
V _{IL}	Low Level Input Voltage	2.0 3.0–5.5	0.50 0.3 V _{CC}			0.50 0.3 V _{CC}		V		
V _{OH}	High Level Output Voltage	2.0	1.9	2.0		1.9		V	V _{IN} = V _{IH} or V _{IL}	I _{OH} = −50 μA
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4				
		3.0 4.5	2.58 3.94			2.48 3.80		V		I _{OH} = −4 mA I _{OH} = −8 mA
V _{OL}	Low Level Output Voltage	2.0	0.0			0.1		V	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA
		3.0	0.0			0.1				
		4.5	0.0			0.1				
		3.0 4.5	0.36 0.36			0.44 0.44		V		I _{OL} = 4 mA I _{OL} = 8 mA
I _{OZ}	TRI-STATE Output Off-State Current	5.5	±0.25			±2.5		μA	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND	
I _{IN}	Input Leakage Current	0–5.5	±0.1			±1.0		μA	V _{IN} = 5.5V or GND	
I _{CC}	Quiescent Supply Current	5.5	4.0			40.0		μA	V _{IN} = V _{CC} or GND	

AC Electrical Characteristics (Preliminary)

Symbol	Parameter	V _{CC} (V)	74VHC			74VHC		Units	Conditions	
			T _A = 25°C			T _A = −40°C to +85°C				
			Min	Typ	Max	Min	Max			
t _{PLH} , t _{PHL}	Propagation Delay I _n to O _n	3.3 ±0.3	6.2	9.7	1.0	11.5	ns		C _L = 15 pF	
			8.7	13.2	1.0	15.0			C _L = 50 pF	
		5.0 ±0.5	4.1	6.4	1.0	7.5	ns		C _L = 15 pF	
			5.6	8.4	1.0	9.5			C _L = 50 pF	
t _{PLH} , t _{PHL}	Propagation Delay S to O _n	3.3 ±0.3	8.4	13.2	1.0	15.5	ns		C _L = 15 pF	
			10.9	16.7	1.0	19.0			C _L = 50 pF	
		5.0 ±0.5	5.3	8.1	1.0	9.5	ns		C _L = 15 pF	
			6.8	10.1	1.0	11.5			C _L = 50 pF	
t _{PZL} , t _{PZH}	TRI-STATE Output Enable Time	3.3 ±0.3	8.7	13.6	1.0	16.0	ns	R _L = 1 kΩ	C _L = 15 pF	
			11.2	17.1	1.0	19.5			C _L = 50 pF	
		5.0 ±0.5	5.6	8.6	1.0	10.0	ns		C _L = 15 pF	
			7.1	10.6	1.0	12.0			C _L = 50 pF	
t _{PLZ} , t _{PHZ}	TRI-STATE Output Disable Time	3.3 ±0.3				ns	R _L = 1 kΩ	C _L = 50 pF		
		5.0 ±0.5				ns		C _L = 50 pF		
C _{IN}	Input Capacitance		4	10		10	pF	V _{CC} = Open		
C _{OUT}	Output Capacitance						pF	V _{CC} = 5.0V		
C _{PD}	Power Dissipation Capacitance		20				pF	(Note 1)		

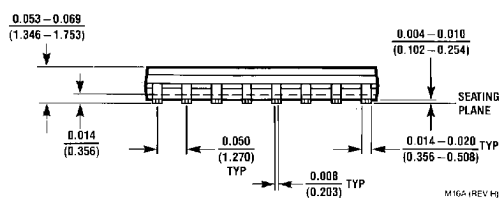
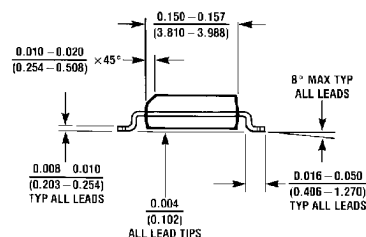
Note 1: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} * V_{CC} * f_{IN} + I_{CC}.

The device number is used to form part of a simplified purchasing code, where the package type and temperature range are defined as follows:



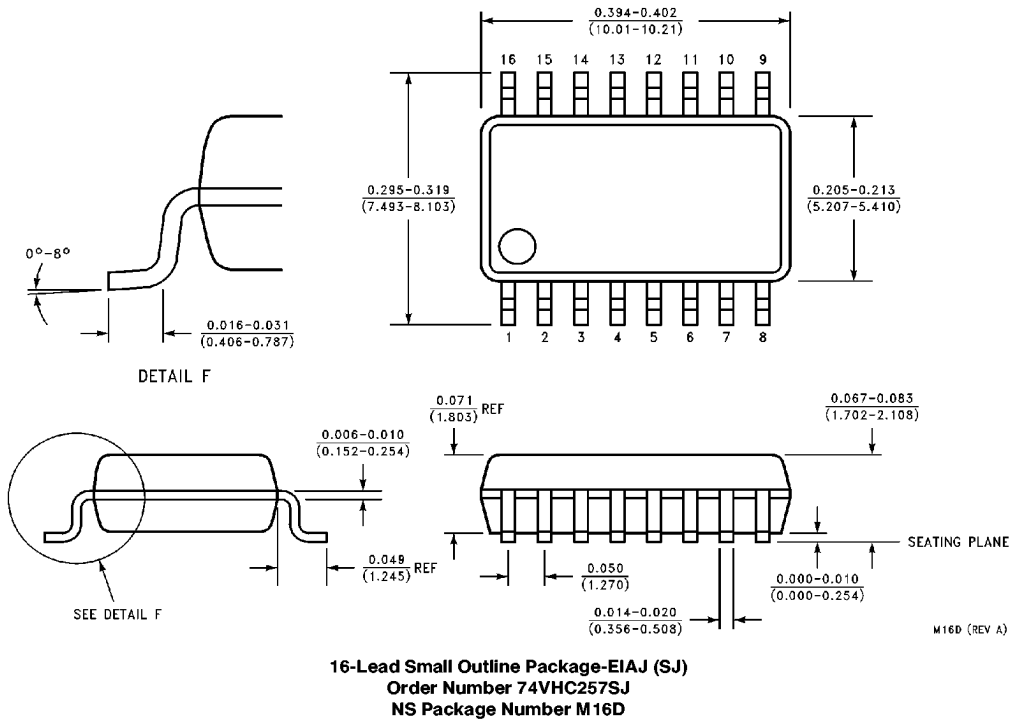
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Figure 1 is a top view of the test chip. The chip is rectangular with dimensions 0.386 - 0.394 (9.804 - 10.00) and 0.228 - 0.244 (5.791 - 6.196). It features 16 pins on the top edge (pins 16 to 9) and 8 pins on the bottom edge (pins 1 to 8). A 30° TYP angle is indicated for the bottom edge. A lead is labeled 'LEAD NO 1 IDENT'.

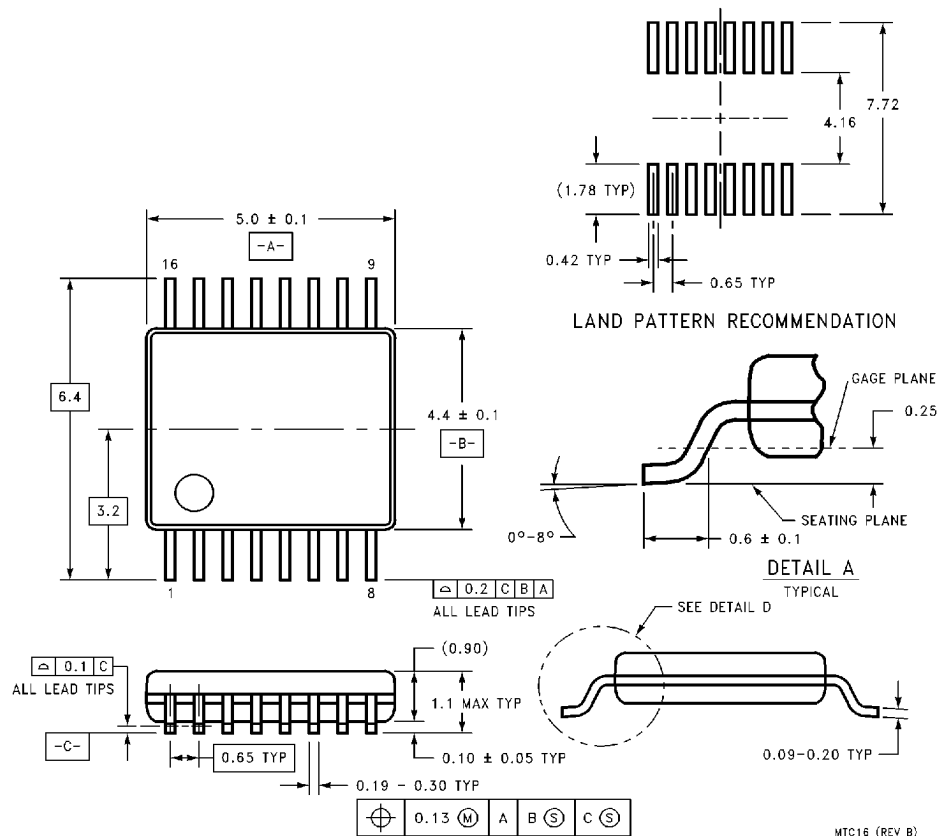


16-Lead Small Outline Integrated Circuit—JEDEC (M)
Order Number 74VHC257M
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



Physical Dimensions (millimeters) (Continued)

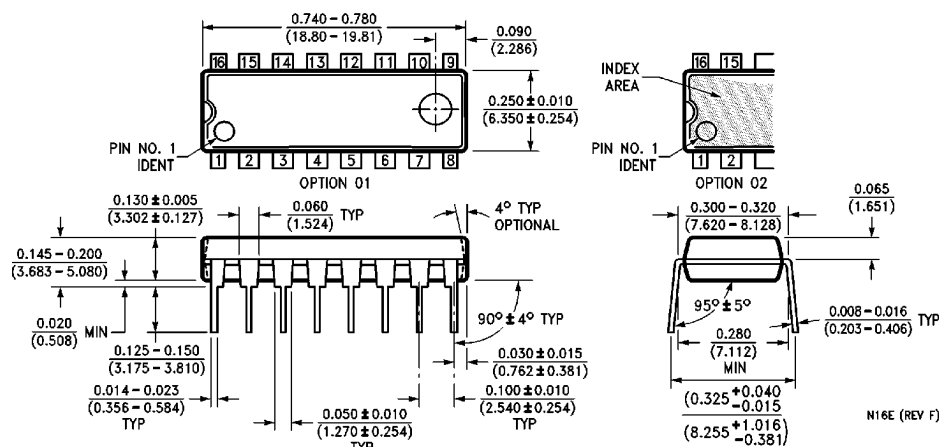


All dimensions are in millimeters.

**16-Lead Molded Thin Shrink Small Outline Package; JEDEC
Order Number 74VHC257MTC
NS Package Number MTC16**

MTC16 (REV B)

Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.300" Wide) Molded Dual-In-Line Package
Order Number 74VHC257N
NS Package Number N16E

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