REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add devices 03 and 04. Editorial changes throughout.	96-05-09	Monica Poelking
B	Changes in accordance with NOR 5962-R220-97	97-03-07	Monica Poelking
C	Changes in accordance with NOR 5962-R297-97	97-05-21	Monica Poelking
D	Add radiation features to 1.4 for device types 03 and 04. - LTG	97-12-08	Monica Poelking

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D						
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28						
REV STATUS OF SHEETS			REV			D	D	D	D	D	D	D	D	D	D	D	D	D	D	
			SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Christopher A. Rauch

CHECKED BY
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APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
94-05-02

REVISION LEVEL
D

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

MICROCIRCUIT, DIGITAL, BIPOLAR, DUAL CHANNEL, BUS TRANSCEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-93226**

SHEET 1 OF 28

DSCC FORM 2233
APR 97

5962-E263-97

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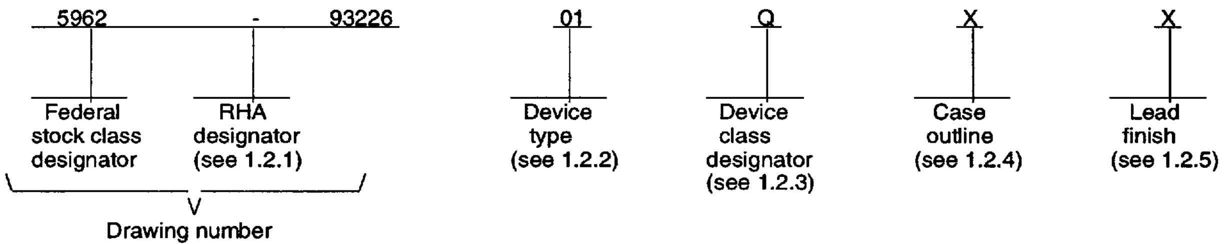
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT63M147	+5.0 V, dual channel bus transceiver (low idle) 1/
02	UT63M149	+5.0 V, dual channel bus transceiver (high idle) 1/
03	UT63M147E	+5.0 V, dual channel bus transceiver (low idle) 1/
04	UT63M145	+5.0 V, dual channel bus transceiver (low idle) 1/

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	36	dual-in-line
Z	See figure 1	24	flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Idle low: TXIN, $\overline{TXIN}$, $\overline{RXOUT}$, RXOUT are at logic 0.
Idle high: TXIN, TXIN, RXOUT, RXOUT are at logic 1.

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1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.3 V dc to +7.0 V dc
Input voltage range (receiver)	10 V_{PP}
Logic input voltage range	-0.3 V dc to +5.5 V dc
Output current (transmitter)	1.0 A
Power dissipation: 100% duty cycle (per channel) 3/	
device 01, 02	2.21 W
device 03, 04	3.6 W
Thermal impedance junction-to-case (Θ_{JC})	
device 01, 02	4.5 °C/W
device 03, 04	6.0 °C/W
Maximum junction temperature (T_J)	
device 01, 02	+125°C
device 03, 04	+175°C
Storage temperature range	-65°C to +150°C
Receiver common mode input voltage range	-5.0 V to +5.0 V

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	
device 01, 02	+4.75 V dc to +5.25 V dc
device 03, 04	+4.5 V dc to +5.5 V dc
Logic input voltage range	0.0 V dc to +5.0 V dc
Receiver differential voltage	8.0 Vpp
Receiver common mode voltage range	±4.0 V dc
Driver peak output current	
device 01, 02	700 mA
device 03, 04	600 mA
Serial data rate	
device 01, 02	0 to 1 MHz
device 03, 04	300 KHz to 1 MHz
Radiation features:	
Total dose	1 x 10^6 Rads (Si)
Single event phenomenon (SEP) effective linear energy threshold, no upsets or latchup (see 4.4.4.5)	> 35 MeV/(mg/cm2)
Dose rate upset (20 ns pulse)	4/
Dose rate latchup	4/
Dose rate survivability	4/
Neutron irradiated	> 1 x 10^{14}
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent 5/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ V_{CC} = 5.0 V, T_C = +25°C.
4/ When characterized as a result of the procuring activities request, the condition will be specified.
5/ Fault coverage is for digital circuits only.

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SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1553 - Aircraft Internal Time Division Command/Response Multiplex Databus.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements for microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 132 (see MIL-PRF-38535, appendix A).

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ 2/ Min $\le V_{CC} \le$ Max, GND=0.0V unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Input low voltage RXEN, TXIHB, TXIN, $\overline{\text{TXIN}}$	V_{IL}		1,2,3	01,02		0.65	V
				03,04		0.8	
Input high voltage RXEN, TXIHB, TXIN, $\overline{\text{TXIN}}$	V_{IH}			All	2.0		
Input low current RXEN, TXIHB, TXIN, $\overline{\text{TXIN}}$	I_{IL}	V_{IL} = 0.4 V		01, 02	-1.1		mA
				03, 04	-0.1		
Input high current RXEN, TXIHB, TXIN, $\overline{\text{TXIN}}$	I_{IH}	V_{IH} = 2.7 V		All	-40	40	µA
Transmitter inhibit input current, TXIHB	I_{IIH}	V_{IH} = 2.7 V		01, 02		100	µA
Output low voltage RXOUT, $\overline{\text{RXOUT}}$	V_{OL}	I_{OL} = 4 mA		01, 02		0.65	V
				03, 04		0.55	
Output high voltage RXOUT, $\overline{\text{RXOUT}}$	V_{OH}	I_{OH} = 0.4 mA		01, 02	2.4		
				03, 04	2.4		
V_{CC} supply current	I_{CC}	0% duty cycle (non-trans.) 25% duty cycle (f = 1 MHz) 50% duty cycle (f = 1 MHz) 87.5% duty cycle (f = 1 MHz) 100% duty cycle (f = 500 Khz)	1, 2, 3	01, 02		55 300 500 800 800 [3]	mA
V_{CC} supply current	I_{CC}	0% duty cycle (non-trans.) 25% duty cycle (f = 1 MHz) 50% duty cycle (f = 1 MHz) 87.5% duty cycle (f = 1 MHz) 100% duty cycle (f = 1 MHz)	1, 2, 3	03, 04		22 190 360 590 680 [3]	mA
Functional tests		See 4.4.1b	7, 8	All			
RECEIVER							
Input capacitance RXEN, TXIN, $\overline{\text{TXIN}}$, TXIHB	C_{IN}	f = 1 MHz sinewave see 4.4.1c	4,5,6	All		15	pF

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ 2/ $Min \le V_{CC} \le Max$, GND=0.0V unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Common mode input voltage 3/	V_{IC}	f = 1 MHz, Direct-coupled stub; input 1.2 V_{PP} 200 ns rise/fall ±25 ns	4,5,6	All	-5.0	5.0	V
Input threshold voltage (no response) 3/	V_{TH1}	f = 1 MHz,Transformercoupled stub; rise/fall 200 ns at (receiver output 0 to 1 transition)				0.20	V_{PP}, L-L
Input threshold voltage (no response)	V_{TH2}	f = 1 MHz, Direct-coupled stub; rise/fall 200 ns at (receiver output 0 to 1 transition)				0.28	
Input threshold voltage (response) 3/	VTH3	f = 1 MHz,Transformercoupled stub; rise/fall 200 ns at (receiver output 0 to 1 transition)			0.86	14.0	
Input threshold voltage (response)	V_{TH4}	f = 1 MHz, Direct-coupled stub; rise/fall 200 ns at (receiver output 0 to 1 transition)			1.20	20.0 3/	
Common mode rejection 3/	CMRR	Pass/Fail 4/					
Differential input voltage level 3/	V_{IDR}					8.0	V_{P-P}
TRANSMITTER							
Output voltage swing MIL-STD-1553B 3/ transformer-coupled stub	V_{O1}	f = 1 MHz, R_L = 70 Ω See figure 4, point A	4,5,6	01 -03	18	27	V_{PP}, L-L
Output voltage swing MIL-STD-1760 transformer-coupled stub	V_{O1}	f = 1 MHz, R_L = 70 Ω See figure 4 point A Tested by Direct-Coupled 7 V - 9 V		04	22	27	V_{PP}, L-L
Output voltage swing MIL-STD-1553B direct-coupled stub,	V_{O2}	f = 1 MHz, R_L = 35 Ω See figure 4 point A		01- 03	6	9	V_{PP}, L-L
Output voltage swing 3/ MIL-STD-1553A transformer-coupled stub	V_{O3}	f = 1 MHz, R_L = 35 Ω See figure 4 point A		01- 03	6	20	V_{PP}, L-L

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ 1/ 2/ Min $\leq V_{CC} \leq$ Max, GND=0.0V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output noise voltage differential Transformer coupled stub 3/	V_{NS1}	f = DC to 10 MHz $R_L = 70\ \Omega$ See figure 4 point A	4,5,6	All		14	mV-RMS L-L
Output noise voltage differential Direct 3/ coupled stub	V_{NS2}	f = DC to 10 MHz $R_L = 35\ \Omega$ See figure 4 point A		01, 02 03, 04		10 5	
Output symmetry 3/ Transformer-coupled stub	V_{OS1}	$R_L = 140\ \Omega$ See figure 4 point A measurement taken 2.5 μs after end of transmission		01, 02 03, 04	-360 -250	+360 +250	mV_{PP}, L-L
Output symmetry 3/ Direct-coupled stub	V_{OS2}	$R_L = 35\ \Omega$ See figure 4 point A measurement taken 2.5 μs after end of transmission		All	-90	+90	mV_{PP}, L-L
Output voltage distortion (overshoot or ring) 3/ Transformer-coupled stub	V_{DIS1}	$R_L = 70\ \Omega$ See figure 4 point A		01, 02 03, 04	-2.0 -0.9	+2.0 +0.9	$V_{PEAK, L-L}$
Output voltage distortion (overshoot or ring) Direct-coupled stub	V_{DIS2}	$R_L = 35\ \Omega$ See figure 4 point A		01, 02 03, 04	-1.0 -0.3	+1.0 +0.3	V_{PEAK}, L-L
Output capacitance RXOUT, RXOUT	C_{OUT}	f = 1 MHz sinewave See 4.4.1c		All		20	pF
Terminal input impedance Transformer-coupled stub 3/	T_{IZ1}	f = 75 KHz to 1 MHz (power on or power off; non-transmitting, R_L removed from circuit			1		kΩ
Terminal input impedance Direct-coupled stub 3/	T_{IZ2}	f = 75 KHz to 1 MHz (power on or power off; non-transmitting, R_L removed from circuit			2		kΩ
Differential output impedance 3/	T_{OZ}	f = 1 MHz		01, 02	10		kΩ

See footnotes at end of table.

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TABLE IA. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ 1/ 2/ Min $\le V_{CC} \le$ Max, GND=0.0V unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Transmitter output rise and fall time Direct-coupled	t_r, t_f	f = 1 MHz 50% duty cycle $R_L = 35\ \Omega$ output at 10% through 90% points TXOUT, TXOUT	9,10,11	All	100	300	ns
RXOUT delay	t_{RXDD}	RXOUT to $\overline{RXOUT}$			-200	200	
TXIN skew 3/	t_{TXDD}	TXIN to $\overline{TXIN}$		01, 02 03, 04	-15 -25	15 25	
Zero crossing distortion Direct-coupled stub	t_{RZCD}	f = 1 MHz, 3.0 V_{PP}, skew input ±150 ns, rise/fall time=200 ns	9,10,11	All	-150	+150	ns
Zero crossing stability Input TXIN and TXIN should create transmitter output zero crossings at 500, 1000, 1500 and 2000 ns	t_{TZCS}	R_L = 35 ohms See figure 4 point A Zero crossings should not deviate more than ± 25 ns			-25	+25	
Transmitter off; delay from inhibit active 3/ 5/	t_{RDXOFF}	See figure 4 point A TXIN and TXIN toggling 1 MHz TXIHB transitions from logic zero to one		01, 02 03, 04		450 100	
Transmitter on; delay from inhibit inactive 3/ 6/	t_{DXON}	See figure 4 point A TXIN and TXIN toggling 1 MHz TXIHB transitions from logic one to zero		01, 02 03, 04		250 150	
Receiver off 3/	t_{RCVOFF}	See figure 4 point A Receiver turn off time		01, 02 03, 04		200 50	
Receiver on 3/	t_{RCVON}	See figure 4 point A Receiver turn on time		01, 02 03, 04		200 50	
Receiver propagation 3/	t_{RCVPD}	See figure 4 point A Receiver propagation delay		01, 02 03, 04		600 450	
3/ Transmitter propagation	t_{XMITPD}	See figure 4 point A Transmitter propagation delay		01, 02 03, 04		450 200	

1/ Device types 03 and 04 supplied to this drawing have been characterized through all levels M, D, L, R, F, G, and H of irradiation. However, this device is only tested at the 'H' level. Pre and Post irradiation values are identical unless otherwise specified in Table IA. When performing post irradiation electrical measurements for any RHA level, $T_A = +25°C \pm 5°C$. All parameters are tested to worst case conditions unless otherwise specified.
2/ Unless otherwise specified, all testing shall be conducted under worst-case conditions. GND may not vary from 0.0 Vdc by more than ±50 mV. L-L = line to line. V_{CC} max and mins are as specified in 1.4 herein.
3/ Guaranteed to the limits specified in table I, if not tested.
4/ Pass/fail criteria per the test method described in MIL-HDBK-1553 appendix A.
5/ Delay time from transmit inhibit (1.5 V) to transmit off (280 mV).
6/ Delay time from NOT transmit inhibit (1.5 V) to transmit off (1.2 V).

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TABLE IB. SEP test limits. 1/ 2/

Device type	T_A = Temperature ±10°C 3/	V_{DD} = 4.5 V		Bias for latch-up test V_{DD} = 5.5 V no latch-up LET = 3/
		Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section	
03,04	+25°C	LET > 11.4	2.5×10^{-6} cm^2	> 35

1/ For SEP test conditions, see 4.4.4.5.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ Worst case temperature T_A = +125°C.

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Case X

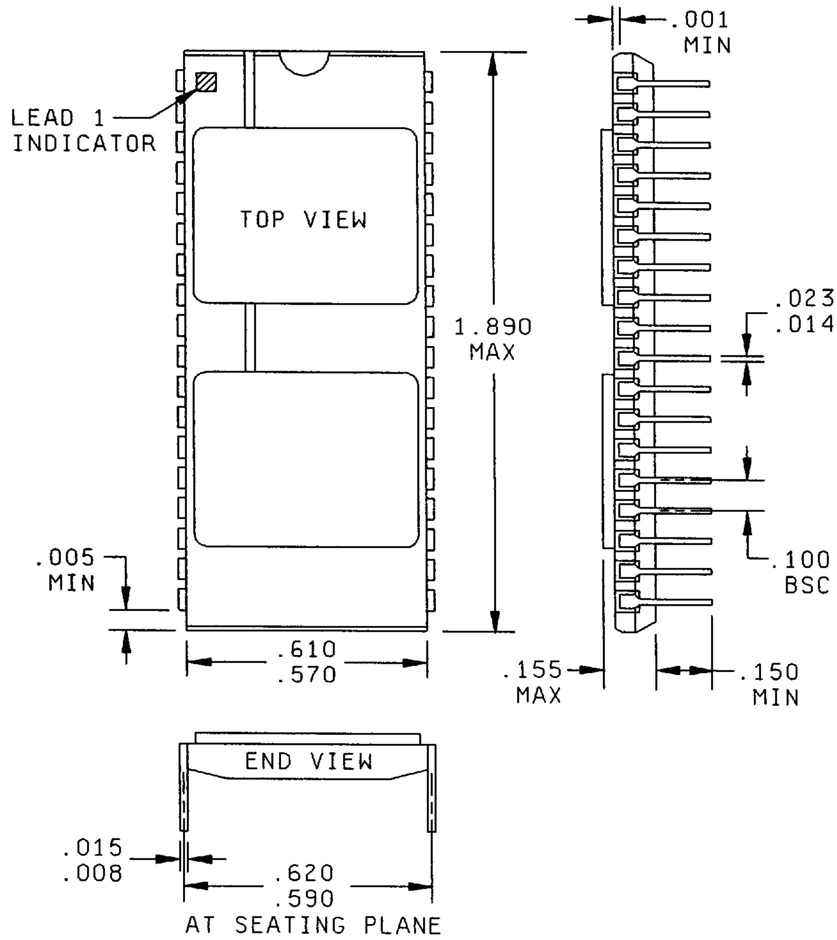

FIGURE 1. Case outline.

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Case Z

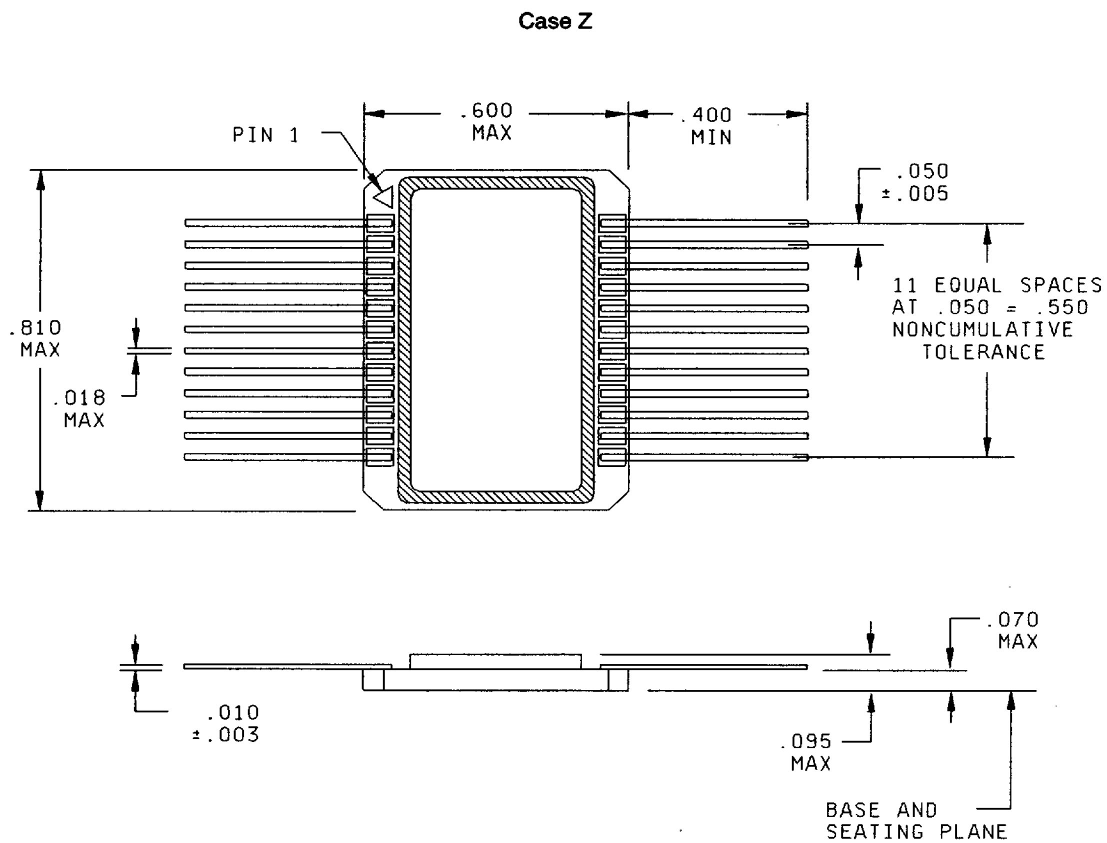

FIGURE 1. Case outline. - Continued.

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Device types	All			
Case outlines	X		Z	
Terminal number	Terminal symbol	Channel	Terminal symbol	Channel
1	TXOUT	A	TXOUT/RXIN	A
2	TXOUT	A	TXOUT/RXIN	A
3	GND	A	GND	A
4	NC		RXOUT	A
5	RXOUT	A	RXEN	A
6	RXEN	A	RXOUT	A
7	GND	A	TXOUT/RXIN	B
8	RXOUT	A	TXOUT/RXIN	B
9	NC		GND	B
10	TXOUT	B	RXOUT	B
11	TXOUT	B	RXEN	B
12	GND	B	RXOUT	B
13	NC		GND	B
14	RXOUT	B	V_{CC}	B
15	RXEN	B	GND	B
16	GND	B	TXIHB	B
17	RXOUT	B	TXIN	B
18	NC		TXIN	B
19	NC		GND	A
20	RXIN	B	V_{CC}	A
21	RXIN	B	GND	A
22	GND	B	TXIHB	A
23	NC		TXIN	A
24	V_{CC}	B	TXIN	A
25	TXIHB	B	---	---
26	TXIN	B	---	---
27	TXIN	B	---	---
28	NC		---	---
29	RXIN	A	---	---
30	RXIN	A	---	---
31	GND	A	---	---
32	NC		---	---
33	V_{CC}	A	---	---
34	TXIHB	A	---	---
35	TXIN	A	---	---
36	TXIN	A	---	---

FIGURE 2. Terminal connections.

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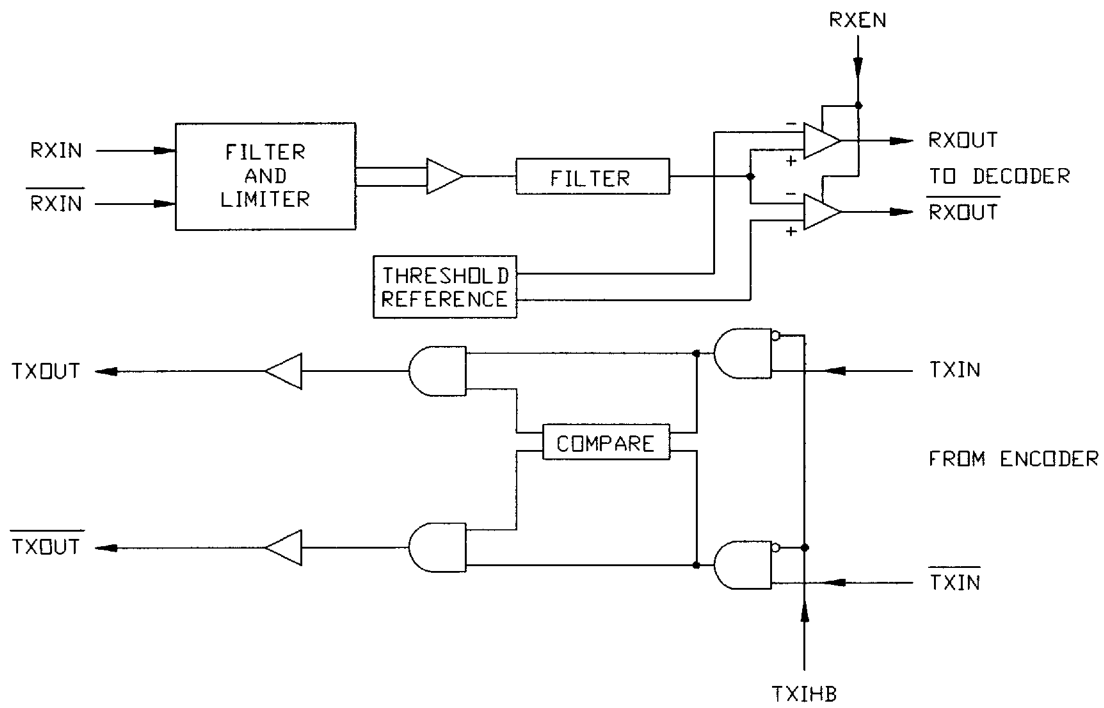

FIGURE 3. Block diagram.

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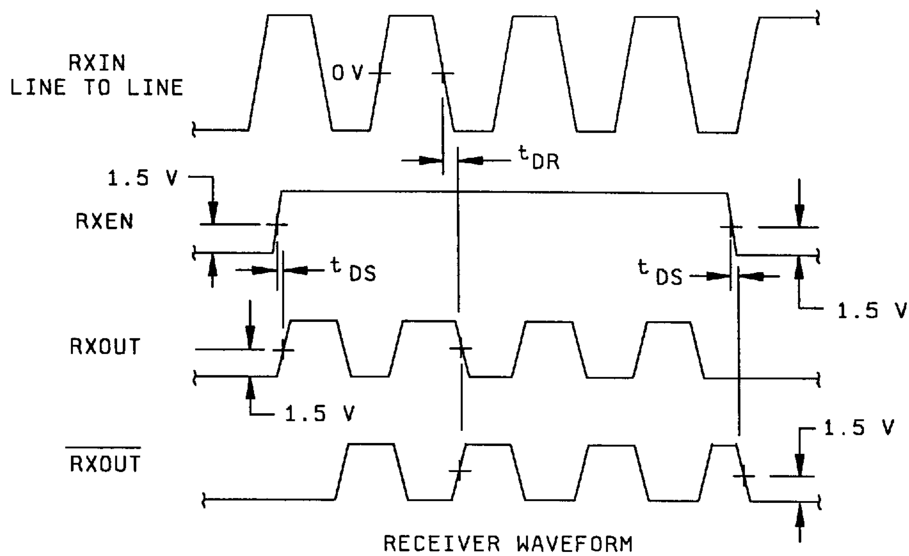

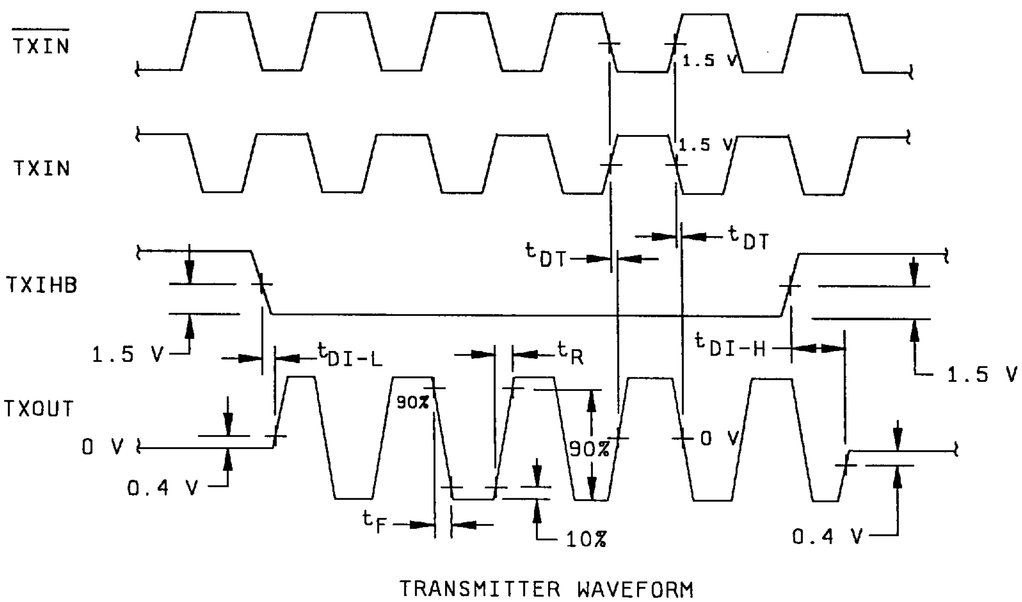

t_{DR} = Receiver delay
t_{DS} = Receiver enable/disable

t_{DI-L} = Inhibited delay
t_{DI-H} = Active output

t_R = Rise time

FIGURE 4. Timing waveforms.

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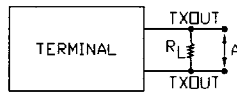
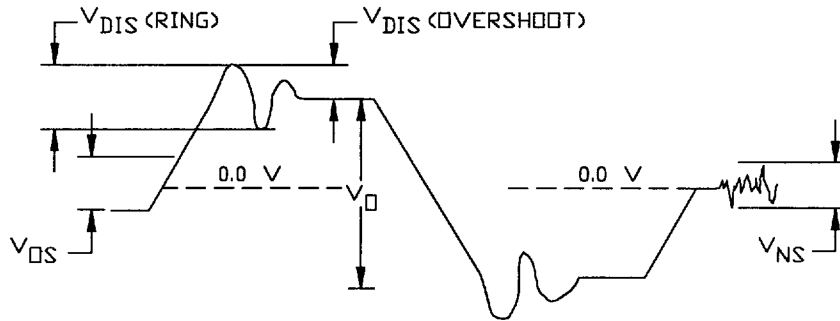
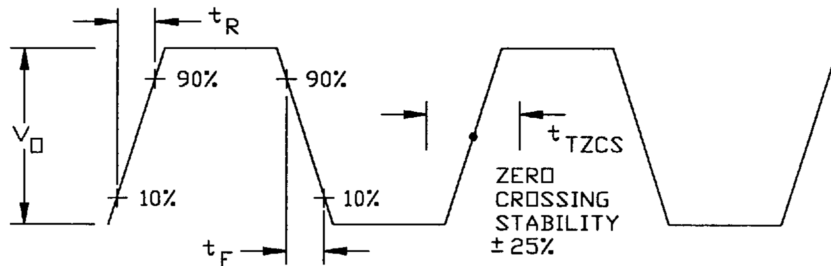
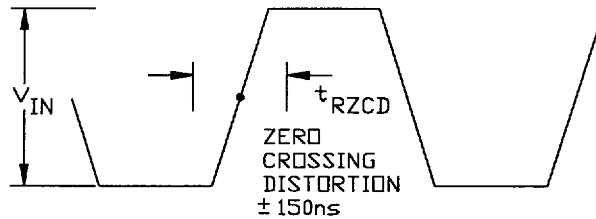




TRANSMITTER OUTPUT CHARACTERISTICS



TRANSMITTER OUTPUT ZERO CROSSING STABILITY



RECEIVER INPUT ZERO CROSSING DISTORTION

FIGURE 4. Timing waveforms - continued.

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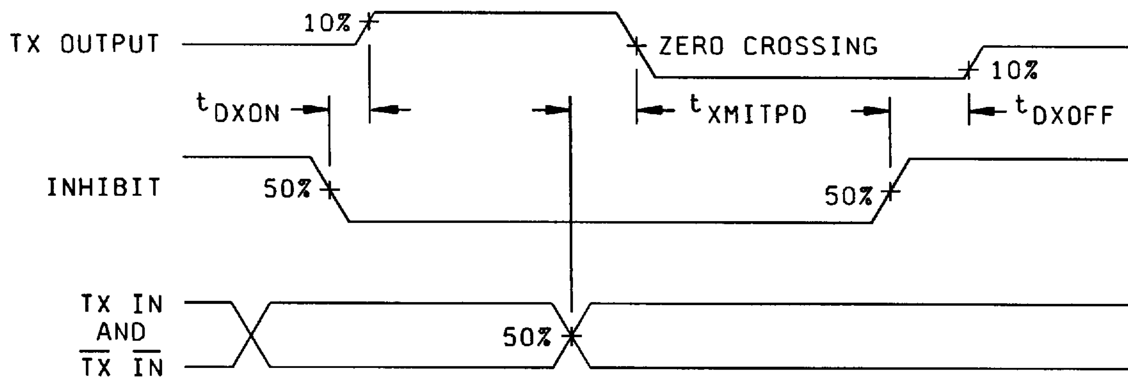

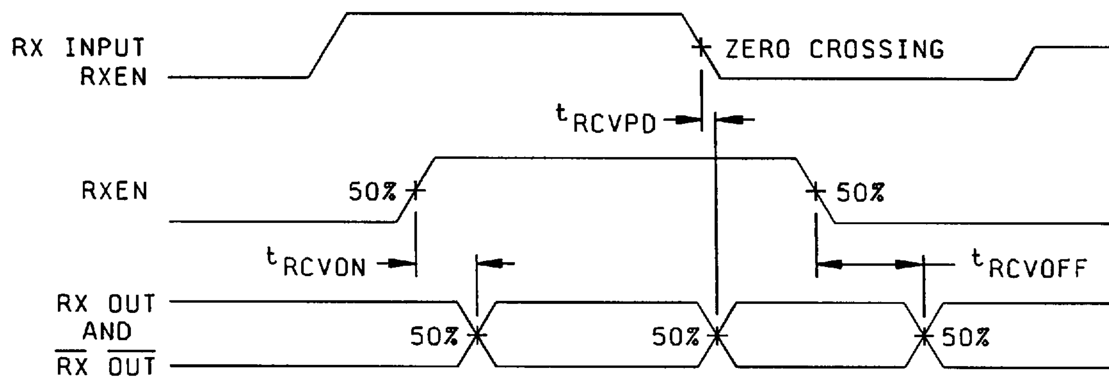

FIGURE 4. Timing waveforms - continued.

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Signal	Bias	Pin	Pin	Bias	Signal
A TXOUT	N/C	1	36	+5 V	A $\overline{\text{TXIN}}$
A $\overline{\text{TXOUT}}$	N/C	2	35	GND	A TXIN
A GND	GND	3	34	+5 V	A TXINB
N/C	N/C	4	33	+5 V	+5 V
A RXOUT	N/C	5	32	-15 V	N/C
A RXEN	GND	6	31	GND	A GND
A GND	GND	7	30	GND	A $\overline{\text{RXIN}}$
A $\overline{\text{RXOUT}}$	N/C	8	29	GND	A RXIN
N/C	N/C	9	28	+15 V	N/C
B TXOUT	N/C	10	27	+5 V	B $\overline{\text{TXIN}}$
B $\overline{\text{TXOUT}}$	N/C	11	26	GND	B TXIN
B GND	GND	12	25	+5 V	B TXINB
N/C	N/C	13	24	+5 V	+5 V
B RXOUT	N/C	14	23	-15 V	N/C
B RXEN	GND	15	22	GND	B GND
B GND	GND	16	21	GND	B $\overline{\text{RXIN}}$
B $\overline{\text{RXOUT}}$	N/C	17	20	GND	B RXIN
N/C	N/C	18	19	+15 V	N/C

Figure 5. Radiation exposure circuit

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and C_{OUT}) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,4,9	1,4,9	1,4,9
Final electrical parameters (see 4.2)	1,2,3,4,5,6,7,8,9, 10,11 1/	1,2,3,4,5,6, 7,8,9,10,11 1/	1,2,3,4,5,6,7, 8,9,10,11 2/ 3/
Group A test requirements (see 4.4)	1,2,3,4,5,6,7,8,9, 10,11	1,2,3,4,5,6, 7,8,9,10,11	1,2,3,4,5,6,7, 8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3 3/
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,4,9	1,4,9	1,4,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits are as specified in Table IIB herein and shall be required where specified and the delta values shall be completed with reference to the zero hour electrical parameters (see table I).

Table IIB. Burn-in delta parameters (+25°C).

Test	Symbol	Conditions	Limit
Supply Current	I_{CC}	0% Duty Cycle, $V_{DD} = 4.5$ V	±0.15 mA or 1% whichever is greater.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or C. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125° C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Neutron testing. Neutron testing shall be performed in accordance with test method 1017 of MIL-STD-883 and herein. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table I, for the subgroups specified in Table IIA herein at T_A = +25°C ± 5°C after an exposure of 2 x 10^{12} neutrons/cm^2 (minimum).

4.4.4.3 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.4 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.5 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see Table IB herein.

4.4.4.6 Dose rate burnout. When required by the customer test shall be performed on devices, SEC, or approved test structures at technology qualifications and after any design or process changes which may effect the RHA capability of the process. Dose rate burnout shall be performed in accordance with test method 1023 of MIL-STD-883 and as specified herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000 or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

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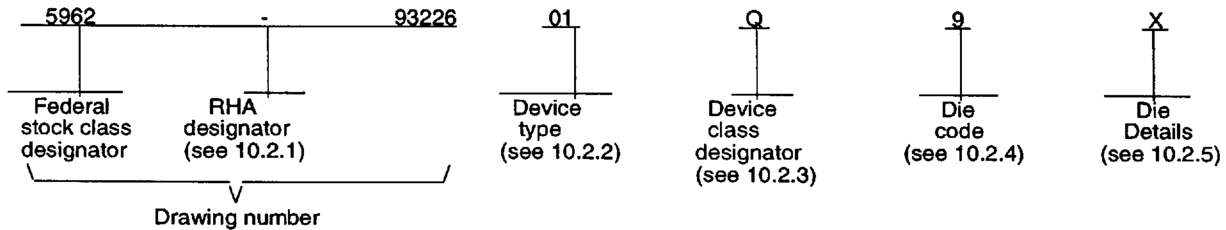
Appendix A

APPENDIX A FORMS A PART OF SMD 5962-93226

10. SCOPE

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2 PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UT63M147	+5.0 V, dual channel bus transceiver (low idle) 1/
02	UT63M149	+5.0 V, dual channel bus transceiver (high idle) 1/
03	UT63M147E	+5.0 V, dual channel bus transceiver (low idle) 1/
04	UT63M145	+5.0 V, dual channel bus transceiver (low idle) 1/

10.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5. Die Details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Die type	Figure number
03	A-1

1/ Idle low: TXIN, $\overline{\text{TXIN}}$, RXOUT, $\overline{\text{RXOUT}}$ are at logic 0.

Idle high: TXIN, $\overline{\text{TXIN}}$, $\overline{\text{RXOUT}}$, RXOUT are at logic 1.

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10.2.5.2. Die bonding pad locations and electrical functions.

Die type	Figure number
03	A-1

10.2.5.3. Interface materials.

Die type	Figure number
03	A-1

10.2.5.4. Assembly related information.

Die type	Figure number
03	A-1

10.3. Absolute maximum ratings.

See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions.

See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specifications, standards, bulletin, and handbooks. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

HANDBOOK

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity).

20.2. Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

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Appendix A

APPENDIX A FORMS A PART OF SMD 5962-93226

30. REQUIREMENTS

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physucal dimensions. The die physical dimensions shall be as specified in 10.2.5.1 and on figures A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figures A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figures A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figures A-1.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not effect the form, fit or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria defined within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4).

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

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40.3 Conformance inspection

40.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein.

50. Die carrier

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60 NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0674.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-STD-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

Die bonding pad locations and electrical functions

Die physical dimensions.
Die size: 171 mils x 187mils.
Die thickness: 17.5 ±1 mils.

Interface materials.
Top metallization: Si Al Cu 9 kA-12.5 kA
Backside metallization: None: Backgrind

Glassivation.
Type: PSG with Nitride
Thickness: 10 kA / ±1 kA

Substrate: Dielectrically isolated

Assembly related information.
Substrate potential: float/isolate die attach pad
Special assembly instructions: TXOUT and $\overline{TXOUT}$ bond out must be matched within 10 mΩ and have low resistance of less than 250 mΩ. V_{CC} bond out on bond pads 1, 2, 3 and 22, 23, 24 must be within 10 mΩ and have low resistance of less than 250 mΩ.

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Appendix A

Die bonding pad locations and electrical functions

PAD	XCENTER	YCENTER	PAD NAME
1	0.0635	0.0790	V_{CC}
2	0.0545	0.0790	V_{CC}
3	0.0435	0.0770	V_{CC}
4	0.0315	0.0790	GND
5	0.0025	0.0790	V_{CC}
6	-0.0119	0.0791	N/C
7	-0.0275	0.0770	GND
8	-0.0397	0.0772	RXOUT
9	-0.0564	0.0772	RXEN
10	-0.0715	0.0790	GND
11	-0.0867	0.0791	$\overline{RXOUT}$
12	-0.0875	0.0350	V_{CC}
13	-0.0886	0.0258	GND
14	-0.0885	-0.0450	$\overline{RXIN}$
15	-0.0885	-0.0550	RXIN
16	-0.0705	-0.0780	V_{CC}
17	-0.0325	-0.0790	V_{CC}
18	-0.0175	-0.0790	TXIN
19	-0.0076	-0.0779	$\overline{TXIN}$
20	0.0032	-0.0783	THIHB
21	0.0315	-0.0790	GND
22	0.0402	-0.0769	V_{CC}
23	0.0565	-0.0780	V_{CC}
24	0.0635	-0.0780	V_{CC}
25	0.0865	-0.0640	TXOUT
26	0.0865	-0.0210	TXOUT
27	0.0885	-0.0010	TXOUT
28	0.0885	0.0070	$\overline{TXOUT}$
29	0.0855	0.0300	$\overline{TXOUT}$
30	0.0855	0.0600	$\overline{TXOUT}$

NOTE:

1. The die center is the coordinate origin (0,0).

Figure A-1

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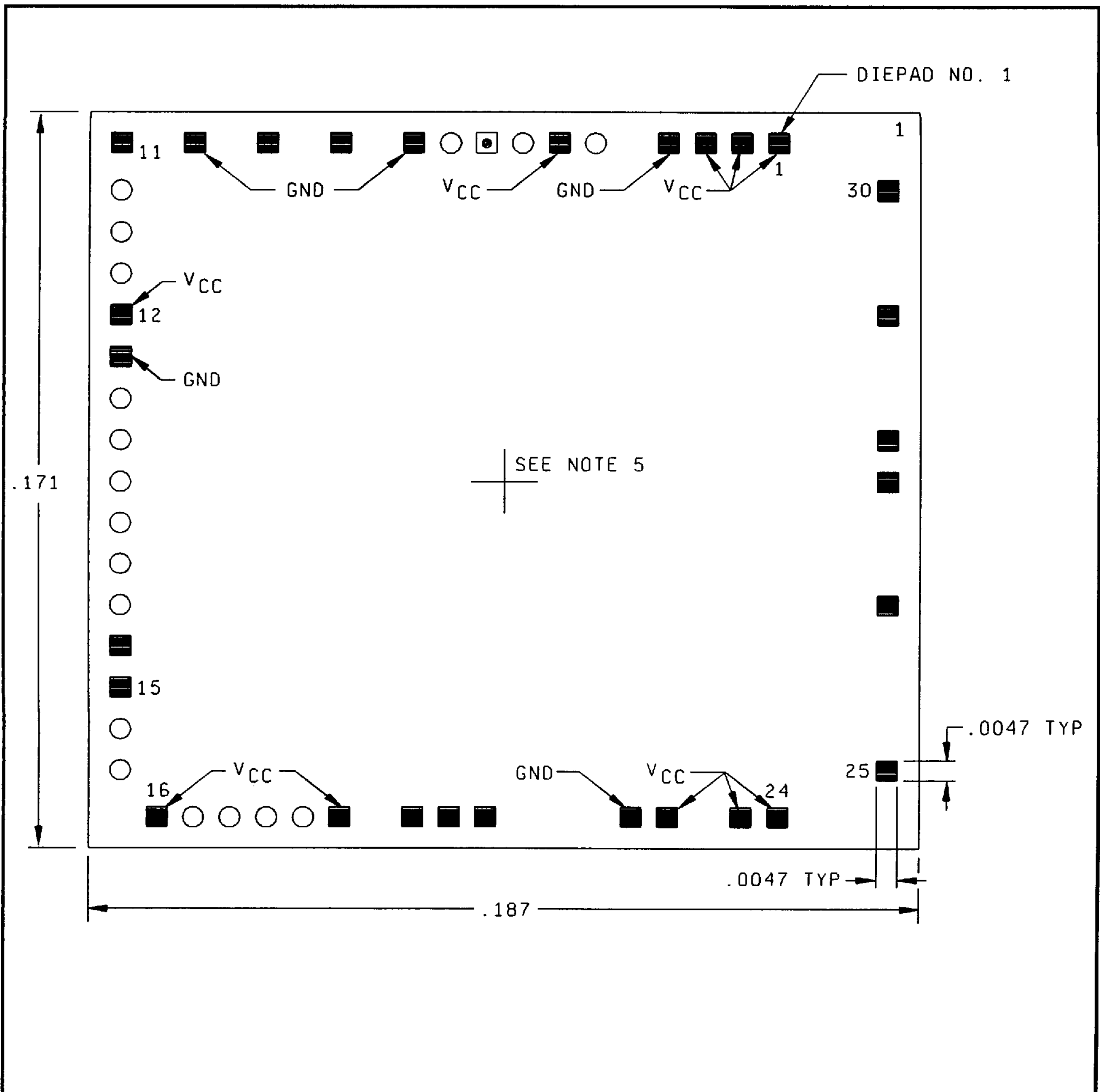

NOTES:

1. All dimensions are in inches and are basic.
2. Backside bias is GND.
3. Die thickness is 0.0175 ±0.001.
4. Die backside is lapped.
5. The die center is the coordinate origin (0,0).
6. Only the square diepads are numbered. The filled diepads are used.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-12-08

Approved sources of supply for SMD 5962-93226 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9322601MXA	65342	UT63M147BBA
5962-9322601MZA	65342	UT63M147CBA
5962-9322602MXA	65342	UT63M149BBA
5962-9322602MZA	65342	UT63M149CBA
5962-9322603QXA	65342	UT63M147EBQA
5962-9322603QZA	65342	UT63M147ECQA
5962-9322603QXC	65342	UT63M147EBQC
5962-9322603QZC	65342	UT63M147ECQC
5962H9322603VXA	65342	UT63M147EBVA
5962H9322603VZA	65342	UT63M147ECVA
5962H9322603VXC	65342	UT63M147EBVC
5962H9322603VZC	65342	UT63M147ECVC
5962H9322603Q9A	65342	UT63M147E-Q DIE
5962H9322603V9A	65342	UT63M147E-V DIE

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9322604QXA	65342	UT63M145BQA
5962-9322604QZA	65342	UT63M145CQA
5962-9322604QXC	65342	UT63M145BQC
5962-9322604QZC	65342	UT63M145CQC
5962H9322604VXA	65342	UT63M145BVA
5962H9322604VZA	65342	UT63M145CVA
5962H9322604VXC	65342	UT63145BVC
5962H9322604VZC	65342	UT63145CVC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronic Systems Inc. 4350 Centennial Boulevard Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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