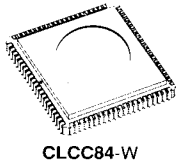
SGS-THOMSON MICROELECTRONICS

ST90E54
ST90T54

32K EPROM HCMOS MCUs WITH BANKSWITCH AND A/D CONVERTER

ADVANCE DATA

- Single chip microcontroller with 32K bytes of EPROM, 1,280 bytes of static RAM and 256 bytes of register file with 224 general purpose registers available as RAM, accumulators or index pointers.
- Bank-Switch logic allowing a maximum addressing capability of 8M bytes in both program and data spaces (16M byte total).
- 8/16 bit CORE with full feature DMA controller, a powerful interrupt handler and a Standard Serial Peripheral Interface (SPI) handling S-bus, I²C-bus, IM-bus and Standard Serial Peripheral Interfaces.
- Up to 8 external interrupts edge-selectable plus 1 non-maskable interrupt.
- 16 bit programmable Timer with 8 bit Prescaler, able to be used as a Watchdog Timer for system integrity.
- Three 16 bit Multifunction Timer modules, each with an 8 bit prescaler and 13 operating modes, allowing simple use for complex waveform generation and measurement, PWM functions and many other system timing operations.
- 8 channel Analog to Digital Converter, with integral sample and hold, fast 11µs conversion time, 8 bit ±1/2 LSB resolution with Analog Watchdog on two channels.
- Two full function Serial Communications Interfaces with 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and address/wake-up bit option.
- On-chip DMA channels associated to the Multifunction Timers and the Serial Communications Interface.
- Up to nine 8 bit I/O ports with programmable input thresholds and output characteristics. Alternative functions allow the full use of all pins.
- Powerful software development tools, including assembler, linker, C-compiler, archiver, software and hardware emulators.
- 84-lead Window Ceramic Leaded Chip Carrier package for ST90E54.
- 84-lead Plastic Leaded Chip Carrier package for ST90T54.



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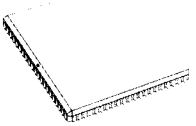

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(Ordering Information at the end of the datasheet)

Figure 1. ST90E54 Block Diagram

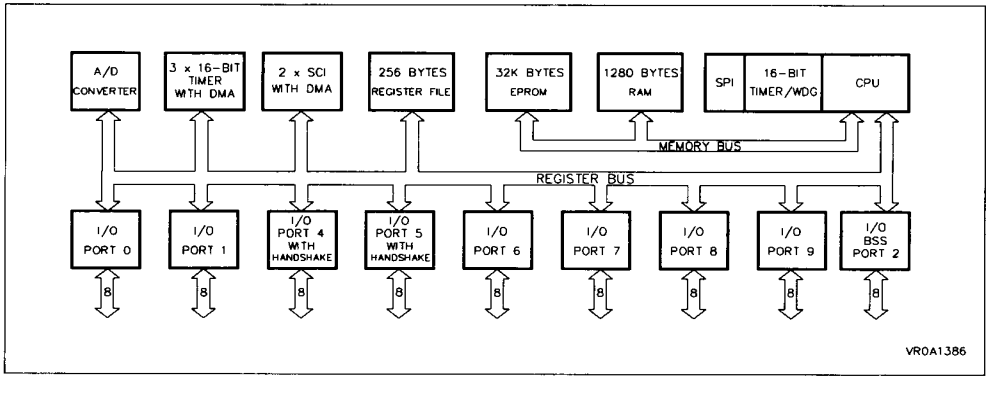
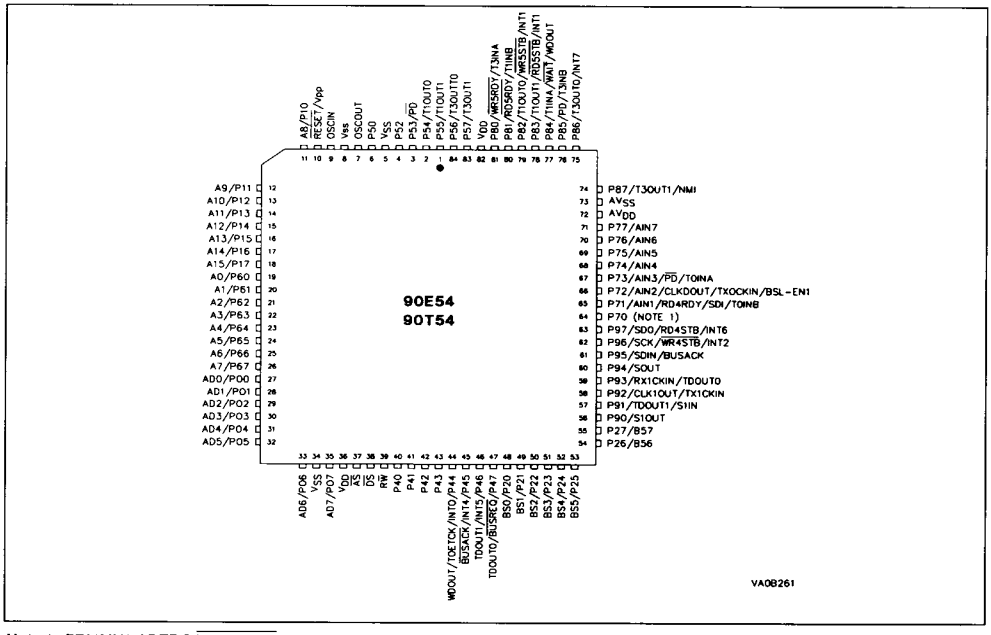


Figure 2. ST90E54,T54 Pin Configuration



Note 1 : P70/AIN0/ADTRG/$\overline{WR4DRDY}$/RX0CKIN/WDIN/BSH_EN1.

GENERAL DESCRIPTION

The ST90E54 and ST90T54 (following mentioned as ST90E54) are EPROM members of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a proprietary n-well HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9054 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E54 may be used for the prototyping and pre-production phases of development, and can be configured as: standalone microcontrollers with 32K bytes of on-chip EPROM, microcontrollers able to manage up to 120K bytes of external memory, (16M byte with the Bankswitch logic), or as parallel processing elements in a system with other processors and peripheral controllers.

A key point of the ST90E54 architecture is its modular approach which allows software commonality with all other members of the ST9 family.

The nucleus of the modular design of the ST90E54 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

GENERAL DESCRIPTION (Continued)

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E54 with up to 72 I/O lines dedicated to digital Input/Output. These lines are grouped into up to nine 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, address and data buses for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (internal and external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Three 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other system timing functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit ±1/2 LSB resolution. An Analog Watchdog feature is included for two input channels.

Completing the device are two full duplex Serial Communications Interfaces, each with an integral 110 to 375000 baud rate generator, asynchronous and byte synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0, Port 1, Port 6, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST90E54 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. The timing of R/$\overline{W}$ may be modified when using the Bank Switch Logic memory expansion to prevent external timing conflicts. R/$\overline{W}$ can be placed in a high impedance state along with Port 0, Port 1, Port 6, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input VPP.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter.

V_{DD}. Main Power Supply Voltage (5V±10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7, P4.0-P4.7, P5.0-P5.7, P6.0-P6.7, P7.0-P7.7, P8.0-P8.7, P9.0-P9.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 8 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as Alternate functions (see next section).

I/O Port Alternate Functions.

Each pin of the I/O ports of the ST90E54 may assume software programmable Alternative Functions as shown in the Pin Configuration Drawings. Table 1 shows the Functions allocated to each I/O Port pins.

PIN DESCRIPTION (Continued)

Table 1. ST90E54,T54 I/O Port Alternate Function Summary

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P0.0	A0/D0	I/O	Address/Data bit 0 mux	27
P0.1	A1/D1	I/O	Address/Data bit 1 mux	28
P0.2	A2/D2	I/O	Address/Data bit 2 mux	29
P0.3	A3/D3	I/O	Address/Data bit 3 mux	30
P0.4	A4/D4	I/O	Address/Data bit 4 mux	31
P0.5	A5/D5	I/O	Address/Data bit 5 mux	32
P0.6	A6/D6	I/O	Address/Data bit 6 mux	33
P0.7	A7/D7	I/O	Address/Data bit 7 mux	35
P1.0	A8	O	Address bit 8	11
P1.1	A9	O	Address bit 9	12
P1.2	A10	O	Address bit 10	13
P1.3	A11	O	Address bit 11	14
P1.4	A12	O	Address bit 12	15
P1.5	A13	O	Address bit 13	16
P1.6	A14	O	Address bit 14	17
P1.7	A15	O	Address bit 15	18
P2.0	BS0	O	Bank Switch Address 0 (A16)	48
P2.1	BS1	O	Bank Switch Address A17	49
P2.2	BS2	O	Bank Switch Address A18	50
P2.3	BS3	O	Bank Switch Address A19	51
P2.4	BS4	O	Bank Switch Address A20	52
P2.5	BS5	O	Bank Switch Address A21	53
P2.6	BS6	O	Bank Switch Address A22	54
P2.7	BS7	O	Bank Switch Address A23	55
P4.0		I/O	I/O Handshake Port 4	40
P4.1		I/O	I/O Handshake Port 4	41
P4.2		I/O	I/O Handshake Port 4	42
P4.3		I/O	I/O Handshake Port 4	43
P4.4	INT0	I	External interrupt 0	44

PIN DESCRIPTION (Continued)

Table 1. ST90E54,T54 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P4.4	WDOUT	O	T/WD output	44
P4.4		I/O	I/O Handshake Port 4	44
P4.5	INT4	I	External interrupt 4	45
P4.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	45
P4.5		I/0	I/O Handshake Port 4	45
P4.6	INT5	I	External interrupt 5	46
P4.6	T0OUTB	O	MF Timer 0 output B	46
P4.6		I/O	I/O Handshake Port 4	46
P4.7	T0OUTA	O	MF Timer 0 output A	47
P4.7	$\overline{\text{BUSREQ}}$	I	External Bus Request	47
P4.7		I/O	I/O Handshake Port 4	47
P5.0		I/O	I/O Handshake Port 5	6
P5.1		I/O	I/O Handshake Port 5	5
P5.2		I/O	I/O Handshake Port 5	4
P5.3		I/O	I/O Handshake Port 5	3
P5.3	P/$\overline{\text{D}}$	O	Program/data space select	3
P5.4	T1OUTA	O	MF Timer 1 output A	2
P5.4		I/0	I/O Handshake Port 5	2
P5.5	T1OUTB	O	MF Timer 1 output B	1
P5.5		I/O	I/O Handshake Port 5	1
P5.6	T3OUTA	O	MF Timer 3 output A	84
P5.6		I/0	I/O Handshake Port 5	84
P5.7	T3OUTB	O	MF Timer 3 output B	83
P5.7		I/O	I/O Handshake Port 5	83
P6.0	A0	O	Address bit 0 (non mux)	19
P6.1	A1	O	Address bit 1 (non mux)	20
P6.2	A2	O	Address bit 2 (non mux)	21
P6.3	A3	O	Address bit 3 (non mux)	22
P6.4	A4	O	Address bit 4 (non mux)	23

PIN DESCRIPTION (Continued)

Table 1. ST90E54,T54 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P6.5	A5	O	Address bit 5 (non mux)	24
P6.6	A6	O	Address bit 6 (non mux)	25
P6.7	A7	O	Address bit 7 (non mux)	26
P7.0	AIN0	I	A/D Analog input 0	64
P7.0	ADTRG	I	A/D conversion trigger	64
P7.0	WRRDY4	I	Handshake Write Ready P4	64
P7.0	RX0CKIN	I	SCI0 Receive Clock input	64
P7.0	WDIN	I	T/WD input	64
P7.0	BSH_EN1	I	Bank Switch High Nibble Enable	64
P7.1	AIN1	I	A/D Analog input 1	65
P7.1	RDRDY4	O	Handshake Read Ready P4	65
P7.1	SDI	I	SPI Serial Data In	65
P7.1	T0INB	I	MF Timer 0 input B	65
P7.2	AIN2	I	A/D Analog input 2	66
P7.2	CLK0OUT	O	SCI0 Byte Sync Clock output	66
P7.2	TX0CKIN	I	SCI0 Transmit Clock input	66
P7.2	BSL_EN1	I	Bank Switch Low Nibble Enable	66
P7.3	AIN3	I	A/D Analog input 3	67
P7.3	P/$\overline{D}$	O	Program/data space select	67
P7.3	T0INA	I	MF Timer 0 input A	67
P7.4	AIN4	I	A/D Analog input 4	68
P7.5	AIN5	I	A/D Analog input 5	69
P7.6	AIN6	I	A/D Analog input 6	70
P7.7	AIN7	I	A/D Analog input 7	71
P8.0	WRRDY5	I	Handshake Write Ready P5	61
P8.0	T3INA	I	MF Timer 3 input A	61
P8.1	RDRDY5	O	Handshake Read Ready P5	60
P8.1	T1INB	I	MF Timer 1 input B	60
P8.2	INT1	I	External interrupt 1	79

PIN DESCRIPTION (Continued)

Table 1. ST9054 I/O Port Alternate Function Summary (Continued)

I/O PORT Port.bit	Name	Function IN/OUT	Alternate Function	Pin
P8.2	T1OUTA	O	MF Timer 1 output A	79
P8.2	$\overline{\text{WRSTB5}}$	O	Handshake Write Strobe P5	79
P8.3	INT3	I	External interrupt 3	78
P8.3	T1OUTB	O	MF Timer 1 output B	78
P8.3	$\overline{\text{RDSTB5}}$	I	Handshake Read Strobe P5	78
P8.4	T1INA	I	MF Timer 1 input A	77
P8.4	$\overline{\text{WAIT}}$	I	External Wait input	77
P8.4	WDOUT	O	T/WD output	77
P8.5	P/D	O	Program/data space select	76
P8.5	T3INB	I	MF Timer 3 input B	76
P8.6	INT7	I	External interrupt 7	75
P8.6	T3OUTA	O	MF Timer 3 output A	75
P8.7	NMI	I	Non-Maskable Interrupt	74
P8.7	T3OUTB	O	MF Timer 3 output B	74
P9.0	S1OUT	O	SCI1 Serial Output	56
P9.1	T0OUTB	O	MF Timer 0 output B	57
P9.1	S1IN	I	SCI1 Serial Input	57
P9.2	CLK1OUT	O	SCI1 Byte Sync Clock output	58
P9.2	TX1CKIN	I	SCI1 Transmit Clock input	58
P9.3	RX1CKIN	I	SCI1 Receive Clock input	59
P9.3	T0OUTA	O	MF Timer 0 output A	59
P9.4	S0OUT	O	SCI0 Serial Output	60
P9.5	S0IN	I	SCI0 Serial Input	61
P9.5	$\overline{\text{BUSACK}}$	O	External Bus Acknowledge	61
P9.6	INT2	I	External interrupt 2	62
P9.6	SCK	O	SPI Serial Clock	62
P9.6	WRSTB4	O	Handshake Write Strobe P4	62
P9.7	INT6	I	External interrupt 6	63
P9.7	SDO	O	SPI Serial Data Out	63

ST90E54 CORE

The Core or Central Processing Unit (CPU) of the ST90E54 includes the 8 bit Arithmetic Logic Unit and the 16 bit Program Counter, System and User Stack Pointers. The microcoded Instruction Set is highly optimised for both byte (8 bit) and word (16 bit) data, BCD and Boolean data types, with 14 addressing modes. Two 8 bit I/O ports are connected to the Core module for external memory interfacing, while a 16 bit Timer/Watchdog gives system security and timing functions, and a Serial Peripheral Interface allows for synchronous communication. Three independent buses are controlled by the Core, a 16 bit Memory bus, an 8 bit Register addressing bus and a 6 bit Interrupt/DMA bus connected to the interrupt and DMA controllers in the on-chip peripherals and the Core. This multiple bus architecture allows a high degree of pipelining and parallel operation within the ST90E54, giving it its efficiency in both numerical calculations and communication with the on-chip peripherals.

MEMORY

The memory of the ST90E54 is functionally divided into two areas, the Register File and Memory. The Memory may optionally be divided into two spaces, each having a maximum of 65,536 bytes. The Memory may be expanded with the Bankswitch logic to give paging of the top 32K bytes of each space to expand the ST90E54 addressing capability to 8M bytes in each space. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E54 32K bytes of on-chip EPROM memory is selected at memory addresses 0 through 7FFFh (hexadecimal) in the PROGRAM space, while the ST90T54 OTP version has the top 64 bytes of the program space reserved by SGS-THOMSON for testing purposes. The Data space includes the 1,280 bytes of on-chip RAM at addresses 0 through 04FFh.

Off-chip memory, addressed using the address and data buses (Port 0, Port 1 and Port 6), may be divided into the Program and Data spaces by the external decoding of the Program/Data select pin (P/$\overline{D}$) available as an Alternate function. At addresses greater than the first 32K of program space, the ST90E54 executes external memory cycles for instruction fetches. The Data Strobe $\overline{DS}$ will not be generated when accessing the internal memory. The on-chip general purpose Registers may be used as additional RAM memory for minimum chip count systems.

EPROM PROGRAMMING

The 32,768 of EPROM memory of the ST90E54 (32,704 for the ST90T54) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

FIGURE 3. Memory Spaces, Bankswitch Disable

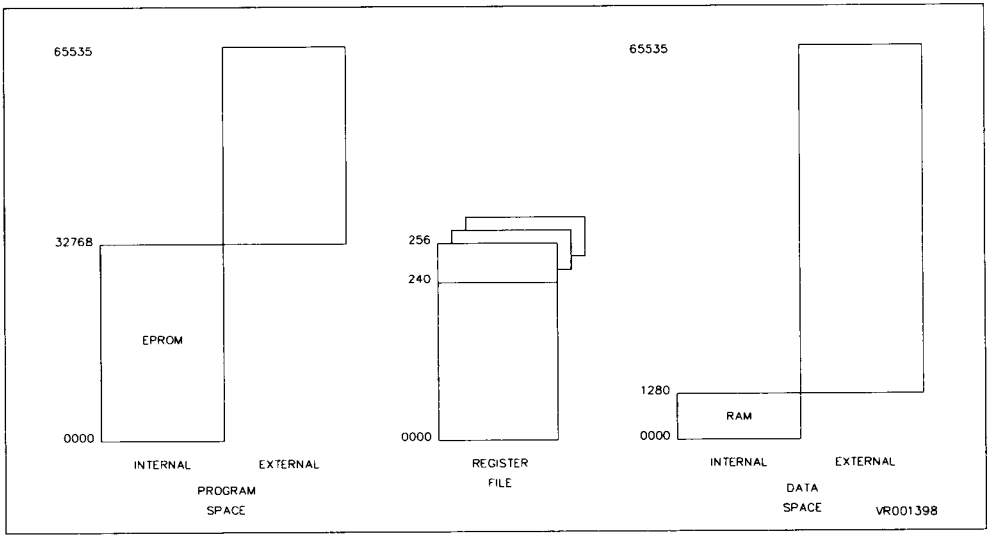
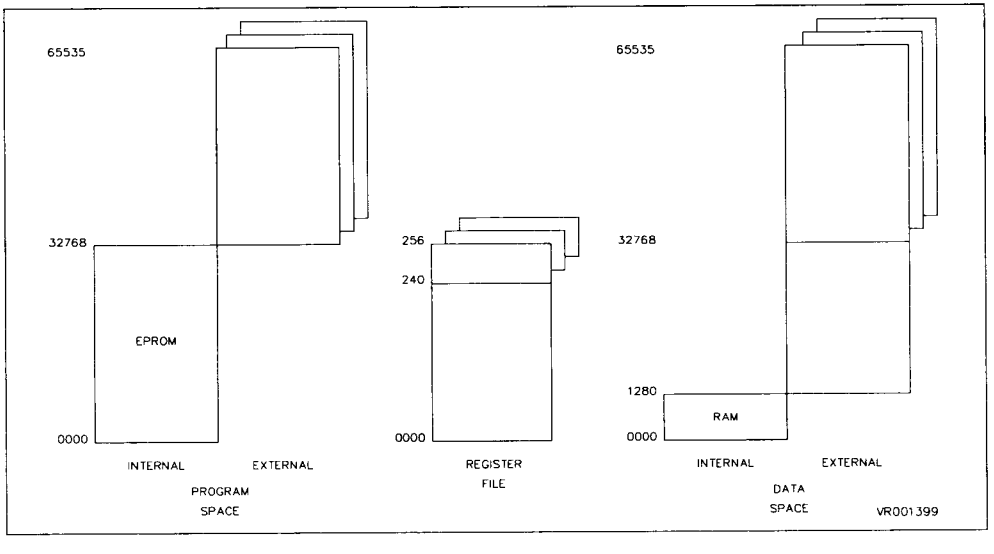


Figure 4. Memory Spaces, Bankswitch Enabled



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} \le AV_{SS} < AV_{DD} \le V_{DD}$	V
V_I	Input Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	V_{SS} – 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	– 0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Oscillator Frequency		12	MHz

DC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40 °C to + 85°C, unless otherwise specified)

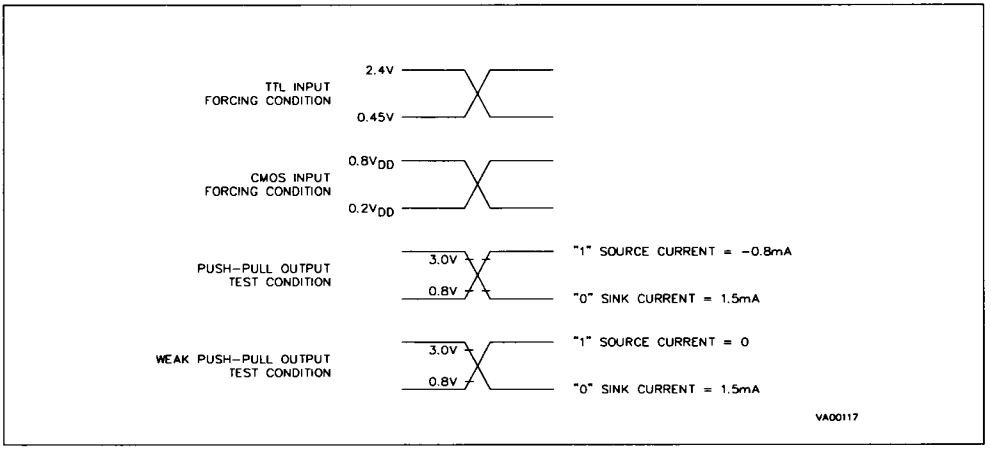
Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	Reset Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	Reset Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	Reset Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = – 1.6mA			0.4	V
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 80	– 200	– 420	µA

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	$V_{IN} < 0.8V$	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, $0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{LKRS}	Reset Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, $0V < V_{IN} < V_{DD}$	– 3		+ 3	µA
I_{LKAP}	Active Pull-up Input Leakage	$0V < V_{IN} < 0.8V$	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	$0V < V_{IN} < V_{DD}$	– 10		+ 10	µA
I_{DD}	Run Mode Current	24MHz, Note 1		32	70	mA
		4MHz, Note 1		6	12	mA
I_{DP2}	Run Mode Current Prescale by 2	24MHz, Note 1		19	40	mA
		4MHz, Note 1		4	8	mA
I_{WFI}	WFI Mode Current	24MHz, Note 1		9	18	mA
		4MHz, Note 1		2.5	5	mA
I_{HALT}	HALT Mode Current	24MHz, Note 1			100	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

Note: 1. All I/O Ports are configured in Bidirectional Weak Pull-up Mode with no DC load, External Clock pin (OSCIN) is driven by square wave external clock. No peripheral working. External interface not active (Internal Program Execution).

DC TEST CONDITIONS



AC ELECTRICAL CHARACTERISTICS

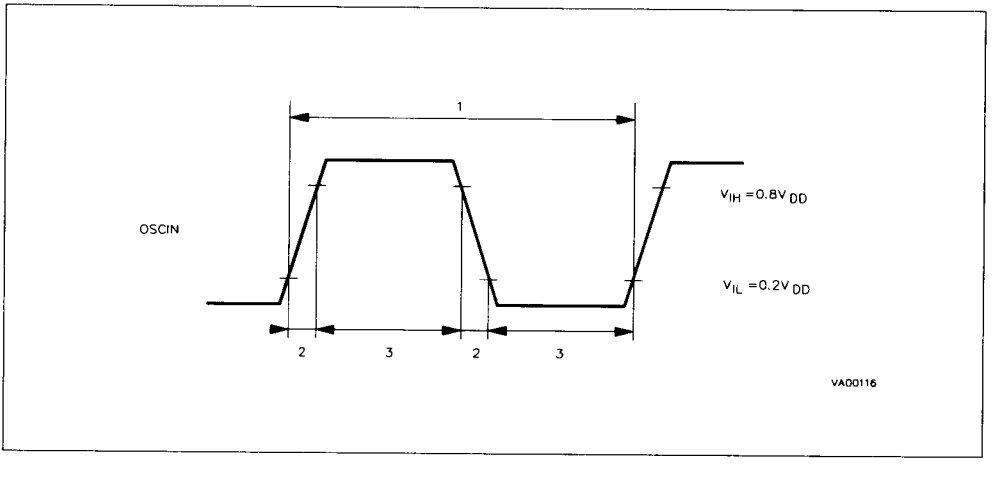
CLOCK TIMING TABLE

(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, unless otherwise specified)

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	a
			83		ns	b
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	25	12	ns	a
			38		ns	b

Notes:
a. Clock divided by 2 internally (MODER.DIV2=1)
b. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



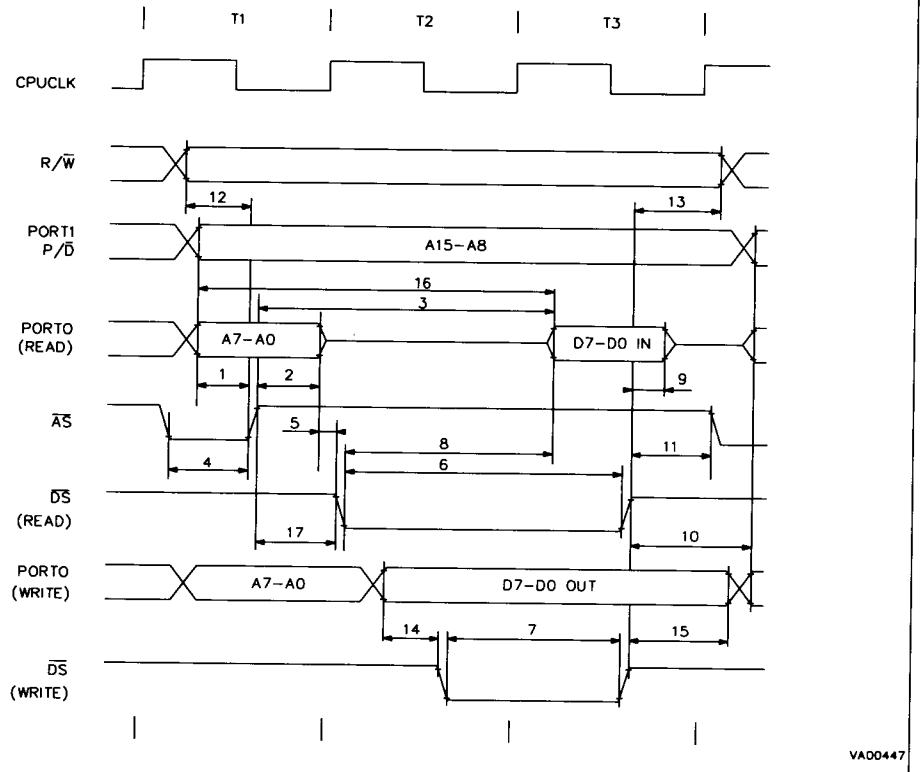
EXTERNAL BUS TIMING TABLE (V_{DD} = 5V ± 10%, T_A = – 40 °C to + 85 °C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	Address Float to $\overline{DS}$ ↓	0	0	0		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) – 16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) – 46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after DS ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) – 64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC = OSCIN Period
TwCH = High Level OSCIN half period
TwCL = Low Level OSCIN half period

EXTERNAL BUS TIMING

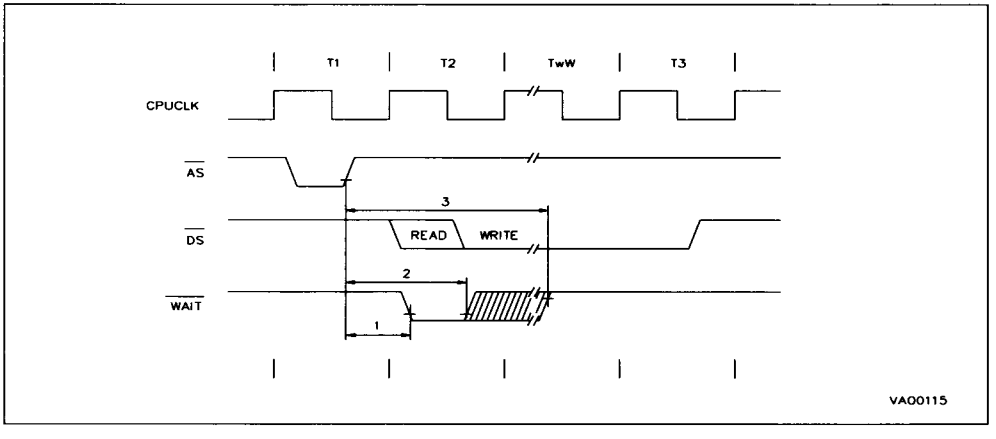


EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC −29	(P+1)TpC −29		40	ns
2	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Minimum Delay	2(P+W+1)TpC −4	(P+W+1)TpC −4	80		ns
3	TdAS (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↑ Maximum Delay	2(P+W+1)TpC −29	(P+W+1)TpC −29		83W+40	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL WAIT TIMING

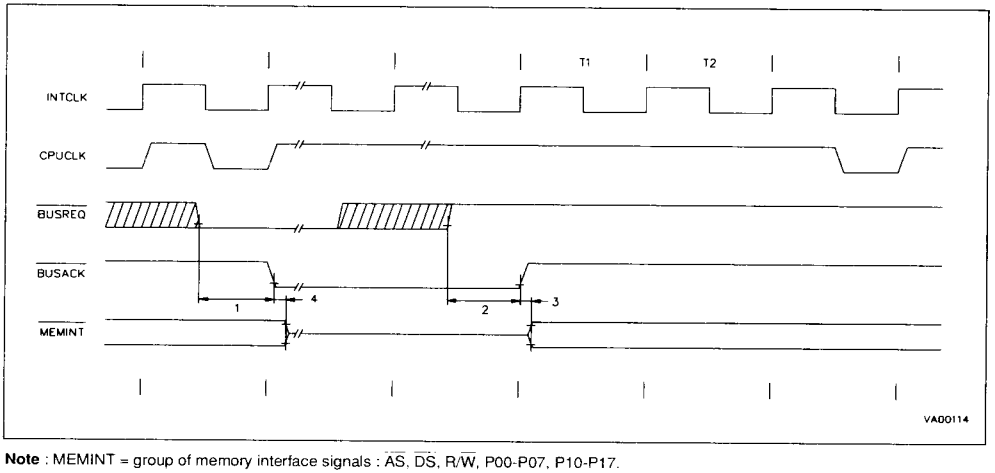


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



Note : MEMINT = group of memory interface signals : $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17.

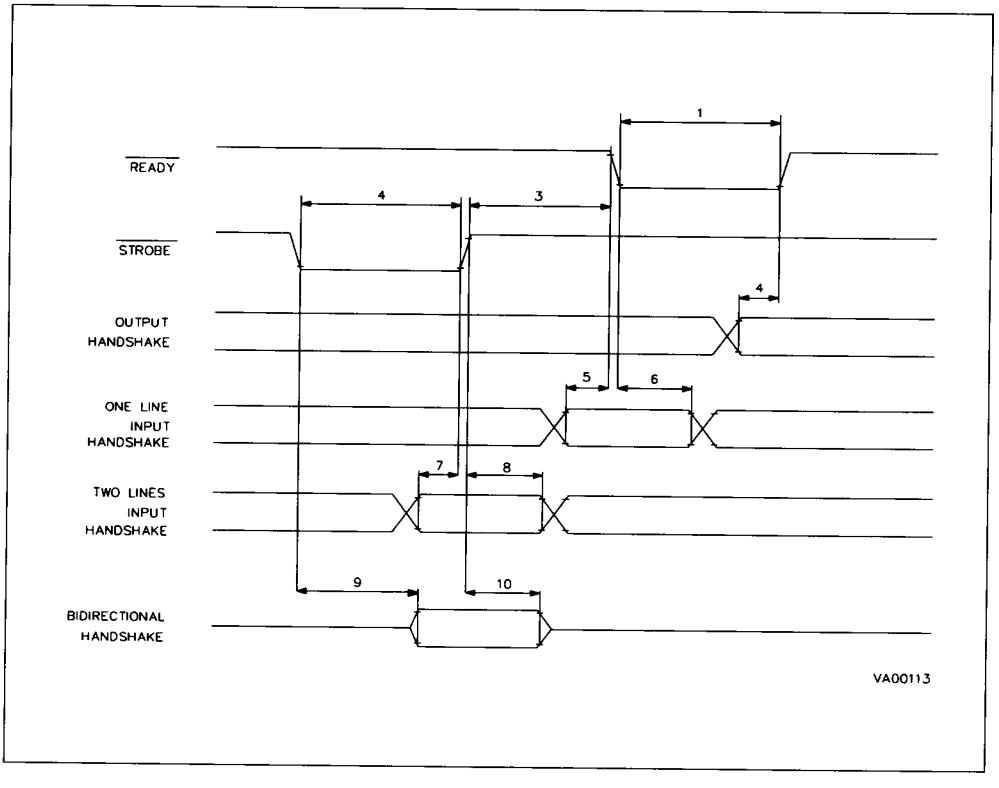
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = −40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) −18		TpC (P+W+1) −18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC −25		TwCH+(W+P) TpC −25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period. prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value (R235.4,3,2)
W = Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

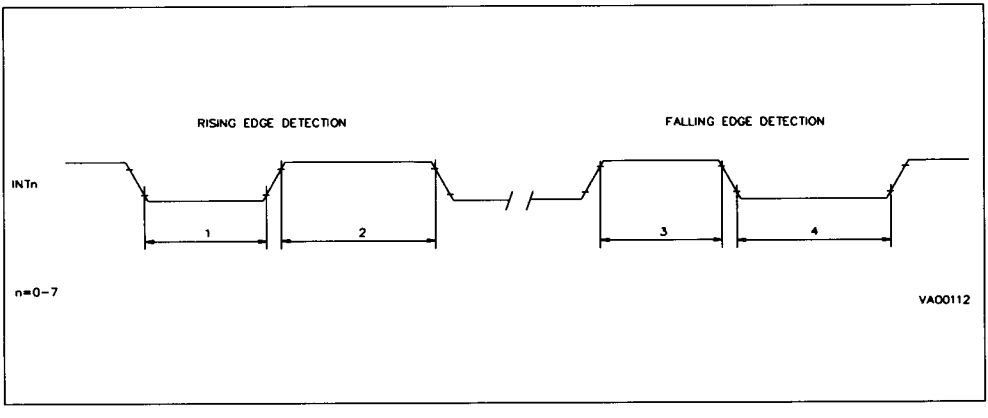


EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

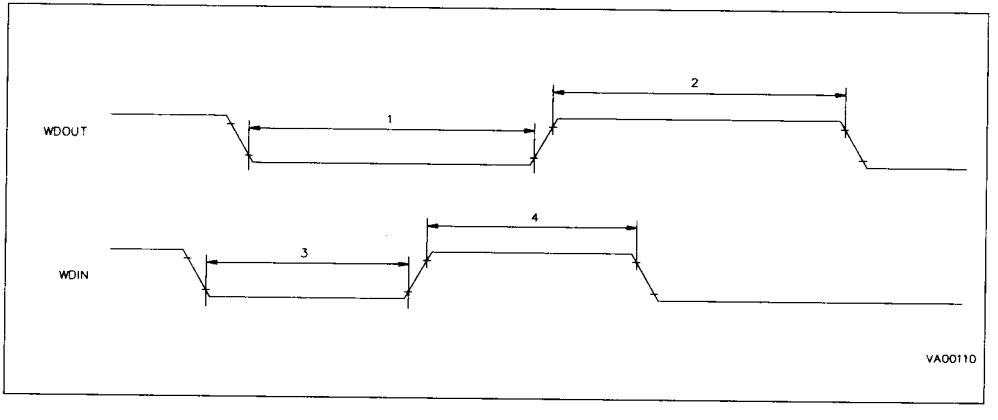
EXTERNAL INTERRUPT TIMING



WATCHDOG TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN Low Pulse Width	350		ns
4	TwWDIH	WDIN High Pulse Width	350		ns

WATCHDOG TIMING

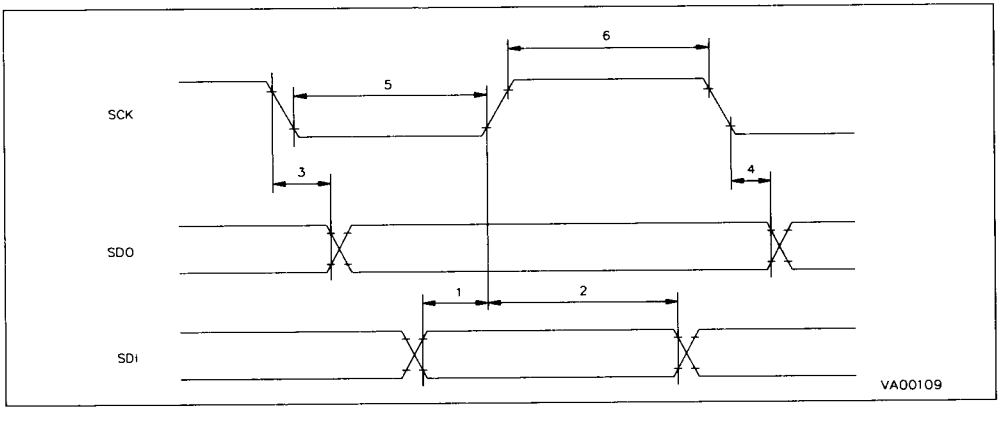


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

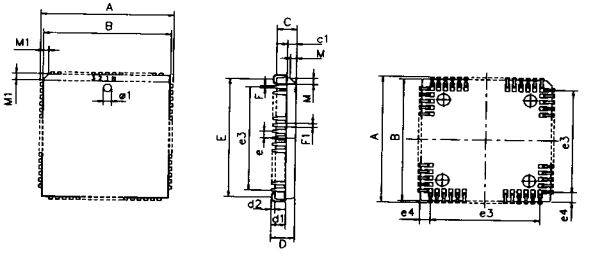
Note: 1. TpC is the Clock period.

SPI TIMING



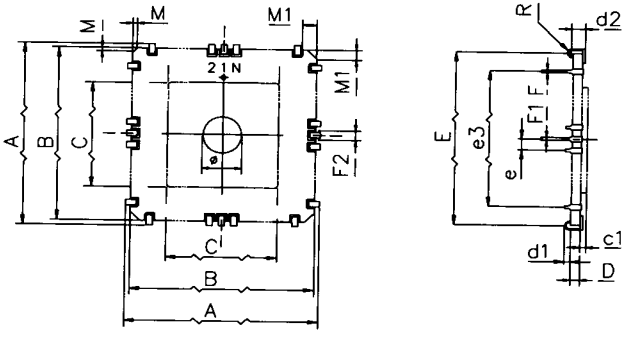
PACKAGES MECHANICAL DATA

Figure 5. 84-Lead Plastic Leaded Chip Carrier



DIM	MM			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	30.10		30.35	1.18		1.19
B	29.20		29.41	1.14		1.15
C						
C1						
D	4.20		5.08	0.16		0.19
D1		2.54			0.02	
D2		0.56				
D3				1.09		1.12
E	27.69		28.70		0.04	
e		1.27				
e3					0.01	
F		0.38				
F1						0.003
G			0.101			
H		1.27			0.04	
H1		1.14			0.04	

Figure 6. 84-Lead Window Ceramic Leaded Chip Carrier (L)



DIM	MM			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	29.37		30.48	1.15		1.19
B	28.83		29.59	1.13		1.16
C			18.92			0.74
C1			0.30			0.01
D	1.37		1.68	0.05		0.06
d1						
d2		2.23			0.08	
E	28.19		29.21	1.10		1.14
e		1.27			0.04	
e3	25.15		25.65	0.91		1
F		0.45			0.01	
F1		0.63			0.02	
F2						
M						
M1						
R		0.76			0.02	

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E54L6	24MHz	– 40°C to + 85°C	CLCC84-W
ST90E54L1	24MHz	0°C to + 70°C	CLCC84-W
ST90T54C6	24MHz	– 40°C to + 85°C	PLCC84
ST90T54C1	24MHz	0°C to + 70°C	PLCC84