5.2 Electrical Characteristics of HD6305X1/X2, HD6305Y1/Y2, HD63P05Y1

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply voltage	V_{CC}	-0.3 ∿ +7.0	V
Input voltage	V_{in}	-0.3 ∿ V_{CC} + 0.3	V
Operating temperature	T_{opr}	0 ∿ +70	°C
Storage temperature	T_{stg}	-55 ∿ +150	°C

[NOTE] These products have a protection circuit in their input terminals against high electrostatic voltage or high electric fields. Notwithstanding, be careful not to apply any voltage higher than the absolute maximum rating to these high input impedance circuits. To assure normal operation, we recommended V_{in}, V_{out}; $V_{SS} \leqq (V_{in}$ or $V_{out}) \leqq V_{CC}$

■ ELECTRICAL CHARACTERISTICS

● DC Characteristics (V_{CC} = 5.0V ± 10%, V_{SS} = GND, T_a = 0 ∿ +70°C, unless otherwise specified.)

Item		Symbol	Test Condition	min	typ	max	Unit
Input voltage "High"	$\overline{RES}$, $\overline{STBY}$	V_{IH}		V_{CC}-0.5	-	V_{CC}+0.3	V
	EXTAL			V_{CC}×0.7	-	V_{CC}+0.3	V
	Others			2.0	-	V_{CC}+0.3	V
Input voltage "Low"	All Input	V_{IL}		-0.3	-	0.8	V
Output voltage "High"	All Output	V_{OH}	I_{OH}= -200μA	2.4	-	-	V
			I_{OH}= -10μA	V_{CC}-0.7	-	-	
Output voltage "Low"	All Output	V_{OL}	I_{OL}=1.6mA	-	-	0.55	V
Input leakage current	TIMER, $\overline{INT}$, D_1 ∿ D_7, $\overline{STBY}$	$\lvert I_{IL} \rvert$	V_{in}=0.5 ∿ V_{CC} - 0.5V	-	-	1.0	μA
Three-state current	A_0 ∿ A_7, B_0 ∿ B_7, C_0 ∿ C_7, ADR_0 ∿ ADR_{13},* $DATA_0$ ∿$DATA_7$, E*, R/$\overline{W}$*	$\lvert I_{TSI} \rvert$		-	-	1.0	μA
Current** dissipation	Operating	I_{CC}	f = 1MHz***	-	5	10	mA
	Wait			-	2	5	mA
	Stop			-	2	10	μA
	Standby			-	2	10	μA
Input**** capacity	All terminals	C_{in}	f = 1MHz, V_{in} = 0V	-	-	12	pF

* At standby mode

** V_{IH} min = V_{CC} - 1.0V. V_{IL} max = 0.8 V. For HD63P05Y1, I_{CC} of EPROM is not included.

*** The value at f = xMHz can be calculated by the following equation: I_{CC} (f = xMHz) = I_{CC} (f = 1MHz) multiplied by X.

**** HD63P05Y1 is MAX. 15pF

● AC Characteristics (V_{CC} = 5.0V ± 10%, V_{SS} =GND, T_a = 0 ∿ +70°C, unless otherwise specified.)

Item	Symbol	Test Condition	HD6305X1/X2/Y1/Y2 HD63P05Y1			HD63A05X1/X2/Y1/Y2 HD63PA05Y1			HD63B05X1/X2/Y1/Y2 HD63PB05Y1			Unit
			min	typ	max	min	typ	max	min	typ	max	
Cycle Time	t_{cyc}	Fig. 6-4	1	-	10	0.666	-	10	0.5	-	10	µs
Enable Rise Time	t_{Er}		-	-	20	-	-	20	-	-	20	ns
Enable Fall Time	t_{Ef}		-	-	20	-	-	20	-	-	20	ns
Enable Pulse Width ("High" Level)	PW_{EH}		450	-	-	300	-	-	220	-	-	ns
Enable Pulse Width ("Low" Level)	PW_{EL}		450	-	-	300	-	-	220	-	-	ns
Address Delay Time	t_{AD}		-	-	250	-	-	190	-	-	180	ns
Address Hold Time	t_{AH}		40	-	-	30	-	-	20	-	-	ns
Data Delay Time	t_{DW}		-	-	200	-	-	160	-	-	120	ns
Data Hold Time (Write)	t_{HW}		40	-	-	30	-	-	20	-	-	ns
Data Set-up Time (Read)	t_{DSR}		80	-	-	60	-	-	50	-	-	ns
Data Hold Time (Read)	t_{HR}		0	-	-	0	-	-	0	-	-	ns

● Port Timing (V_{CC} = 5.0V ± 10%, V_{ss} = GND, T_a = 0 ∿ +70°C, unless otherwise noted.)

Item	Symbol	Test Condition	HD6305X1/X2/Y1/Y2 HD63P05Y1			HD63A05X1/X2/Y1/Y2 HD63PA05Y1			HD63B05X1/X2/Y1/Y2 HD63PB05Y1			Unit
			min	typ	max	min	typ	max	min	typ	max	
Port Data Set-up Time (Port A, B, C, D)	t_{PDS}	Fig. 6-5	200	–	–	200	–	–	200	–	–	ns
Port Data Hold Time (Port A, B, C, D)	t_{PDH}		200	–	–	200	–	–	200	–	–	ns
Port Data Delay Time (Port A, B, C)	t_{PDW}	Fig. 6-6	–	–	300	–	–	300	–	–	300	ns

● Control Signal Timing (V_{CC} = 5.0V ± 10%, V_{ss} = GND, T_a = 0 ∿ +70°C, unless otherwise noted.)

Item	Symbol	Test Condition	HD6305X1/X2/Y1/Y2 HD63P05Y1			HD63A05X1/X2/Y1/Y2 HD63PA05Y1			HD63B05X1/X2/Y1/Y2 HD63PB05Y1			Unit
			min	typ	max	min	typ	max	min	typ	max	
$\overline{INT}$ Pulse Width	t_{IWL}		t_{cyc} +250	–	–	t_{cyc} +200	–	–	t_{cyc} +200	–	–	ns
$\overline{INT_2}$ Pulse Width	t_{IWL2}		t_{cyc} +250	–	–	t_{cyc} +200	–	–	t_{cyc} +200	–	–	ns
$\overline{RES}$ Pulse Width	t_{RWL}		5	–	–	5	–	–	5	–	–	t_{cyc}
Control Set-up Time	t_{CS}	Fig. 6-8	250	–	–	250	–	–	250	–	–	ns
Timer Pulse Width	t_{TWL}		t_{cyc} +250	–	–	t_{cyc} +200	–	–	t_{cyc} +200	–	–	ns
Oscillation Start Time (Crystal)	t_{OSC}	Fig. 6-8*	–	–	20	–	–	20	–	–	20	ms
Reset Delay Time	t_{RHL}	**	80	–	–	80	–	–	80	–	–	ms

* C_L = 22pF±20%, R_S = 60Ω max.

** 2.2 μF

● SCI Timing (V_{CC} = 5.0V ± 10%, V_{SS} = GND, T_a = 0 ∿ +70°C, unless otherwise noted)

Item	Symbol	Test Condition	HD6305X1/X2/Y1/Y2 HD63P05Y1			HD63A05X1/X2/Y1/Y2 HD63PA05Y1			HD63B05X1/X2/Y1/Y2 HD63PB05Y1			Unit
			min	typ	max	min	typ	max	min	typ	min	
Clock Cycle Time	t_{Scyc}	Fig. 6-9 Fig. 6-10	1	-	32768	0.67	-	21845	0.5	-	16384	µs
Data Output Delay Time	t_{TXD}		-	-	250	-	-	250	-	-	250	ns
Data Set-up Time	t_{SRX}		200	-	-	200	-	-	200	-	-	ns
Data Hold Time	t_{HRX}		100	-	-	100	-	-	100	-	-	ns

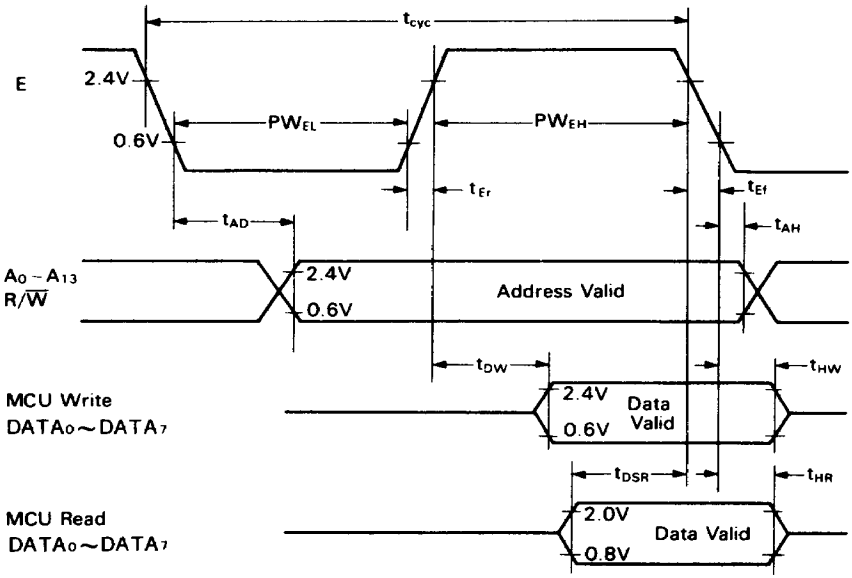


Fig. 5-4 Bus Timing

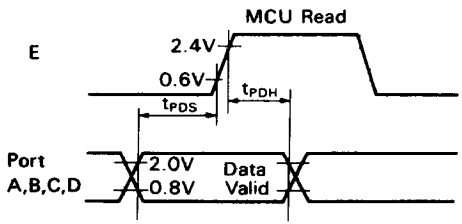


Fig. 5-5 Port Data Set-up and Hold Times (MCU Read)

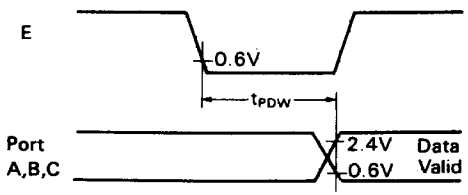


Fig. 5-6 Port Data Delay Time (MCU Write)

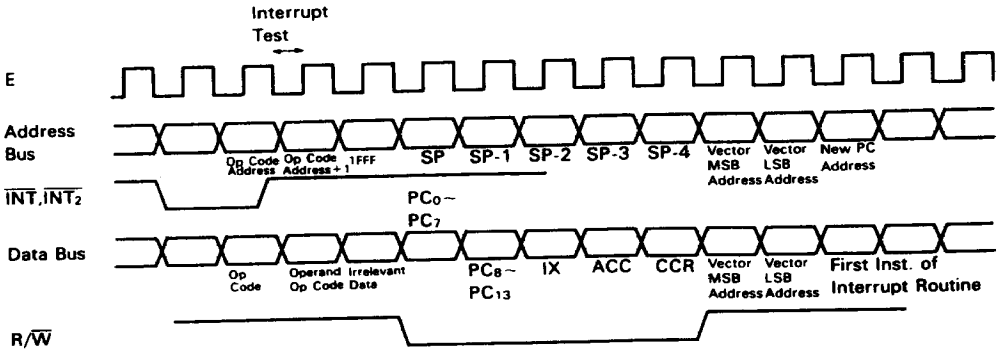


Fig. 5-7 Interrupt Sequence

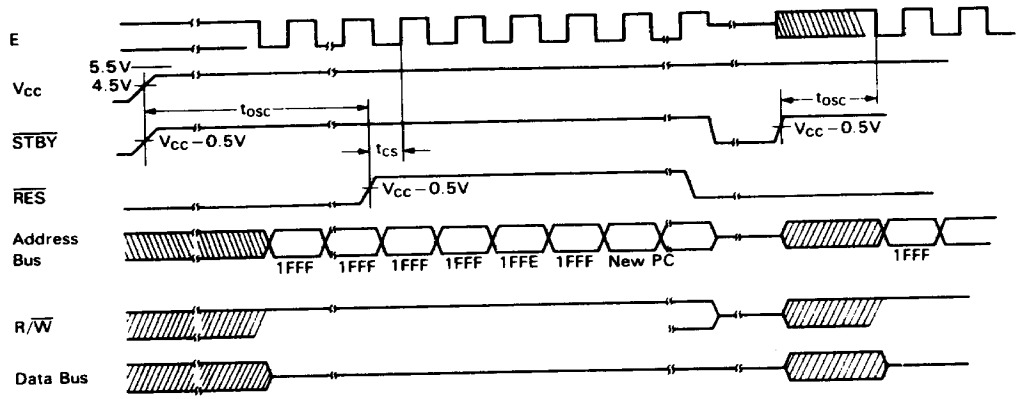


Fig. 5-8 Reset Timing

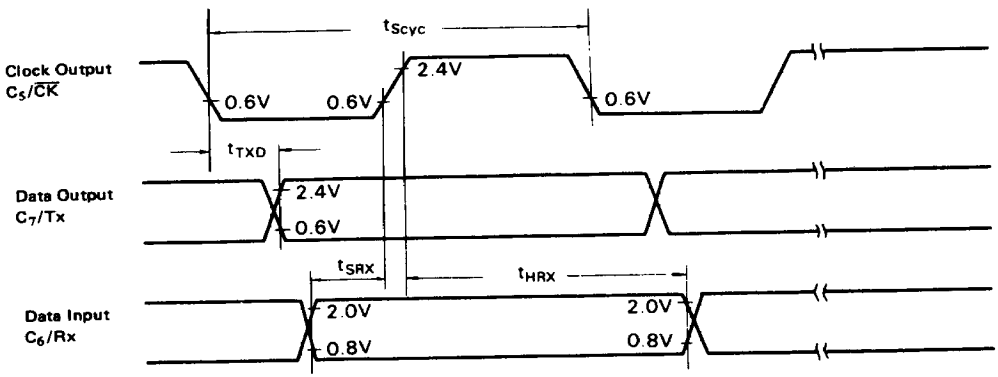


Fig. 5-9 SCI Timing (Internal Clock)

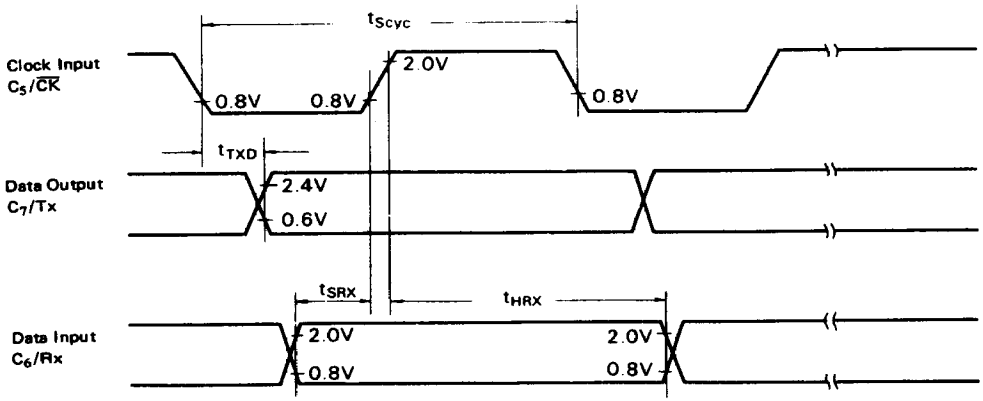
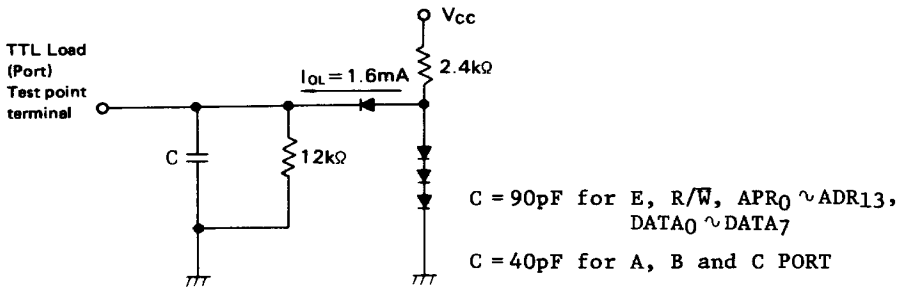


Fig. 5-10 SCI Timing (External Clock)



[NOTES] 1. The load capacitance includes stary capacitance caused by the probe, etc.
2. All diodes are 1S2074 Ⓗ.

Fig. 5-11 Test Load