HB52RF329E2-75F

256 MB Registered SDRAM DIMM
32-Mword × 72-bit, 133 MHz Memory Bus, 2-Bank Module
(36 pcs of 16 M × 4 Components)
PC133 SDRAM

HITACHI

Description

The HB52RF329E2 belongs to 8-byte DIMM (Dual In-line Memory Module) family, and has been developed as an optimized main memory solution for 8-byte processor applications. The HB52RF329E2 is a 16M × 72 × 2-bank Synchronous Dynamic RAM Registered Module, mounted 18 pieces of 64-Mbit SDRAM (HM5264405FTB) sealed in TCP package, 1 piece of PLL clock driver, 3 pieces of register driver and 1 piece of serial EEPROM (2-kbit) for Presence Detect (PD). An outline of the HB52RF329E2 is 168-pin socket type package (dual lead out). Therefore, the HB52RF329E2 makes high density mounting possible without surface mount technology. The HB52RF329E2 provides common data inputs and outputs. Decoupling capacitors are mounted beside each TCP on the module board.

Note: Do not push the cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

Features

- Fully compatible with   : JEDEC standard outline 8-byte DIMM
- 168-pin socket type package (dual lead out)
   — Outline: 133.37 mm (Length) × 38.1 mm (Height) × 4.00 mm (Thickness)
   — Lead pitch: 1.27 mm
- 3.3 V power supply
- Clock frequency: 133 MHz (max)
- LVTTL interface
- Data bus width: × 72 ECC
- Single pulsed $\overline{\text{RAS}}$

Hitachi
semiconductor

HB52RF329E2-75F

- 4 Banks can operates simultaneously and independently
- Burst read/write operation and burst read/single write operation capability
- Programmable burst length: 1/2/4/8/full page
- 2 variations of burst sequence
    — Sequential
    — Interleave
- Programmable $\overline{CE}$ latency: 4 (133 MHz)
    : 3 (100 MHz)
- Byte control by DQMB
- Refresh cycles: 4096 refresh cycles/64 ms
- 2 variations of refresh
    — Auto refresh
    — Self refresh
- Full page burst length capability
    — Sequential burst
    — Burst stop capability

Ordering Information

Type No.	Frequency	$\overline{CE}$ latency	Package	Contact pad
HB52RF329E2-75F[1]	133 MHz	4	168-pin dual lead out socket type	Gold

Note: 1. 100 MHz operation at $\overline{CE}$ latency = 3.

HITACHI

Pin Arrangement
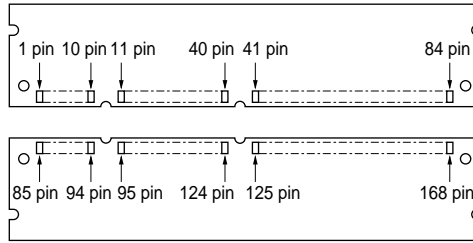
Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	V_{ss}	43	V_{ss}	85	V_{ss}	127	V_{ss}
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	$\overline{S2}$	87	DQ33	129	NC
4	DQ2	46	DQMB2	88	DQ34	130	DQMB6
5	DQ3	47	DQMB3	89	DQ35	131	DQMB7
6	V_{cc}	48	NC	90	V_{cc}	132	NC
7	DQ4	49	V_{cc}	91	DQ36	133	V_{cc}
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	V_{ss}	54	V_{ss}	96	V_{ss}	138	V_{ss}
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	V_{cc}	101	DQ45	143	V_{cc}
18	V_{cc}	60	DQ20	102	V_{cc}	144	DQ52
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	NC	104	DQ47	146	NC
21	CB0	63	NC	105	CB4	147	REGE
22	CB1	64	V_{ss}	106	CB5	148	V_{ss}
23	V_{ss}	65	DQ21	107	V_{ss}	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55

HITACHI

HB52RF329E2-75F

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{W}$	69	DQ24	111	$\overline{CE}$	153	DQ56
28	DQMB0	70	DQ25	112	DQMB4	154	DQ57
29	DQMB1	71	DQ26	113	DQMB5	155	DQ58
30	$\overline{S0}$	72	DQ27	114	NC	156	DQ59
31	NC	73	V_{CC}	115	$\overline{RE}$	157	V_{CC}
32	V_{SS}	74	DQ28	116	V_{SS}	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	76	DQ30	118	A3	160	DQ62
35	A4	77	DQ31	119	A5	161	DQ63
36	A6	78	V_{SS}	120	A7	162	V_{SS}
37	A8	79	CK2	121	A9	163	CK3
38	A10 (AP)	80	NC	122	A13 (BA0)	164	NC
39	A12 (BA1)	81	WP	123	A11	165	SA0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA1
41	V_{CC}	83	SCL	125	CK1	167	SA2
42	CK0	84	V_{CC}	126	NC	168	V_{CC}

HITACHI

Pin Description

Pin name	Function	
A0 to A11	Address input	
	— Row address	A0 to A11
	— Column address	A0 to A9
A13/A12	Bank select address	BA0/BA1
DQ0 to DQ63	Data input/output	
CB0 to CB7	Check bit (Data input/output)	
$\overline{S0}$ to $\overline{S3}$	Chip select input	
$\overline{RE}$	Row enable ($\overline{RAS}$) input	
$\overline{CE}$	Column enable ($\overline{CAS}$) input	
$\overline{W}$	Write enable input	
DQMB0 to DQMB7	Byte data mask	
CK0 to CK3	Clock input	
CKE0	Clock enable input	
WP	Write protect for serial PD	
REGE[1]	Register enable	
SDA	Data input/output for serial PD	
SCL	Clock input for serial PD	
SA0 to SA2	Serial address input	
V_{CC}	Primary positive power supply	
V_{SS}	Ground	
NC	No connection	

Note: 1. REGE is the Register Enable pin which permits the DIMM to operate in "buffered" mode and "registered" mode. To conform to this specification, mother boards must pull this pin to high state ("registerd" mode).

Serial PD Matrix*[1]

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes used by module manufacturer	1	0	0	0	0	0	0	0	80	128
1	Total SPD memory size	0	0	0	0	1	0	0	0	08	256 byte
2	Memory type	0	0	0	0	0	1	0	0	04	SDRAM
3	Number of row addresses bits	0	0	0	0	1	1	0	0	0C	12
4	Number of column addresses bits	0	0	0	0	1	0	1	0	0A	10
5	Number of banks	0	0	0	0	0	0	1	0	02	2
6	Module data width	0	1	0	0	1	0	0	0	48	72 bit
7	Module data width (continued)	0	0	0	0	0	0	0	0	00	0 (+)
8	Module interface signal levels	0	0	0	0	0	0	0	1	01	LVTTL
9	SDRAM cycle time (highest $\overline{CE}$ latency) 7.5 ns	0	1	1	1	0	1	0	1	75	CL = 3
10	SDRAM access from Clock (highest $\overline{CE}$ latency) 5.4 ns	0	1	0	1	0	1	0	0	54	*[5]
11	Module configuration type	0	0	0	0	0	0	1	0	02	ECC
12	Refresh rate/type	1	0	0	0	0	0	0	0	80	Normal (15.625 µs) Self refresh
13	SDRAM width	0	0	0	0	0	1	0	0	04	16M × 4
14	Error checking SDRAM width	0	0	0	0	0	1	0	0	04	× 4
15	SDRAM device attributes: minimum clock delay for back-to-back random column addresses	0	0	0	0	0	0	0	1	01	1 CLK
16	SDRAM device attributes: Burst lengths supported	1	0	0	0	1	1	1	1	8F	1, 2, 4, 8, full page
17	SDRAM device attributes: number of banks on SDRAM device	0	0	0	0	0	1	0	0	04	4
18	SDRAM device attributes: $\overline{CE}$ latency	0	0	0	0	0	1	1	0	06	2, 3
19	SDRAM device attributes: $\overline{S}$ latency	0	0	0	0	0	0	0	1	01	0
20	SDRAM device attributes: $\overline{W}$ latency	0	0	0	0	0	0	0	1	01	0
21	SDRAM device attributes	0	0	0	1	0	1	1	0	16	Registered

HITACHI

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
22	SDRAM device attributes: General	0	0	0	0	1	1	1	0	0E	$V_{CC} \pm 10\%$
23	SDRAM cycle time (2nd highest $\overline{CE}$ latency) Undefined	1	0	1	0	0	0	0	0	A0	CL = 2
24	SDRAM access from Clock (2nd highest $\overline{CE}$ latency) Undefined	0	1	1	0	0	0	0	0	60	*5
25	SDRAM cycle time (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
26	SDRAM access from Clock (3rd highest $\overline{CE}$ latency) Undefined	0	0	0	0	0	0	0	0	00	
27	Minimum row precharge time	0	0	0	1	0	1	0	0	14	20 ns
28	Row active to row active min	0	0	0	0	1	1	1	1	0F	15 ns
29	$\overline{RE}$ to $\overline{CE}$ delay min	0	0	0	1	0	1	0	0	14	20 ns
30	Minimum $\overline{RE}$ pulse width	0	0	1	0	1	1	0	1	2D	45 ns
31	Density of each bank on module	0	0	1	0	0	0	0	0	20	2 bank 128M byte
32	Address and command signal input setup time	0	0	0	1	0	1	0	1	15	1.5 ns*5
33	Address and command signal input hold time	0	0	0	0	1	0	0	0	08	0.8 ns*5
34	Data signal input setup time	0	0	0	1	0	1	0	1	15	1.5 ns*5
35	Data signal input hold time	0	0	0	0	1	0	0	0	08	0.8 ns*5
36 to 61	Superset information	0	0	0	0	0	0	0	0	00	Future use
62	SPD data revision code	0	0	0	0	0	0	1	0	02	JEDEC2
63	Checksum for bytes 0 to 62	1	1	0	0	0	0	0	0	C0	192
64	Manufacturer's JEDEC ID code	0	0	0	0	0	1	1	1	07	HITACHI
65 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	*2 (ASCII-8bit code)
73	Manufacturer's part number	0	1	0	0	1	0	0	0	48	H
74	Manufacturer's part number	0	1	0	0	0	0	1	0	42	B
75	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
76	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
77	Manufacturer's part number	0	1	0	1	0	0	1	0	52	R
78	Manufacturer's part number	0	1	0	0	0	1	1	0	46	F
79	Manufacturer's part	0	0	1	1	0	0	1	1	33	3

HITACHI

Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
80	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
81	Manufacturer's part number	0	0	1	1	1	0	0	1	39	9
82	Manufacturer's part number	0	1	0	0	0	1	0	1	45	E
83	Manufacturer's part number	0	0	1	1	0	0	1	0	32	2
84	Manufacturer's part number	0	0	1	0	1	1	0	1	2D	—
85	Manufacturer's part number	0	0	1	1	0	1	1	1	37	7
86	Manufacturer's part number	0	0	1	1	0	1	0	1	35	5
87	Manufacturer's part number	0	1	0	0	0	1	1	0	46	F
88	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
89	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
90	Manufacturer's part number	0	0	1	0	0	0	0	0	20	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30	Initial
92	Revision code	0	0	1	0	0	0	0	0	20	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Assembly serial number	*3									
99 to 125	Manufacturer specific data	—	—	—	—	—	—	—	—	—	*4
126	Reserved (Intel specification frequency)	0	1	1	0	0	1	0	0	64	
127	Reserved (Intel specification $\overline{CE}$# latency support)	1	0	0	0	0	1	1	1	87	

Notes: 1. All serial PD data are not protected. 0: Serial data, "driven Low", 1: Serial data, "driven High".

2. Byte72 is manufacturing location code. (ex: In case of Japan, byte72 is 4AH. 4AH shows "J" on ASCII code.)

3. Bytes 95 through 98 are assembly serial number.

4. All bits of 99 through 125 are not defined ("1" or "0").

5. These specifications are defined based on component specification, not module.

HITACHI

Block Diagram

$\overline{RS0}$
$\overline{RS1}$
RDQMB0

RDQMB4

DQMB $\overline{CS}$ D0	DQMB $\overline{CS}$ D18
I/O0 to I/O3	I/O0 to I/O3

DQ0 to DQ3 4 10 Ω

DQMB $\overline{CS}$ D9	DQMB $\overline{CS}$ D27
I/O0 to I/O3	I/O0 to I/O3

DQ32 to DQ35 4 10 Ω

DQMB $\overline{CS}$ D1	DQMB $\overline{CS}$ D19
I/O0 to I/O3	I/O0 to I/O3

DQ4 to DQ7 4 10 Ω

DQMB $\overline{CS}$ D10	DQMB $\overline{CS}$ D28
I/O0 to I/O3	I/O0 to I/O3

DQ36 to DQ39 4 10 Ω

RDQMB1

RDQMB5

DQMB $\overline{CS}$ D2	DQMB $\overline{CS}$ D20
I/O0 to I/O3	I/O0 to I/O3

DQ8 to DQ11 4 10 Ω

DQMB $\overline{CS}$ D11	DQMB $\overline{CS}$ D29
I/O0 to I/O3	I/O0 to I/O3

DQ40 to DQ43 4 10 Ω

DQMB $\overline{CS}$ D3	DQMB $\overline{CS}$ D21
I/O0 to I/O3	I/O0 to I/O3

DQ12 to DQ15 4 10 Ω

DQMB $\overline{CS}$ D12	DQMB $\overline{CS}$ D30
I/O0 to I/O3	I/O0 to I/O3

DQ44 to DQ47 4 10 Ω

DQMB D4	DQMB D22
I/O0 to I/O3	I/O0 to I/O3

CB0 to CB3 4 10 Ω

DQMB D13 $\overline{CS}$	DQMB D31 $\overline{CS}$
I/O0 to I/O3	I/O0 to I/O3

CB4 to CB7 4 10 Ω

$\overline{RS2}$
$\overline{RS3}$
RDQMB2

RDQMB6

DQMB $\overline{CS}$ D5	DQMB $\overline{CS}$ D23
I/O0 to I/O3	I/O0 to I/O3

DQ16 to DQ19 4 10 Ω

DQMB $\overline{CS}$ D14	DQMB $\overline{CS}$ D32
I/O0 to I/O3	I/O0 to I/O3

DQ48 to DQ51 4 10 Ω

DQMB $\overline{CS}$ D6	DQMB $\overline{CS}$ D24
I/O0 to I/O3	I/O0 to I/O3

DQ20 to DQ23 10 Ω

DQMB $\overline{CS}$ D15	DQMB $\overline{CS}$ D33
I/O0 to I/O3	I/O0 to I/O3

DQ52 to DQ55 4 10 Ω

RDQMB3

RDQMB7

DQMB $\overline{CS}$ D7	DQMB $\overline{CS}$ D25
I/O0 to I/O3	I/O0 to I/O3

DQ24 to DQ27 4 10 Ω

DQMB $\overline{CS}$ D16	DQMB $\overline{CS}$ D34
I/O0 to I/O3	I/O0 to I/O3

DQ56 to DQ59 4 10 Ω

DQMB $\overline{CS}$ D8	DQMB $\overline{CS}$ D26
I/O0 to I/O3	I/O0 to I/O3

DQ28 to DQ31 4 10 Ω

DQMB $\overline{CS}$ D17	DQMB $\overline{CS}$ D35
I/O0 to I/O3	I/O0 to I/O3

DQ60 to DQ63 4 10 Ω

REGISTER:
$\overline{S0}, \overline{S1}, \overline{S2}, \overline{S3}$ → $\overline{RS0}, \overline{RS1}, \overline{RS2}, \overline{RS3}$
DQMB0 to DQMB7 → RDQMB0 to RDQMB7
BA0 to BA1 → RBA0 to RBA1 -> BA0 to BA1: SDRAMs D0 to D35
A0 to A11 → RA0 to RA11 -> A0 to A11: SDRAMs D0 to D35
$\overline{RE}$ → $\overline{RRAS}$ -> $\overline{RAS}$: SDRAMs D0 to D35
$\overline{CE}$ → $\overline{RCAS}$ -> $\overline{CAS}$: SDRAMs D0 to D35
CKE0 → RCKE0 -> CKE: SDRAMs D0 to D35
$\overline{W}$ → $\overline{RW}$ -> $\overline{WE}$: SDRAMs D0 to D35

V_{CC} —10k— REGE
PLL CK

CK0 10 Ω 12 pF → PLL → CK: SDRAMs (D0 to D35) Register

CK1 to CK3 10 Ω 12 pF → V_{SS}

V_{CC} → V_{CC} (D0 to D35, U0)
0.0022 μF × 25 pcs   0.22 μF × 19 pcs
V_{SS} → V_{SS} (D0 to D35, U0)

* D0 to D35: HM5264405
  PLL: 2510
  Register: 162834
  U0: 2-kbit EEPROM

Serial PD

SCL → SCL   SDA → SDA
U0
A0 A1 A2   → WP 47 kΩ
SA0 SA1 SA2 V_{SS}

Notes:
1. The SDA pull-up resistor is required due to the open-drain/open-collector output.
2. The SCL pull-up resistor is recommended because of the normal SCL line inacitve "high" state.

HITACHI

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on any pin relative to V_{SS}	V_T	−0.5 to V_{CC} + 0.5 ($\leq$ 4.6 (max))	V	1
Supply voltage relative to V_{SS}	V_{CC}	−0.5 to +4.6	V	1
Short circuit output current	Iout	50	mA	
Power dissipation	P_T	18.0	W	
Operating temperature	Topr	0 to +55	°C	
Storage temperature	Tstg	−50 to +100	°C	

Note: 1.   Respect to V_{SS}

DC Operating Conditions (Ta = 0 to +55°C)

Parameter	Symbol	Min	Max	Unit	Notes
Supply voltage	V_{CC}	3.0	3.6	V	1, 2
	V_{SS}	0	0	V	3
Input high voltage	V_{IH}	2.0	V_{CC}	V	1, 4
Input low voltage	V_{IL}	0	0.8	V	1, 5
Ambient illuminance	—	—	100	lx	

Notes: 1.   All voltage referred to V_{SS}
2.   The supply voltage with all V_{CC} pins must be on the same level.
3.   The supply voltage with all V_{SS} pins must be on the same level.
4. V_{IH} (max) = V_{CC} + 2.0 V for pulse width $\leq$ 3 ns at V_{CC}.
5. V_{IL} (min) = V_{CC} − 2.0 V for pulse width $\leq$ 3 ns at V_{SS}.

HITACHI

V_{IL}/V_{IH} **Clamp** (Component characteristics)

This SDRAM component has V_{IL} and V_{IH} clamp for CK, CKE, $\overline{S}$, DQMB and DQ pins.

Minimum V_{IL} Clamp Current

V_{IL} (V)	I (mA)
−2	−32
−1.8	−25
−1.6	−19
−1.4	−13
−1.2	−8
−1	−4
−0.9	−2
−0.8	−0.6
−0.6	0
−0.4	0
−0.2	0
0	0

HITACHI
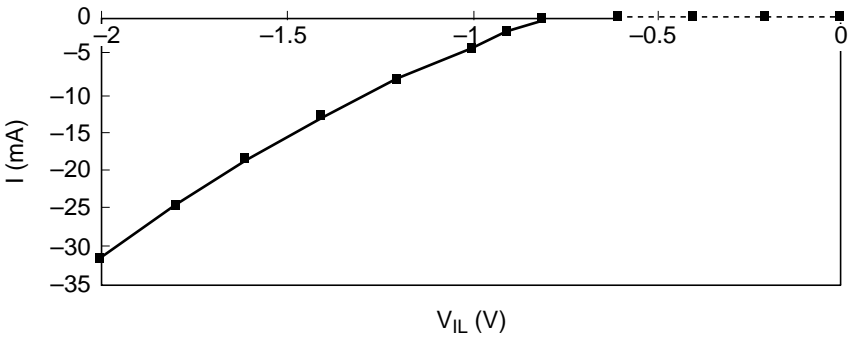
Minimum V_{IH} Clamp Current (referred to V_{CC})

V_{IH} (V)	I (mA)
V_{CC} + 2	10
V_{CC} + 1.8	8
V_{CC} + 1.6	5.5
V_{CC} + 1.4	3.5
V_{CC} + 1.2	1.5
V_{CC} + 1	0.3
V_{CC} + 0.8	0
V_{CC} + 0.6	0
V_{CC} + 0.4	0
V_{CC} + 0.2	0
V_{CC} + 0	0

HITACHI
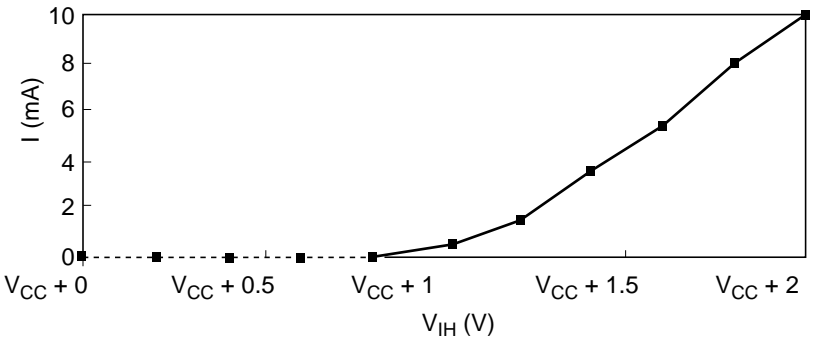
I_{OL}/I_{OH} Characteristics (Component characteristics)

Output Low Current (I_{OL})

Vout (V)	I_{OL} Min (mA)	I_{OL} Max (mA)
0	0	0
0.4	27	71
0.65	41	108
0.85	51	134
1	58	151
1.4	70	188
1.5	72	194
1.65	75	203
1.8	77	209
1.95	77	212
3	80	220
3.45	81	223

HITACHI
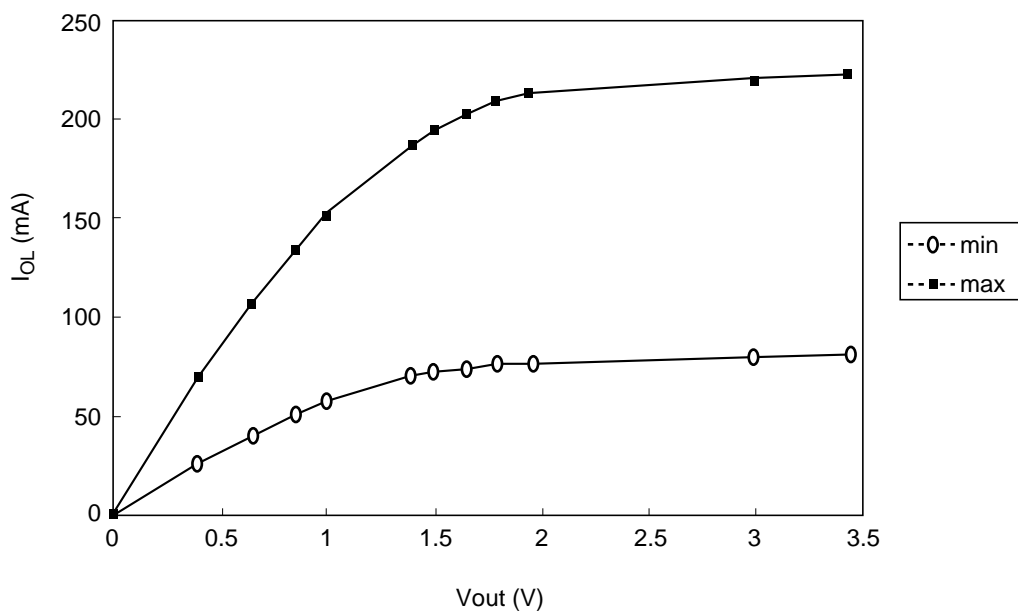
Output High Current (I_{OH}) (Ta = 0 to 55°C, V_{CC} = 3.0 V to 3.45 V, V_{SS} = 0 V)

Vout (V)	I_{OH} Min (mA)	I_{OH} Max (mA)
3.45	—	−3
3.3	—	−28
3	0	−75
2.6	−21	−130
2.4	−34	−154
2	−59	−197
1.8	−67	−227
1.65	−73	−248
1.5	−78	−270
1.4	−81	−285
1	−89	−345
0	−93	−503

HITACHI

DC Characteristics (Ta = 0 to 55°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

Parameter	Symbol	PC133 $\overline{CE}$ latency = 4		PC100 $\overline{CE}$ latency = 3		Unit	Test conditions	Notes
		Min	Max	Min	Max			
Operating current	I_{CC1}	—	2495	—	2495	mA	Burst length = 1 t_{RC} = min	1, 2, 3
Standby current in power down	I_{CC2P}	—	803	—	803	mA	CKE = V_{IL}, t_{CK} = 12 ns	6
Standby current in power down (input signal stable)	I_{CC2PS}	—	767	—	767	mA	CKE = V_{IL}, t_{CK} = ∞	7
Standby current in non power down	I_{CC2N}	—	1271	—	1271	mA	CKE, $\overline{S}$ = V_{IH}, t_{CK} = 12 ns	4
Active standby current in power down	I_{CC3P}	—	839	—	839	mA	CKE = V_{IL}, t_{CK} = 12 ns	1, 2, 6
Active standby current in non power down	I_{CC3N}	—	1415	—	1415	mA	CKE, $\overline{S}$ = V_{IH}, t_{CK} = 12 ns	1, 2, 4
Burst operating current	I_{CC4}	—	2675	—	2315	mA	t_{CK} = min, BL = 4	1, 2, 5
Refresh current	I_{CC5}	—	3125	—	3125	mA	t_{RC} = min	3
Self refresh current	I_{CC6}	—	731	—	731	mA	$V_{IH} \geq V_{CC} - 0.2$ V $V_{IL} \leq 0.2$ V	8
Input leakage current	I_{LI}	−10	10	−10	10	μA	$0 \leq Vin \leq V_{CC}$	
Output leakage current	I_{LO}	−10	10	−10	10	μA	$0 \leq Vout \leq V_{CC}$ DQ = disable	
Output high voltage	V_{OH}	2.4	—	2.4	—	V	I_{OH} = −4 mA	
Output low voltage	V_{OL}	—	0.4	—	0.4	V	I_{OL} = 4 mA	

Notes: 1. I_{CC} depends on output load condition when the device is selected. I_{CC} (max) is specified at the output open condition.
2. One bank operation.
3. Input signals are changed once per one clock.
4. Input signals are changed once per two clocks.
5. Input signals are changed once per four clocks.
6. After power down mode, CK operating current.
7. After power down mode, no CK operating current.
8. After self refresh mode set, self refresh current.

HITACHI

Capacitance (Ta = 25°C, V_{CC} = 3.3 V ± 0.3 V)

Parameter	Symbol	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	25	pF	1, 2, 4
Input capacitance ($\overline{RE}$, $\overline{CE}$, $\overline{W}$)	C_{I2}	25	pF	1, 2, 4
Input capacitance (CKE)	C_{I3}	45	pF	1, 2, 4
Input capacitance ($\overline{S}$)	C_{I4}	20	pF	1, 2, 4
Input capacitance (CK)	C_{I5}	45	pF	1, 2, 4
Input capacitance (DQMB)	C_{I6}	20	pF	1, 2, 4
Input/Output capacitance (DQ)	$C_{I/O1}$	25	pF	1, 2, 3, 4

Notes: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. Measurement condition: f = 1 MHz, 1.4 V bias, 200 mV swing.
3. DQMB = V_{IH} to disable Data-out.
4. This parameter is sampled and not 100% tested.

AC Characteristics (Ta = 0 to 55°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V)

			HB52RF329E2-75F					
			PC133 $\overline{CE}$ latency = 4		PC100 $\overline{CE}$ latency = 3			
Parameter	HITACHI Symbol	PC100 Symbol	Min	Max	Min	Max	Unit	Notes
System clock cycle time	t_{CK}	Tclk	7.5	—	10	—	ns	1
CK high pulse width	t_{CKH}	Tch	3.4	—	4	—	ns	1
CK low pulse width	t_{CKL}	Tcl	3.4	—	4	—	ns	1
Access time from CK	t_{AC}	Tac	—	6.3	—	7.5	ns	1, 2
Data-out hold time	t_{OH}	Toh	1.8	—	2.1	—	ns	1, 2
CK to Data-out low impedance	t_{LZ}		1.1	—	1.1	—	ns	1, 2, 3
CK to Data-out high impedance	t_{HZ}		—	6.3	—	7.5	ns	1, 4
Data-in setup time	t_{DS}	Tsi	2.4	—	2.9	—	ns	1
Data in hold time	t_{DH}	Thi	1.7	—	3.4	—	ns	1
Address setup time	t_{AS}	Tsi	1.9	—	2.6	—	ns	1
Address hold time	t_{AH}	Thi	1.5	—	3.0	—	ns	1
CKE setup time	t_{CES}	Tsi	1.9	—	2.6	—	ns	1, 5
CKE setup time for power down exit	t_{CESP}	Tpde	1.9	—	2.6	—	ns	1
CKE hold time	t_{CEH}	Thi	1.5	—	3.0	—	ns	1

HITACHI

AC Characteristics (Ta = 0 to 55°C, V_{CC} = 3.3 V ± 0.3 V, V_{SS} = 0 V) (cont)

| Parameter | HITACHI Symbol | PC100 Symbol | HB52RF329E2-75F | | | | | |
| | | | PC133 $\overline{CE}$ latency = 4 | | PC100 $\overline{CE}$ latency = 3 | | | |
			Min	Max	Min	Max	Unit	Notes
Command setup time	t_{CS}	Tsi	1.9	—	2.6	—	ns	1
Command hold time	t_{CH}	Thi	1.5	—	3.0	—	ns	1, 5
Ref/Active to Ref/Active command period	t_{RC}	Trc	67.5	—	70	—	ns	1
Active to precharge command period	t_{RAS}	Tras	45	120000	50	120000	ns	1
Active command to column command (same bank)	t_{RCD}	Trcd	22.5	—	20	—	ns	1
Precharge to active command period	t_{RP}	Trp	22.5	—	20	—	ns	1
Write recovery or data-in to precharge lead time	t_{DPL}	Tdpl	10	—	10	—	ns	1
Active (a) to Active (b) command period	t_{RRD}	Trrd	15	—	20	—	ns	1
Transition time (rise to fall)	t_T		1	5	1	5	ns	
Refresh period	t_{REF}		—	64	—	64	ms	

Notes: 1. AC measurement assumes t_T = 1 ns. Reference level for timing of input signals is 1.5 V.
2. Access time is measured at 1.5 V. Load condition is C_L = 50 pF.
3. t_{LZ} (max) defines the time at which the outputs achieves the low impedance state.
4. t_{HZ} (max) defines the time at which the outputs achieves the high impedance state.
5. t_{CES} defines CKE setup time to CK rising edge except power down exit command.

Test Conditions

- Input and output timing reference levels: 1.5 V
- Input waveform and output load: See following figures
- Ambient illuminance: Under 100 lx.

HITACHI
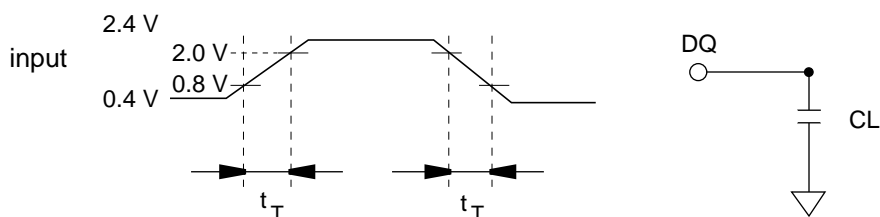
Relationship Between Frequency and Minimum Latency

Parameter	HITACHI Symbol	PC100 Symbol	133 $\overline{\text{CE}}$ latency = 4	100 $\overline{\text{CE}}$ latency = 3	Notes
Frequency (MHz)					
t_{CK} (ns)			7.5	10	
Active command to column command (same bank)	I_{RCD}		3	2	1
Active command to active command (same bank)	I_{RC}		9	7	$= [I_{RAS} + I_{RP}]$ 1
Active command to precharge command (same bank)	I_{RAS}		6	5	1
Precharge command to active command (same bank)	I_{RP}		3	2	1
Write recovery or data-in to precharge command (same bank)	I_{DPL}	Tdpl	2	1	1
Active command to active command (different bank)	I_{RRD}		2	2	1
Self refresh exit time	I_{SREX}	Tsrx	2	2	2
Last data in to active command (Auto precharge, same bank)	I_{APW}	Tdal	5	3	$= [I_{DPL} + I_{RP}]$
Self refresh exit to command input	I_{SEC}		9	7	$= [I_{RC}]$ 3
Precharge command to high impedance	I_{HZP}	Troh	4	3	
Last data out to active command (auto precharge) (same bank)	I_{APR}		0	0	
Last data out to precharge (early precharge)	I_{EP}		−3	−2	
Column command to column command	I_{CCD}	Tccd	1	1	
Write command to data in latency	I_{WCD}	Tdwd	1	1	
DQMB to data in	I_{DID}	Tdqm	1	1	
DQMB to data out	I_{DOD}	Tdqz	3	3	
CKE to CK disable	I_{CLE}	Tcke	2	2	
Register set to active command	I_{RSA}	Tmrd	3	1	
$\overline{\text{S}}$ to command disable	I_{CDD}		0	0	
Power down exit to command input	I_{PEC}		1	1	
Burst stop to output valid data hold	I_{BSR}		3	2	
Burst stop to output high impedance	I_{BSH}		4	3	
Burst stop to write data ignore	I_{BSW}		1	1	

Notes: 1. I_{RCD} to I_{RRD} are recommended value.

2. Be valid [DSEL] or [NOP] at next command of self refresh exit.

3. Except [DSEL] and [NOP]

HITACHI

Pin Functions

CK0 to CK3 (input pin): CK is the master clock input to this pin. The other input signals are referred at CK rising edge.

$\overline{S0}$ to $\overline{S3}$ (input pin): When $\overline{S}$ is Low, the command input cycle becomes valid. When $\overline{S}$ is High, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

$\overline{RE}$, $\overline{CE}$ and $\overline{W}$ (input pins): Although these pin names are the same as those of conventional DRAMs, they function in a different way. These pins define operation commands (read, write, etc.) depending on the combination of their voltage levels. For details, refer to the command operation section.

A0 to A11 (input pins): Row address (AX0 to AX11) is determined by A0 to A11 level at the bank active command cycle CK rising edge. Column address (AY0 to AY9) is determined by A0 to level at the read or write command cycle CK rising edge. And this column address becomes burst access start address. A10 defines the precharge mode. When A10 = High at the precharge command cycle, all banks are precharged. But when A10 = Low at the precharge command cycle, only the bank that is selected by A12/A13 (BA) is precharged.

A12/A13 (input pin): A12/A13 are bank select signal (BA). The memory array is divided into bank 0, bank 1, bank 2 and bank 3. If A12 is Low and A13 is Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 is High and A13 is High, bank 3 is selected.

CKE0 (input pin): This pin determines whether or not the next CK is valid. If CKE is High, the next CK rising edge is valid. If CKE is Low, the next CK rising edge is invalid. This pin is used for power-down and clock suspend modes.

DQMB0 to DQMB7 (input pins): Read operation: If DQMB is High, the output buffer becomes High-Z. If the DQMB is Low, the output buffer becomes Low-Z.

Write operation: If DQMB is High, the previous data is held (the new data is not written). If DQMB is Low, the data is written.

DQ0 to DQ63, CB0 to CB7 (input/output pins): Data is input to and output from these pins.

V_{CC} (power supply pins): 3.3 V is applied.

V_{SS} (power supply pins): Ground is connected.

HITACHI

Command Operation

Command Truth Table

The SDRAM module recognizes the following commands specified by the $\overline{S}$, $\overline{RE}$, $\overline{CE}$, $\overline{W}$ and address pins.

Command	Symbol	CKE n-1	n	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	A12/A13	A10	A0 to A11
Ignore command	DESL	H	×	H	×	×	×	×	×	×
No operation	NOP	H	×	L	H	H	H	×	×	×
Burst stop in full page	BST	H	×	L	H	H	L	×	×	×
Column address and read command	READ	H	×	L	H	L	H	V	L	V
Read with auto-precharge	READ A	H	×	L	H	L	H	V	H	V
Column address and write command	WRIT	H	×	L	H	L	L	V	L	V
Write with auto-precharge	WRIT A	H	×	L	H	L	L	V	H	V
Row address strobe and bank active	ACTV	H	×	L	L	H	H	V	V	V
Precharge select bank	PRE	H	×	L	L	H	L	V	L	×
Precharge all bank	PALL	H	×	L	L	H	L	×	H	×
Refresh	REF/SELF	H	V	L	L	L	H	×	×	×
Mode register set	MRS	H	×	L	L	L	L	V	V	V

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}. V: Valid address input

Ignore command [DESL]: When this command is set ($\overline{S}$ is High), the SDRAM module ignore command input at the clock. However, the internal status is held.

No operation [NOP]: This command is not an execution command. However, the internal operations continue.

Burst stop in full-page [BST]: This command stops a full-page burst operation (burst length = full-page) and is illegal otherwise. When data input/output is completed for a full page of data, it automatically returns to the start address, and input/output is performed repeatedly.

Column address strobe and read command [READ]: This command starts a read operation. In addition, the start address of burst read is determined by the column address and the bank select address (BA). After the read operation, the output buffer becomes High-Z.

Read with auto-precharge [READ A]: This command automatically performs a precharge operation after a burst read with a burst length of 1, 2, 4 or 8. When the burst length is full-page, this command is illegal.

HITACHI

Column address strobe and write command [WRIT]: This command starts a write operation. When the burst write mode is selected, the column address and the bank select address (BA) become the burst write start address. When the single write mode is selected, data is only written to the location specified by the column address and the bank select address (BA).

Write with auto-precharge [WRIT A]: This command automatically performs a precharge operation after a burst write with a length of 1, 2, 4 or 8, or after a single write operation. When the burst length is full-page, this command is illegal.

Row address strobe and bank activate [ACTV]: This command activates the bank that is selected by Bank select address (BA) and determines the row address (AX0 to AX11). When A12 and A13 are Low, bank 0 is activated. When A12 is High and A13 is Low, bank 1 is activated. When A12 is Low and A13 is High, bank 2 is activated. When A12 and A13 are High, bank 3 is activated.

Precharge selected bank [PRE]: This command starts precharge operation for the bank selected by Bank select address (BA). If A12 and A13 are Low, bank 0 is selected. If A12 is High and A13 is Low, bank 1 is selected. If A12 is Low and A13 is High, bank 2 is selected. If A12 and A13 are High, bank 3 is selected.

Precharge all banks [PALL]: This command starts a precharge operation for all banks.

Refresh [REF/SELF]: This command starts the refresh operation. There are two types of refresh operation, the one is auto-refresh, and the other is self-refresh. For details, refer to the CKE truth table section.

Mode register set [MRS]: The SDRAM module has a mode register that defines how it operates. The mode register is specified by the address pins (A0 to A13) at the mode register set cycle. For details, refer to the mode register configuration. After power on, the contents of the mode register are undefined, execute the mode register set command to set up the mode register.

HITACHI

DQMB Truth Table

Command	Symbol	CKE		DQMB
		n - 1	n	
Write enable/output enable	ENB	H	×	L
Write inhibit/output disable	MASK	H	×	H

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.
Write: I_{DID} is needed.
Read: I_{DOD} is needed.

The SDRAM module can mask input/output data by means of DQMB.

During reading, the output buffer is set to Low-Z by setting DQMB to Low, enabling data output. On the other hand, when DQMB is set to High, the output buffer becomes High-Z, disabling data output.

During writing, data is written by setting DQMB to Low. When DQMB is set to High, the previous data is held (the new data is not written). Desired data can be masked during burst read or burst write by setting DQMB. For details, refer to the DQMB control section of the SDRAM module operating instructions.

CKE Truth Table

Current state	Command	CKE		$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	Address
		n - 1	n					
Active	Clock suspend mode entry	H	L	×	×	×	×	×
Any	Clock suspend	L	L	×	×	×	×	×
Clock suspend	Clock suspend mode exit	L	H	×	×	×	×	×
Idle	Auto-refresh command (REF)	H	H	L	L	L	H	×
Idle	Self-refresh entry (SELF)	H	L	L	L	L	H	×
Idle	Power down entry	H	L	L	H	H	H	×
		H	L	H	×	×	×	×
Self refresh	Self refresh exit (SELFX)	L	H	L	H	H	H	×
		L	H	H	×	×	×	×
Power down	Power down exit	L	H	L	H	H	H	×
		L	H	H	×	×	×	×

Note: H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

Clock suspend mode entry: The SDRAM module enters clock suspend mode from active mode by setting CKE to Low. If command is input in the clock suspend mode entry cycle, the command is valid. The clock suspend mode changes depending on the current status (1 clock before) as shown below.

HITACHI

ACTIVE clock suspend: This suspend mode ignores inputs after the next clock by internally maintaining the bank active status.

READ suspend and READ with Auto-precharge suspend: The data being output is held (and continues to be output).

WRITE suspend and WRIT with Auto-precharge suspend: In this mode, external signals are not accepted. However, the internal state is held.

Clock suspend: During clock suspend mode, keep the CKE to Low.

Clock suspend mode exit: The SDRAM module exits from clock suspend mode by setting CKE to High during the clock suspend state.

IDLE: In this state, all banks are not selected, and completed precharge operation.

Auto-refresh command [REF]: When this command is input from the IDLE state, the SDRAM module starts auto-refresh operation. (The auto-refresh is the same as the CBR refresh of conventional DRAMs.) During the auto-refresh operation, refresh address and bank select address are generated inside the SDRAM module. For every auto-refresh cycle, the internal address counter is updated. Accordingly, 4096 times are required to refresh the entire memory. Before executing the auto-refresh command, all the banks must be in the IDLE state. In addition, since the precharge for all banks is automatically performed after auto-refresh, no precharge command is required after auto-refresh.

Self-refresh entry [SELF]: When this command is input during the IDLE state, the SDRAM module starts self-refresh operation. After the execution of this command, self-refresh continues while CKE is Low. Since self-refresh is performed internally and automatically, external refresh operations are unnecessary.

Power down mode entry: When this command is executed during the IDLE state, the SDRAM module enters power down mode. In power down mode, power consumption is suppressed by cutting off the initial input circuit.

Self-refresh exit: When this command is executed during self-refresh mode, the SDRAM module can exit from self-refresh mode. After exiting from self-refresh mode, the SDRAM module enters the IDLE state.

Power down exit: When this command is executed at the power down mode, the SDRAM module can exit from power down mode. After exiting from power down mode, the SDRAM module enters the IDLE state.

HITACHI

Function Truth Table

The following table shows the operations that are performed when each command is issued in each mode of the SDRAM module. The following table assumes that CKE is high.

Current state	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	Address	Command	Operation
Precharge	H	×	×	×	×	DESL	Enter IDLE after t_{RP}
	L	H	H	H	×	NOP	Enter IDLE after t_{RP}
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL*4
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL*4
	L	L	H	H	BA, RA	ACTV	ILLEGAL*4
	L	L	H	L	BA, A10	PRE, PALL	NOP*6
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Idle	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL*5
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL*5
	L	L	H	H	BA, RA	ACTV	Bank and row active
	L	L	H	L	BA, A10	PRE, PALL	NOP
	L	L	L	H	×	REF, SELF	Refresh
	L	L	L	L	MODE	MRS	Mode register set

HITACHI

Current state	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	Address	Command	Operation
Row active	H	×	×	×	×	DESL	NOP
	L	H	H	H	×	NOP	NOP
	L	H	H	L	×	BST	NOP
	L	H	L	H	BA, CA, A10	READ/READ A	Begin read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Begin write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop to full page
	L	H	L	H	BA, CA, A10	READ/READ A	Continue burst read to $\overline{CE}$ latency and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst read/start write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Term burst read and Precharge
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Read with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL*4
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL*4
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*4
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

HITACHI

25

Current state	$\overline{S}$	$\overline{RE}$	$\overline{CE}$	$\overline{W}$	Address	Command	Operation
Write	H	×	×	×	×	DESL	Continue burst to end
	L	H	H	H	×	NOP	Continue burst to end
	L	H	H	L	×	BST	Burst stop on full page
	L	H	L	H	BA, CA, A10	READ/READ A	Term burst and New read
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	Term burst and New write
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	Term burst write and Precharge*2
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Write with auto-precharge	H	×	×	×	×	DESL	Continue burst to end and precharge
	L	H	H	H	×	NOP	Continue burst to end and precharge
	L	H	H	L	×	BST	ILLEGAL
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL*4
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL*4
	L	L	H	H	BA, RA	ACTV	Other bank active ILLEGAL on same bank*3
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*4
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL
Refresh (auto-refresh)	H	×	×	×	×	DESL	Enter IDLE after t_{RC}
	L	H	H	H	×	NOP	Enter IDLE after t_{RC}
	L	H	H	L	×	BST	Enter IDLE after t_{RC}
	L	H	L	H	BA, CA, A10	READ/READ A	ILLEGAL*5
	L	H	L	L	BA, CA, A10	WRIT/WRIT A	ILLEGAL*5
	L	L	H	H	BA, RA	ACTV	ILLEGAL*5
	L	L	H	L	BA, A10	PRE, PALL	ILLEGAL*5
	L	L	L	H	×	REF, SELF	ILLEGAL
	L	L	L	L	MODE	MRS	ILLEGAL

Notes: 1. H: V_{IH}. L: V_{IL}. ×: V_{IH} or V_{IL}.

The other combinations are inhibit.

2. An interval of t_{DPL} is required between the final valid data input and the precharge command.

3. If t_{RRD} is not satisfied, this operation is illegal.

4. Illegal for same bank, except for another bank.

5. Illegal for all banks.

6. NOP for same bank, except for another bank.

HITACHI

From PRECHARGE state, command operation

To [DESL], [NOP] or [BST]: When these commands are executed, the SDRAM module enters the IDLE state after t_{RP} has elapsed from the completion of precharge.

From IDLE state, command operation

To [DESL], [NOP], [BST], [PRE] or [PALL]: These commands result in no operation.

To [ACTV]: The bank specified by the address pins and the ROW address is activated.

To [REF], [SELF]: The SDRAM module enters refresh mode (auto-refresh or self-refresh).

To [MRS]: The SDRAM module enters the mode register set cycle.

From ROW ACTIVE state, command operation

To [DESL], [NOP] or [BST]: These commands result in no operation.

To [READ], [READ A]: A read operation starts. (However, an interval of t_{RCD} is required.)

To [WRIT], [WRIT A]: A write operation starts. (However, an interval of t_{RCD} is required.)

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands set the SDRAM module to precharge mode. (However, an interval of t_{RAS} is required.)

From READ state, command operation

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: Data output by the previous read command continues to be output. After $\overline{CE}$ latency, the data output resulting from the next command will start.

To [WRIT], [WRIT A]: These commands stop a burst read, and start a write cycle.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

HITACHI

To [PRE], [PALL]: These commands stop a burst read, and the SDRAM module enters precharge mode.

From READ with AUTO-PRECHARGE state, command operation

To [DESL], [NOP]: These commands continue read operations until the burst operation is completed, and the SDRAM module then enters precharge mode.

To [ACTV]: This command makes other banks bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From WRITE state, command operation

To [DESL], [NOP]: These commands continue write operations until the burst operation is completed.

To [BST]: This command stops a full-page burst.

To [READ], [READ A]: These commands stop a burst and start a read cycle.

To [WRIT], [WRIT A]: These commands stop a burst and start the next write cycle.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

To [PRE], [PALL]: These commands stop burst write and the SDRAM module then enters precharge mode.

From WRITE with AUTO-PRECHARGE state, command operation

To [DESL], [NOP]: These commands continue write operations until the burst is completed, and the SDRAM module enters precharge mode.

To [ACTV]: This command makes the other bank active. (However, an interval of t_{RRD} is required.) Attempting to make the currently active bank active results in an illegal command.

From REFRESH state, command operation

To [DESL], [NOP], [BST]: After an auto-refresh cycle (after t_{RC}), the SDRAM module automatically enters the IDLE state.

HITACHI

Simplified State Diagram
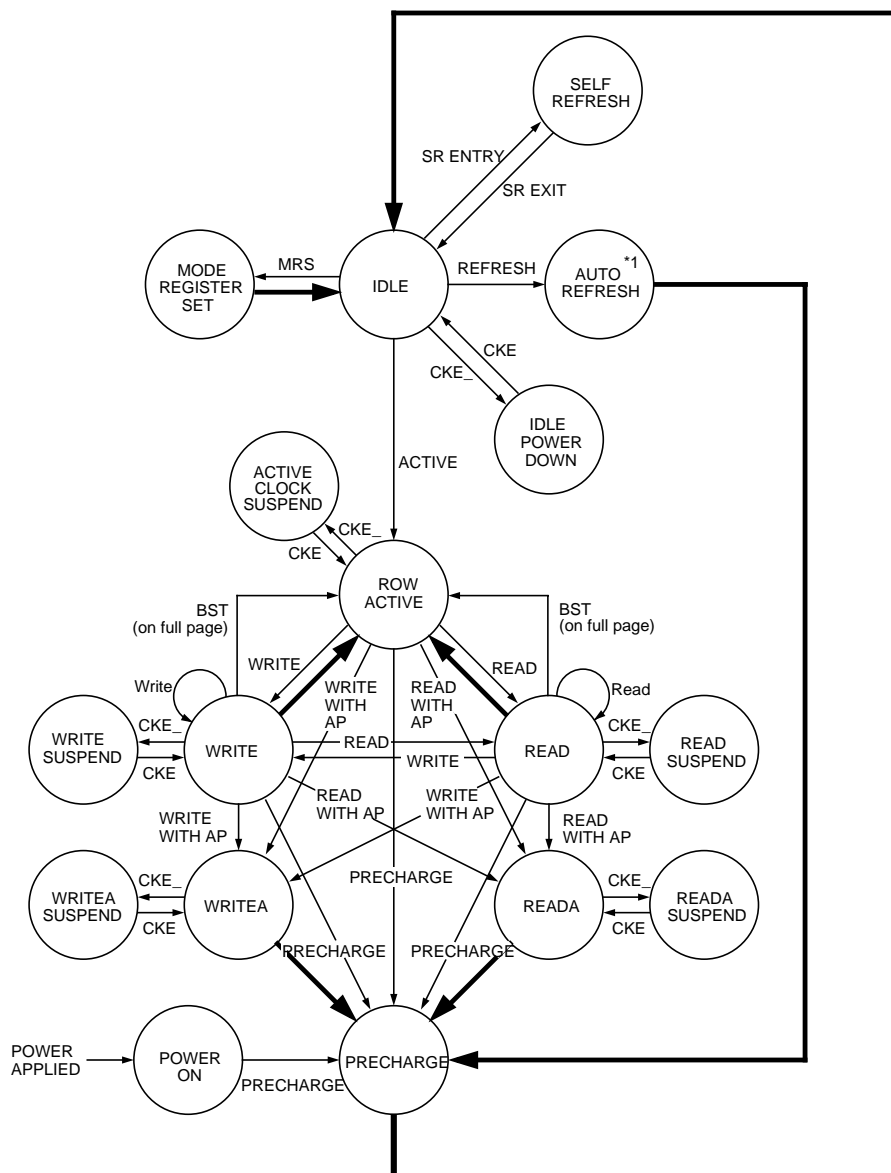
Automatic transition after completion of command.
Transition resulting from command input.

Note: 1. After the auto-refresh operation, precharge operation is performed automatically and enter the IDLE state.

HITACHI

Mode Register Configuration

The mode register is set by the input to the address pins (A0 to A13) during mode register set cycles. The mode register consists of five sections, each of which is assigned to address pins.

A13, A12, A11, A10, A9 A8: (OPCODE): The SDRAM module has two types of write modes. One is the burst write mode, and the other is the single write mode. These bits specify write mode.

Burst read and burst write: Burst write is performed for the specified burst length starting from the column address specified in the write cycle.

Burst read and single write: Data is only written to the column address specified during the write cycle, regardless of the burst length.

A7: Keep this bit Low at the mode register set cycle. If this pin is high, the vender test mode is set.

A6, A5, A4: (LMODE): These pins specify the $\overline{CE}$ latency.

A3: (BT): A burst type is specified. When full-page burst is performed, only "sequential" can be selected.

A2, A1, A0: (BL): These pins specify the burst length.

A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
OPCODE						0	LMODE			BT	BL		

A6	A5	A4	CAS Latency
0	0	0	R
0	0	1	R
0	1	0	3
0	1	1	4
1	X	X	R

A3	Burst Type
0	Sequential
1	Interleave

A2	A1	A0	Burst Length BT=0	Burst Length BT=1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	R	R
1	0	1	R	R
1	1	0	R	R
1	1	1	F.P.	R

A13	A12	A11	A10	A9	A8	Write mode
0	0	0	0	0	0	Burst read and burst write
X	X	X	X	0	1	R
X	X	X	X	1	0	Burst read and single write
X	X	X	X	1	1	R

F.P. = Full Page
R is Reserved (inhibit)
X: 0 or 1

HITACHI

Burst Sequence

Burst length = 2

Starting Ad.	Addressing(decimal)	
A0	Sequential	Interleave
0	0, 1,	0, 1,
1	1, 0,	1, 0,

Burst length = 4

Starting Ad.		Addressing(decimal)	
A1	A0	Sequential	Interleave
0	0	0, 1, 2, 3,	0, 1, 2, 3,
0	1	1, 2, 3, 0,	1, 0, 3, 2,
1	0	2, 3, 0, 1,	2, 3, 0, 1,
1	1	3, 0, 1, 2,	3, 2, 1, 0,

Burst length = 8

Starting Ad.			Addressing(decimal)	
A2	A1	A0	Sequential	Interleave
0	0	0	0, 1, 2, 3, 4, 5, 6, 7,	0, 1, 2, 3, 4, 5, 6, 7,
0	0	1	1, 2, 3, 4, 5, 6, 7, 0,	1, 0, 3, 2, 5, 4, 7, 6,
0	1	0	2, 3, 4, 5, 6, 7, 0, 1,	2, 3, 0, 1, 6, 7, 4, 5,
0	1	1	3, 4, 5, 6, 7, 0, 1, 2,	3, 2, 1, 0, 7, 6, 5, 4,
1	0	0	4, 5, 6, 7, 0, 1, 2, 3,	4, 5, 6, 7, 0, 1, 2, 3,
1	0	1	5, 6, 7, 0, 1, 2, 3, 4,	5, 4, 7, 6, 1, 0, 3, 2,
1	1	0	6, 7, 0, 1, 2, 3, 4, 5,	6, 7, 4, 5, 2, 3, 0, 1,
1	1	1	7, 0, 1, 2, 3, 4, 5, 6,	7, 6, 5, 4, 3, 2, 1, 0,

HITACHI

Operation of the Registered SDRAM module

Read/Write Operations

Bank active: Before executing a read or write operation, the corresponding bank and the row address must be activated by the bank active (ACTV) command. Bank 0, bank 1, bank 2 or bank 3 is activated according to the status of the Bank select address (BA) pin, and the row address (AX0 to AX11) is activated by the A0 to A11 pins at the bank active command cycle. An interval of t_{RCD} is required between the bank active command input and the following read/write command input.

Read operation: A read operation starts when a read command is input. Output buffer becomes Low-Z in the ($\overline{CE}$ Latency - 1) cycle after read command set. The SDRAM module can perform a burst read operation.

The burst length can be set to 1, 2, 4, 8 or full-page. The start address for a burst read is specified by the column address and the bank select address (BA) at the read command set cycle. In a read operation, data output starts after the number of clocks specified by the $\overline{CE}$ Latency. The $\overline{CE}$ Latency can be set to 3 or 4.

When the burst length is 1, 2, 4 or 8, the Dout buffer automatically becomes High-Z at the next clock after the successive burst-length data has been output.

The $\overline{CE}$ latency and burst length must be specified at the mode register.

$\overline{CE}$ Latency

CL = $\overline{CE}$ latency
Burst Length = 4

Burst Length
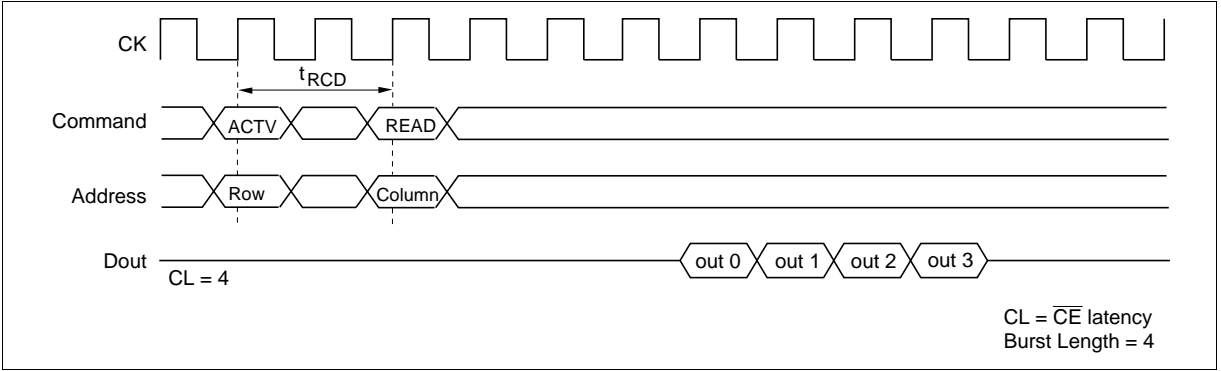
BL : Burst Length
$\overline{CE}$ Latency = 4
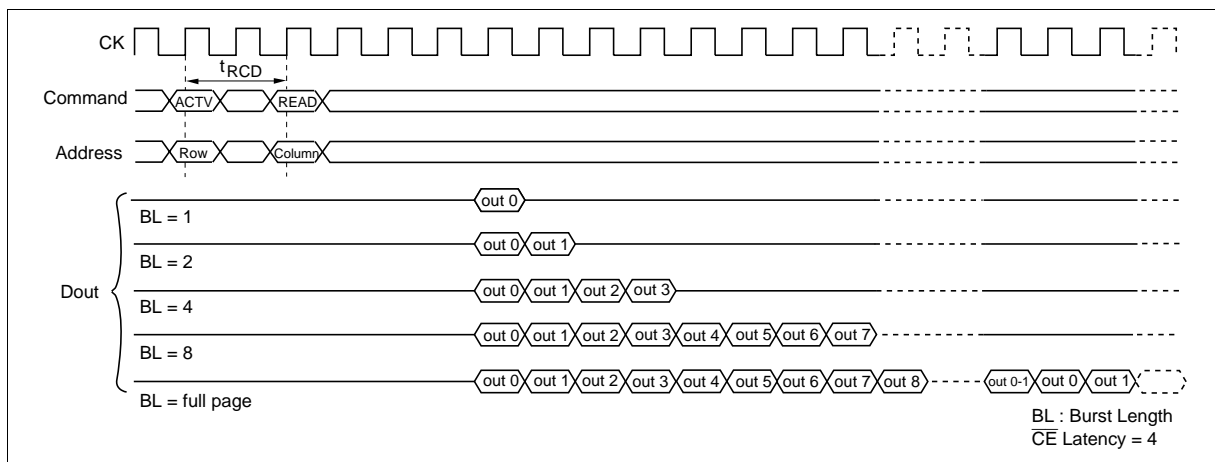
Write operation: Burst write or single write mode is selected by the OPCODE (A13, A12, A11, A10, A9, A8) of the mode register.

1. Burst write: A burst write operation is enabled by setting OPCODE (A9, A8) to (0, 0). A burst write starts in the next clock as a write command set. (The latency of data input is 1 clock.) The burst length can be set to 1, 2, 4, 8, and full-page, like burst read operations. The write start address is specified by the column address (and the bank select address (BA) at the write command set cycle.

$\overline{CE}$ Latency = 4

HITACHI
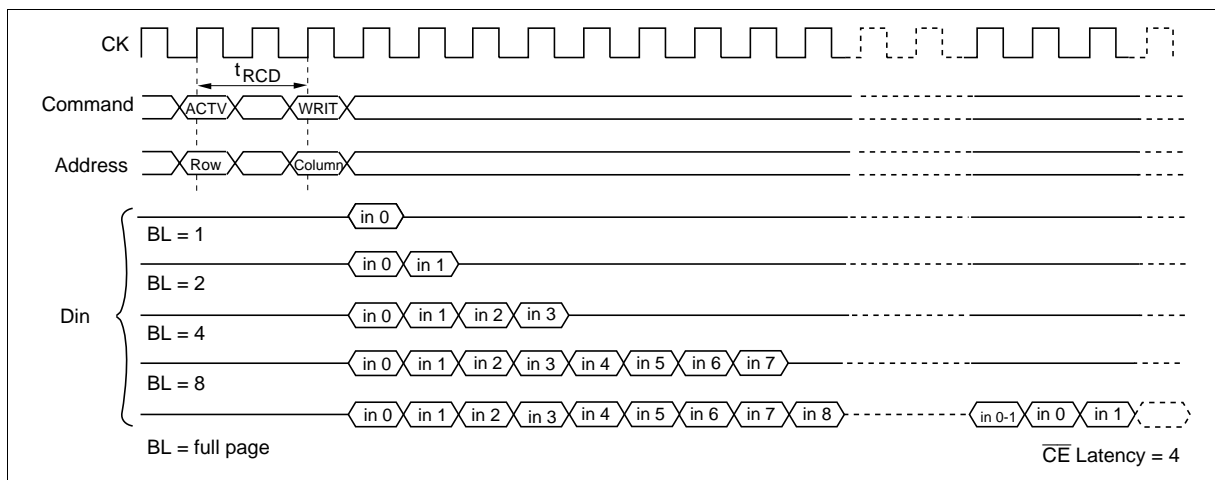
2. Single write: A single write operation is enabled by setting OPCODE (A9, A8) to (1, 0). In a single write operation, data is only written to the column address and the bank select address (BA) specified by the write command set cycle without regard to the burst length setting. (The latency of data input is 1 clock).
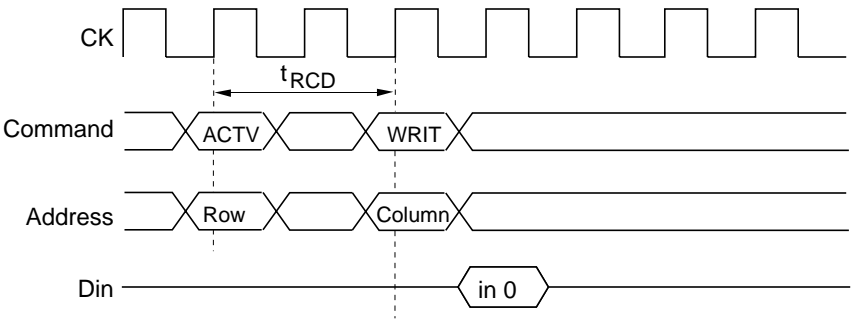
Auto Precharge

Read with auto-precharge: In this operation, since precharge is automatically performed after completing a read operation, a precharge command need not be executed after each read operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval defined by l_{APR} is required before execution of the next command.

$\overline{CE}$ latency	Precharge start cycle
3	1 cycle before the final data is output
4	2 cycle before the final data is output

Burst Read (Burst Length = 4)
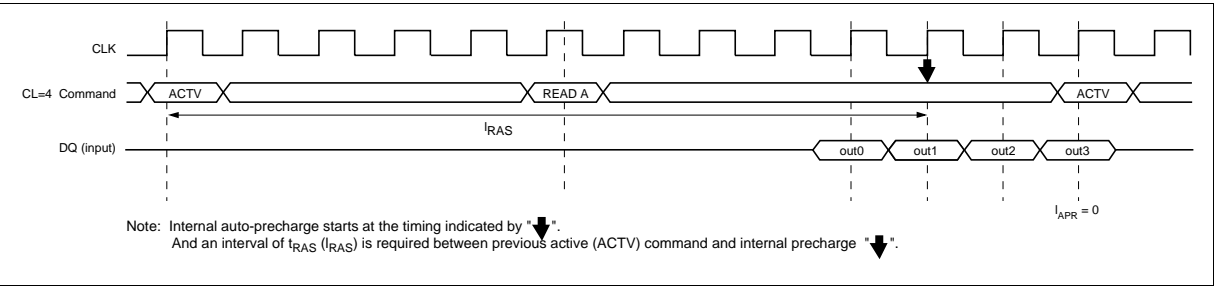
Note: Internal auto-precharge starts at the timing indicated by "⬇".
And an interval of t_{RAS} (l_{RAS}) is required between previous active (ACTV) command and internal precharge "⬇".

Write with auto-precharge: In this operation, since precharge is automatically performed after completing a burst write or single write operation, a precharge command need not be executed after each write operation. The command executed for the same bank after the execution of this command must be the bank active (ACTV) command. In addition, an interval of l_{APW} is required between the final valid data input and input of next command.

Burst Write (Burst Length = 4)
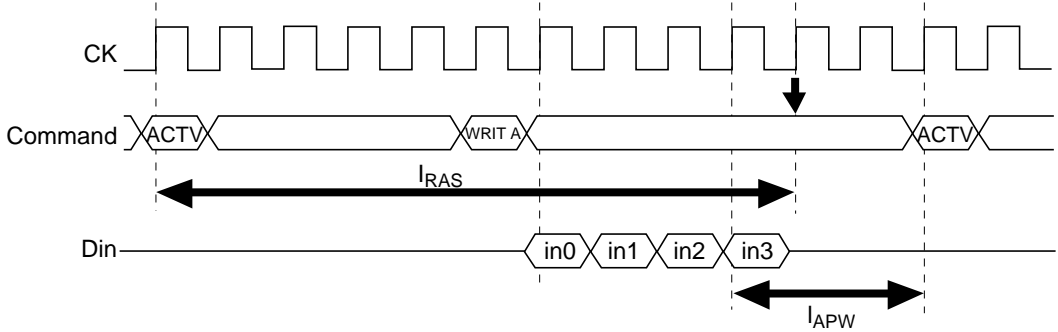
Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of t_{RAS} (l_{RAS}) is required between previous active (ACTV) command and internal precharge "↓".

Single Write
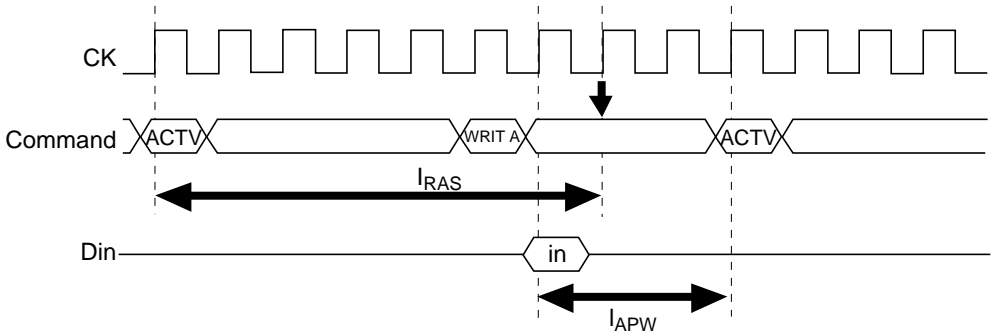
Note: Internal auto-precharge starts at the timing indicated by "↓".
and an interval of t_{RAS} (l_{RAS}) is required between previous active (ACTV) command and internal precharge "↓".

HITACHI

Full-page Burst Stop

Burst stop command during burst read: The burst stop (BST) command is used to stop data output during a full-page burst. The BST command sets the output buffer to High-Z and stops the full-page burst read. The timing from command input to the last data changes depending on the $\overline{CE}$ latency setting. In addition, the BST command is valid only during full-page burst mode, and is illegal with burst lengths 1, 2, 4 and 8.

$\overline{CE}$ latency	BST to valid data	BST to high impedance
3	2	3
4	3	4

$\overline{CE}$ Latency = 3, Burst Length = full page
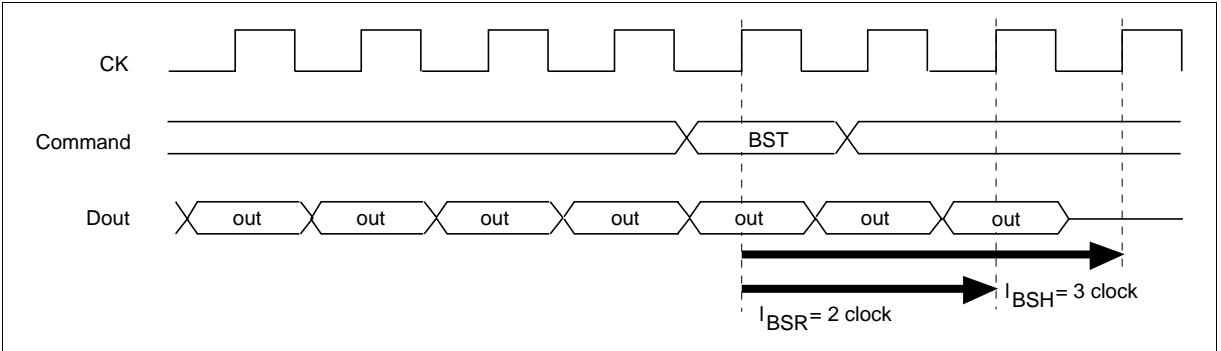
$\overline{CE}$ Latency = 4, Burst Length = full page
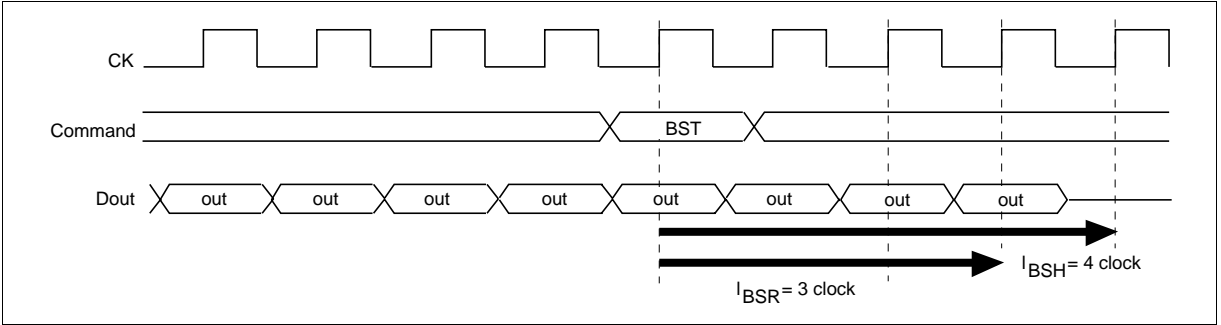
Burst stop command at burst write: The burst stop command (BST command) is used to stop data input during a full-page burst write. No data is written in the same clock as the BST command, and in subsequent clocks. In addition, the BST command is only valid during full-page burst mode, and is illegal with burst lengths of 1, 2, 4 and 8. And an interval of t_{DPL} is required between last data-in and the next precharge command.

HITACHI

Burst Length = full page
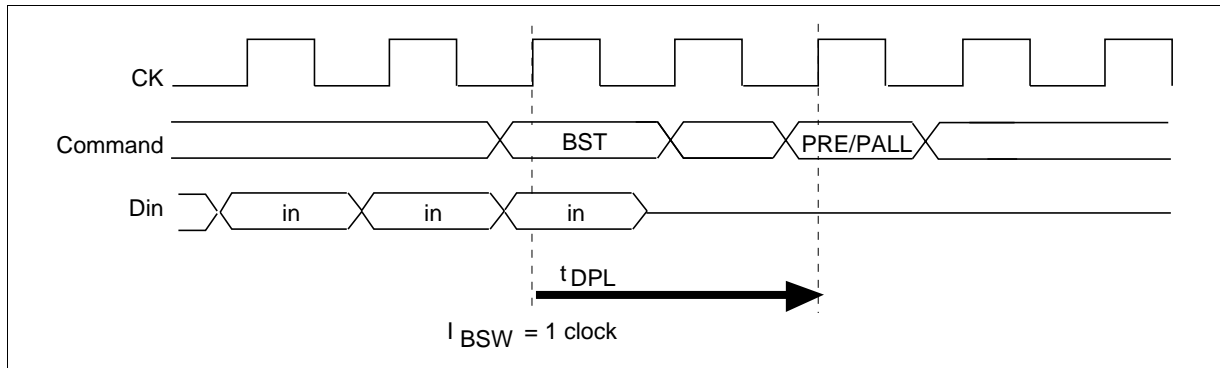
Command Intervals

Read command to Read command interval:

1. Same bank, same ROW address: When another read command is executed at the same ROW address of the same bank as the preceding read command execution, the second read can be performed after an interval of no less than 1 clock. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (same ROW address in same bank)
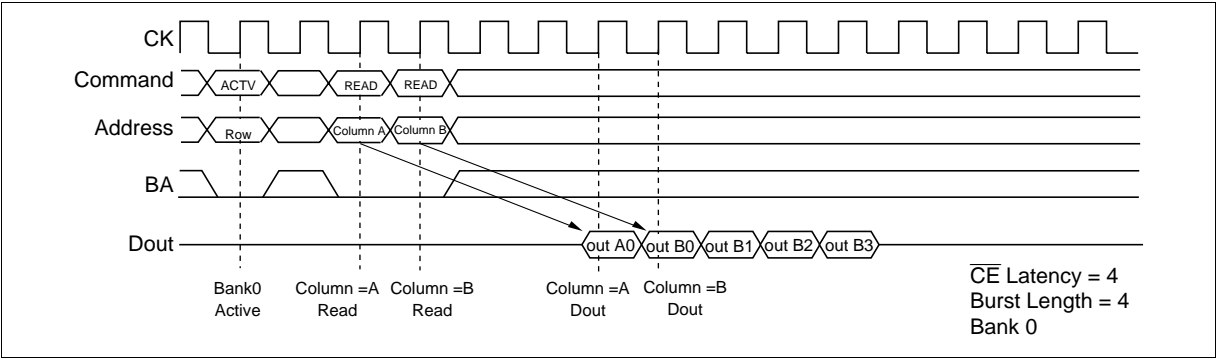
2. Same bank, different ROW address: When the ROW address changes on same bank, consecutive read commands cannot be executed; it is necessary to separate the two read commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the second read can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. Even when the first command is a burst read that is not yet finished, the data read by the second command will be valid.

READ to READ Command Interval (different bank)

HITACHI
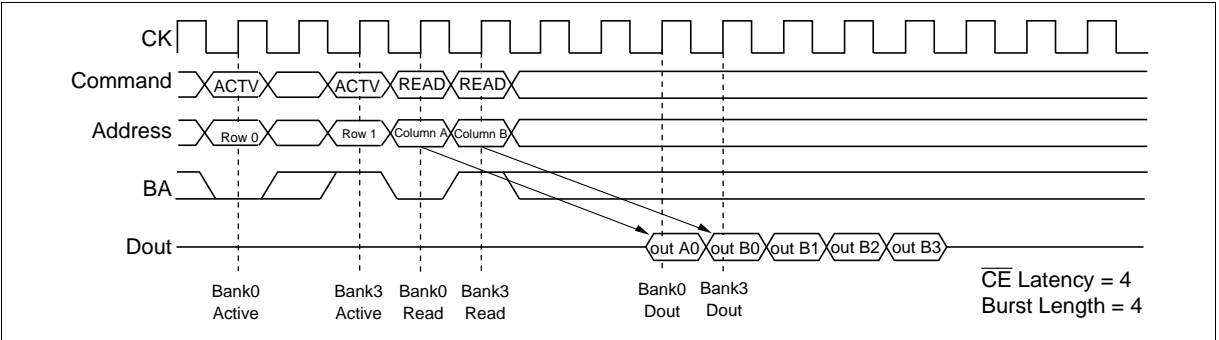
Write command to Write command interval:

1. Same bank, same ROW address: When another write command is executed at the same ROW address of the same bank as the preceding write command, the second write can be performed after an interval of no less than 1 clock. In the case of burst writes, the second write command has priority.

WRITE to WRITE Command Interval (same ROW address in same bank)
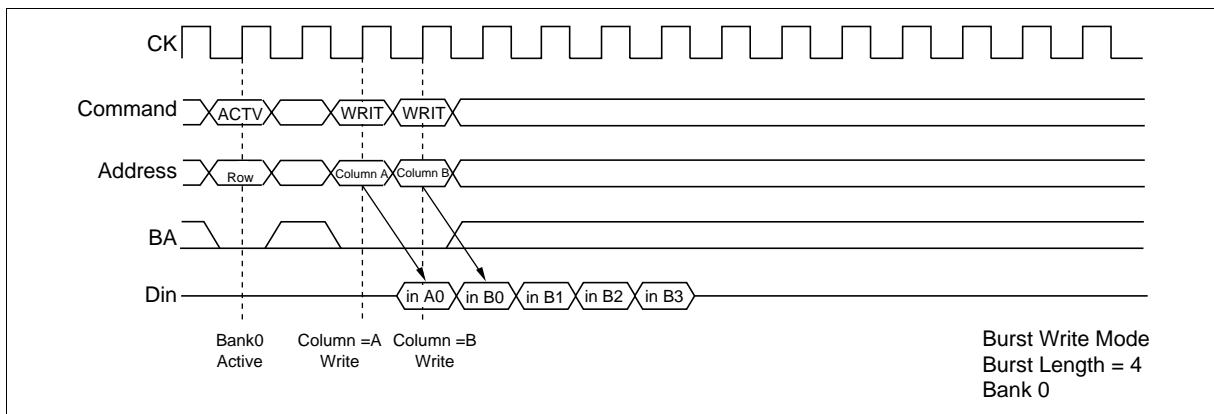
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two write commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the second write can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. In the case of burst write, the second write command has priority.

WRITE to WRITE Command Interval (different bank)

HITACHI
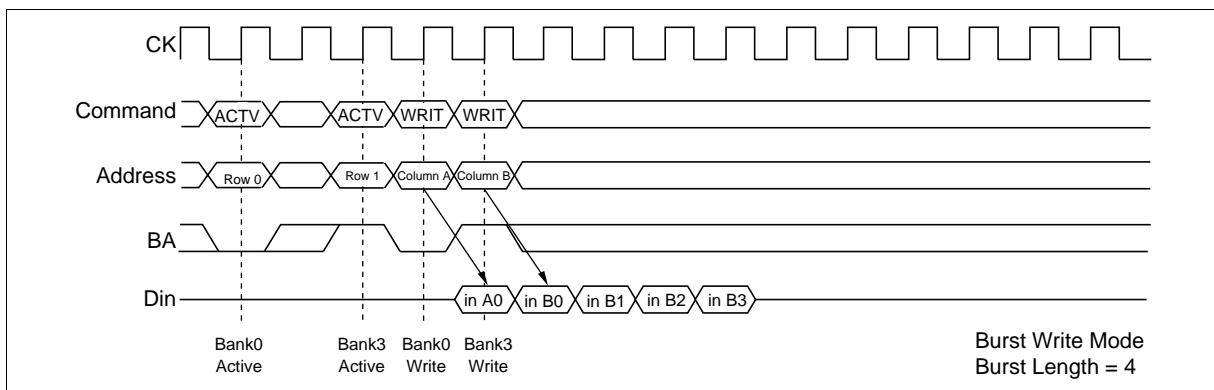
Read command to Write command interval:

1. Same bank, same ROW address: When the write command is executed at the same ROW address of the same bank as the preceding read command, the write command can be performed after an interval of no less than 1 clock. However, DQMB must be set High so that the output buffer becomes High-Z before data input.

READ to WRITE Command Interval (1)
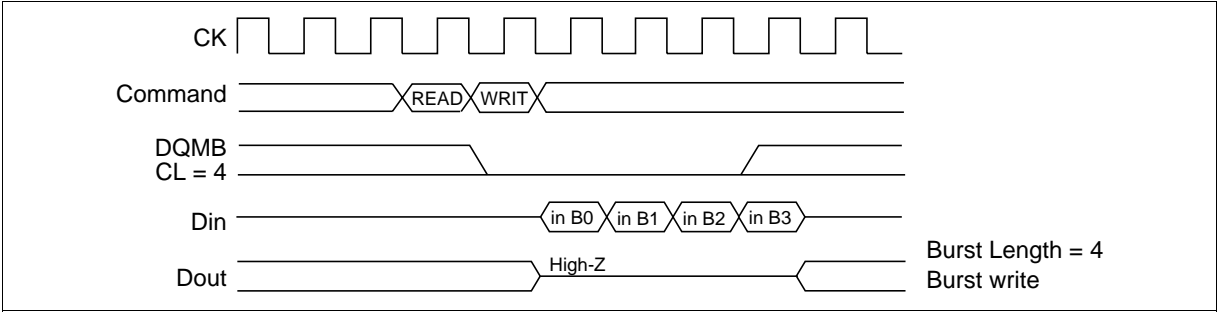
READ to WRITE Command Interval (2)
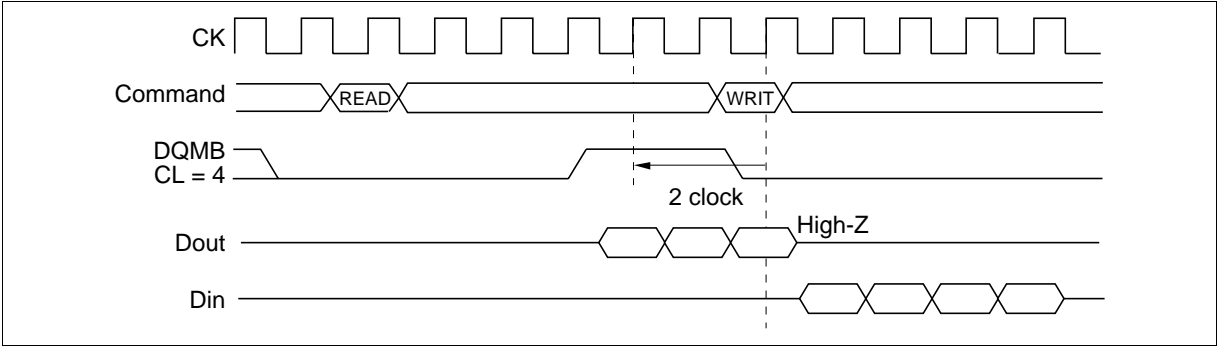
2. Same bank, different ROW address: When the ROW address changes, consecutive write commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the write command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. However, DQMB must be set High so that the output buffer becomes High-Z before data input.

HITACHI

Write command to Read command interval:

1. Same bank, same ROW address: When the read command is executed at the same ROW address of the same bank as the preceding write command, the read command can be performed after an interval of no less than 1 clock. However, in the case of a burst write, data will continue to be written until one cycle before the read command is executed.

WRITE to READ Command Interval (1)
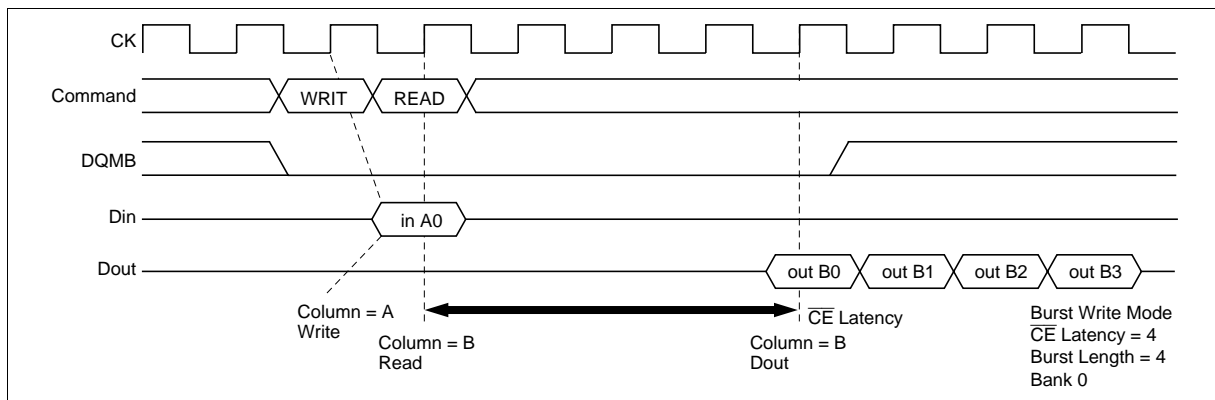
WRITE to READ Command Interval (2)
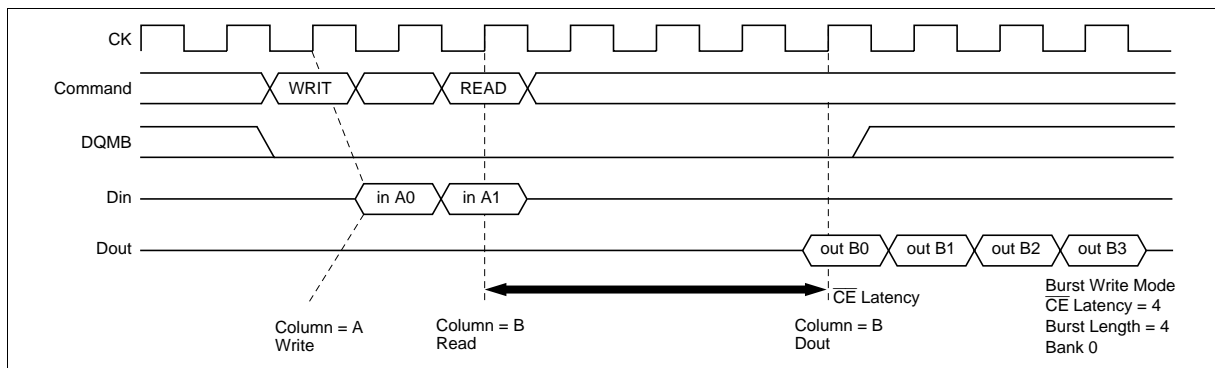
2. Same bank, different ROW address: When the ROW address changes, consecutive read commands cannot be executed; it is necessary to separate the two commands with a precharge command and a bank-active command.

3. Different bank: When the bank changes, the read command can be performed after an interval of no less than 1 clock, provided that the other bank is in the bank-active state. However, in the case of a burst write, data will continue to be written until one clock before the read command is executed (as in the case of the same bank and the same address).

HITACHI

Read with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. Even when the first read with auto-precharge is a burst read that is not yet finished, the data read by the second command is valid. The internal auto-precharge of one bank starts at the next clock of the second command.

Read with Auto Precharge to Read Command Interval (Different bank)

Note: Internal auto-precharge starts at the timing indicated by " ↓ ".
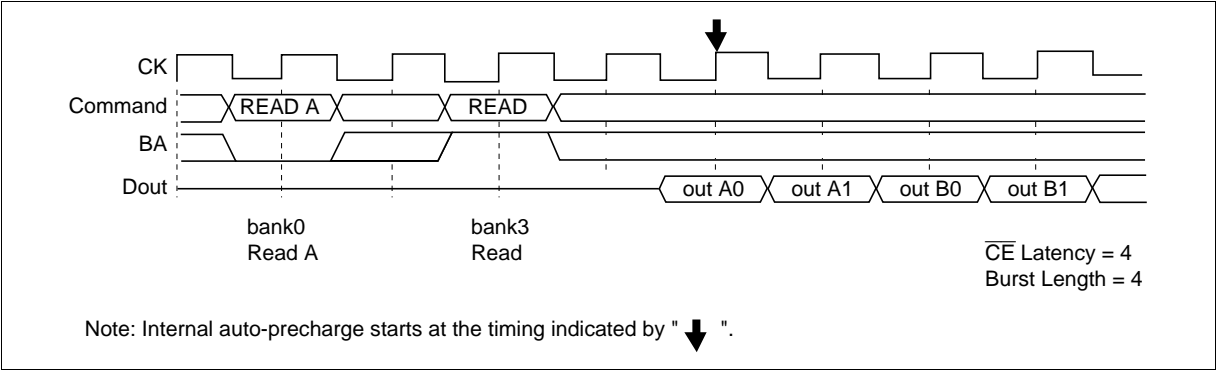
2. Same bank: The consecutive read command (the same bank) is illegal.

Write with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. In the case of burst writes, the second write command has priority. The internal auto-precharge of one bank starts at the next clock of the second command .

Write with Auto Precharge to Write Command Interval (Different bank)

Note: Internal auto-precharge starts at the timing indicated by " ↓ ".
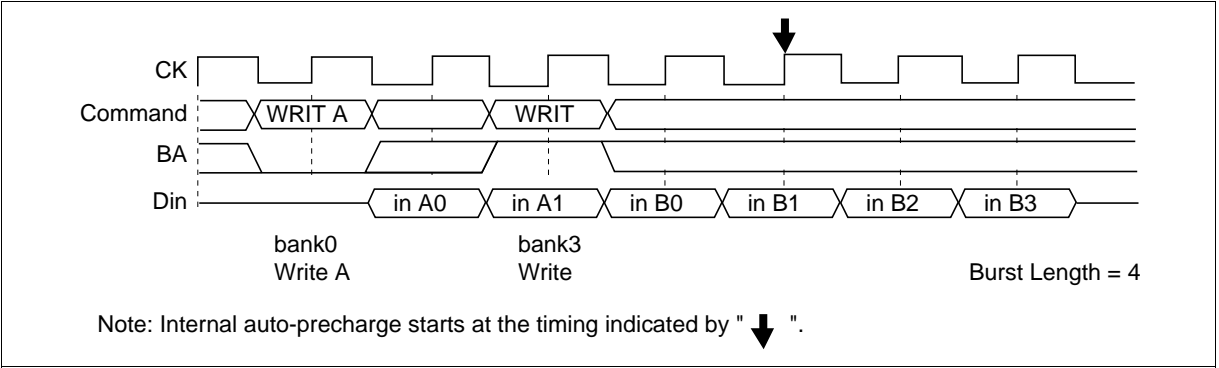
2. Same bank: The consecutive write command (the same bank) is illegal.

HITACHI

Read with auto precharge to Write command interval

1. Different bank: When some banks are in the active state, the second write command (another bank) is executed. However, DQMB must be set High so that the output buffer becomes High-Z before data input. The internal auto-precharge of one bank starts at the next clock of the second command.

Read with Auto Precharge to Write Command Interval (Different bank)
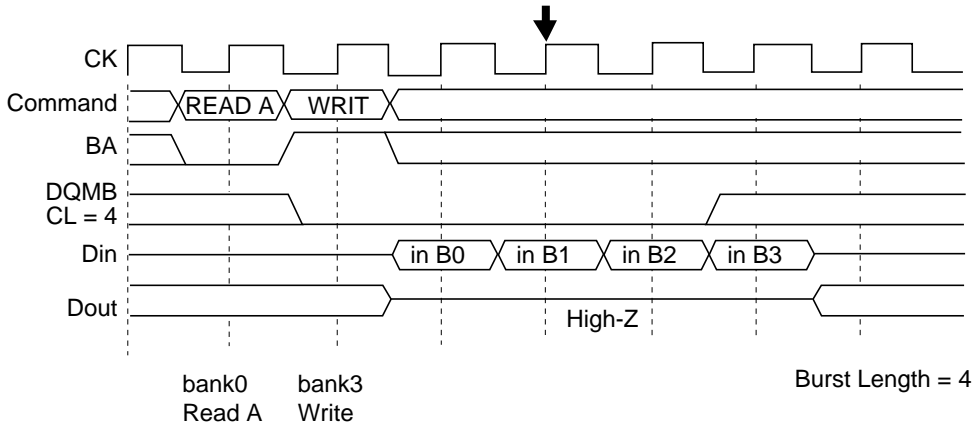
Note: Internal auto-precharge starts at the timing indicated by " ⬇ ".

2. Same bank: The consecutive write command from read with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

HITACHI

Write with auto precharge to Read command interval

1. Different bank: When some banks are in the active state, the second read command (another bank) is executed. However, in case of a burst write, data will continue to be written until one clock before the read command is executed. The internal auto-precharge of one bank starts at the next clock of the second command.

Write with Auto Precharge to Read Command Interval (Different bank)

bank0   bank3
Write A   Read

$\overline{CE}$ Latency = 4
Burst Length = 4

Note: Internal auto-precharge starts at the timing indicated by " ↓ ".
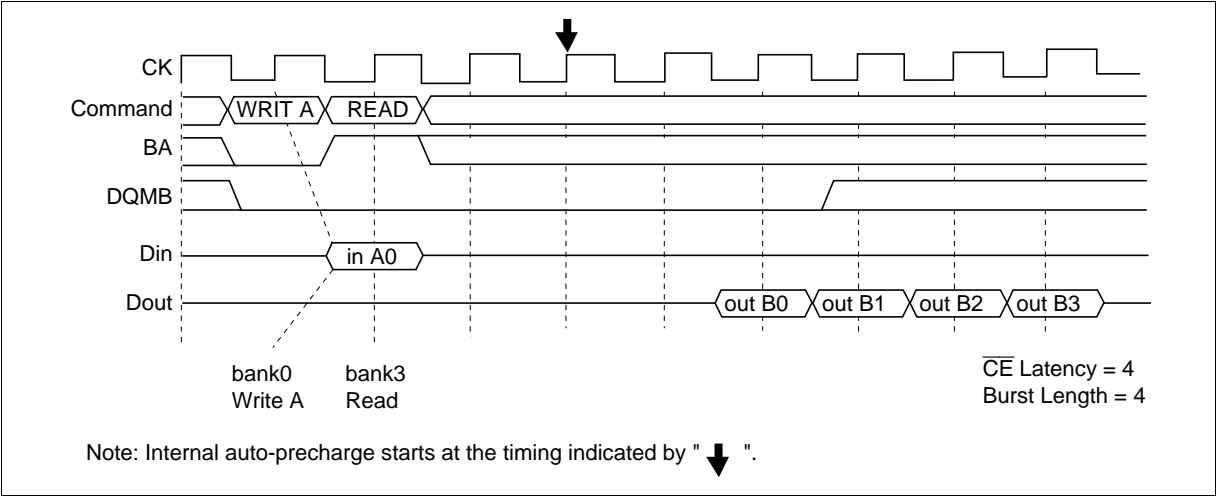
2. Same bank: The consecutive read command from write with auto precharge (the same bank) is illegal. It is necessary to separate the two commands with a bank active command.

HITACHI

Read command to Precharge command interval (same bank):

When the precharge command is executed for the same bank as the read command that preceded it, the minimum interval between the two commands is one clock. However, since the output buffer then becomes High-Z after the clocks defined by l_{HZP}, there is a case of interruption to burst read data output will be interrupted, if the precharge command is input during burst read. To read all data by burst read, the clocks defined by l_{EP} must be assured as an interval from the final data output to precharge command execution.

READ to PRECHARGE Command Interval (same bank): To output all data

$\overline{CE}$ Latency = 3, Burst Length = 4

$\overline{CE}$ Latency = 4, Burst Length = 4

HITACHI
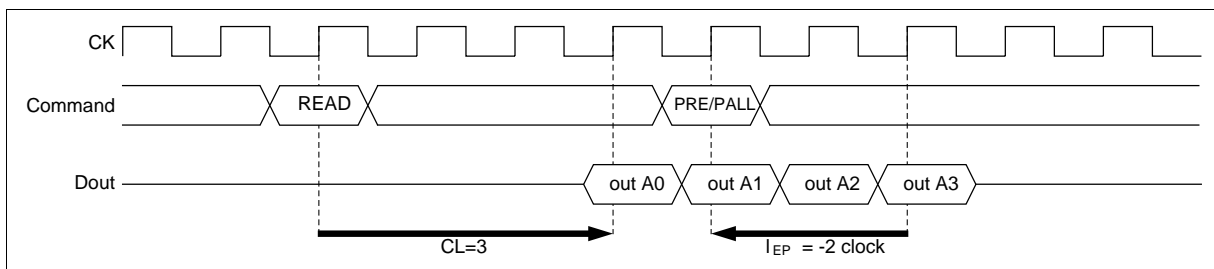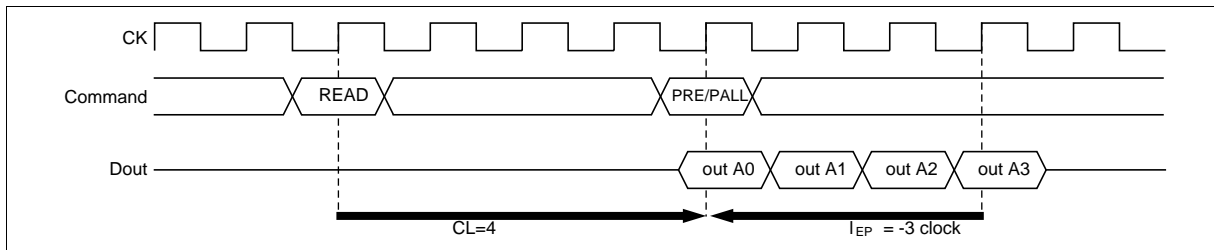
READ to PRECHARGE Command Interval (same bank): To stop output data

$\overline{\text{CE}}$ **Latency = 3, Burst Length = 1, 2, 4, 8, full page burst**
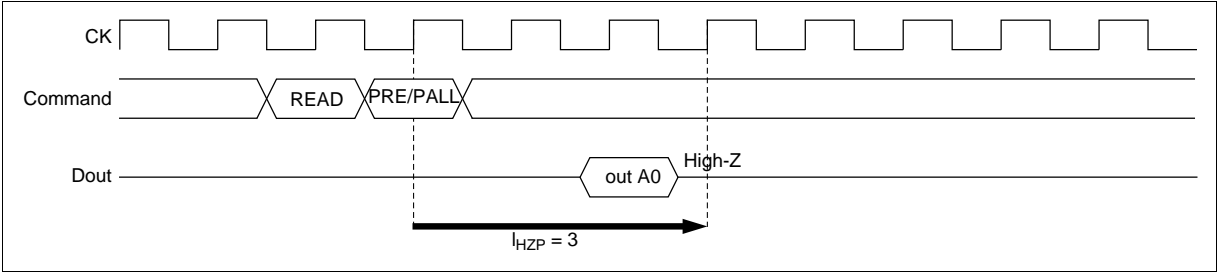
$\overline{\text{CE}}$ **Latency = 4, Burst Length = 1, 2, 4, 8, full page burst**

HITACHI
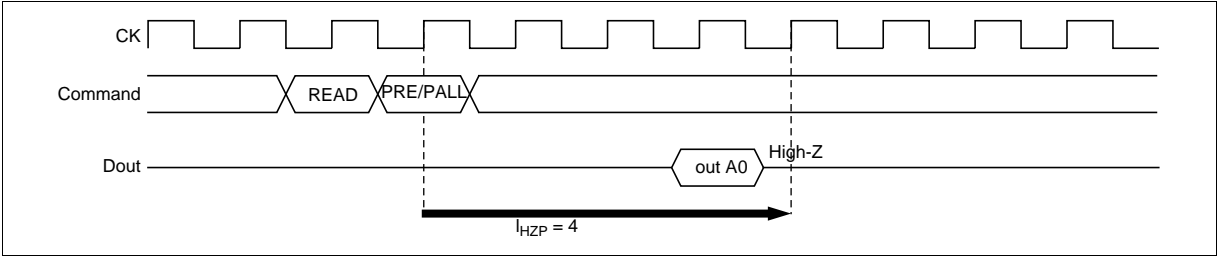
Write command to Precharge command interval (same bank): When the precharge command is executed for the same bank as the write command that preceded it, the minimum interval between the two commands is 1 clock. However, if the burst write operation is unfinished, the input data must be masked by means of DQMB for assurance of the clock defined by t_{DPL}.

WRITE to PRECHARGE Command Interval (same bank):

Burst Length = 4 (To stop write operation)
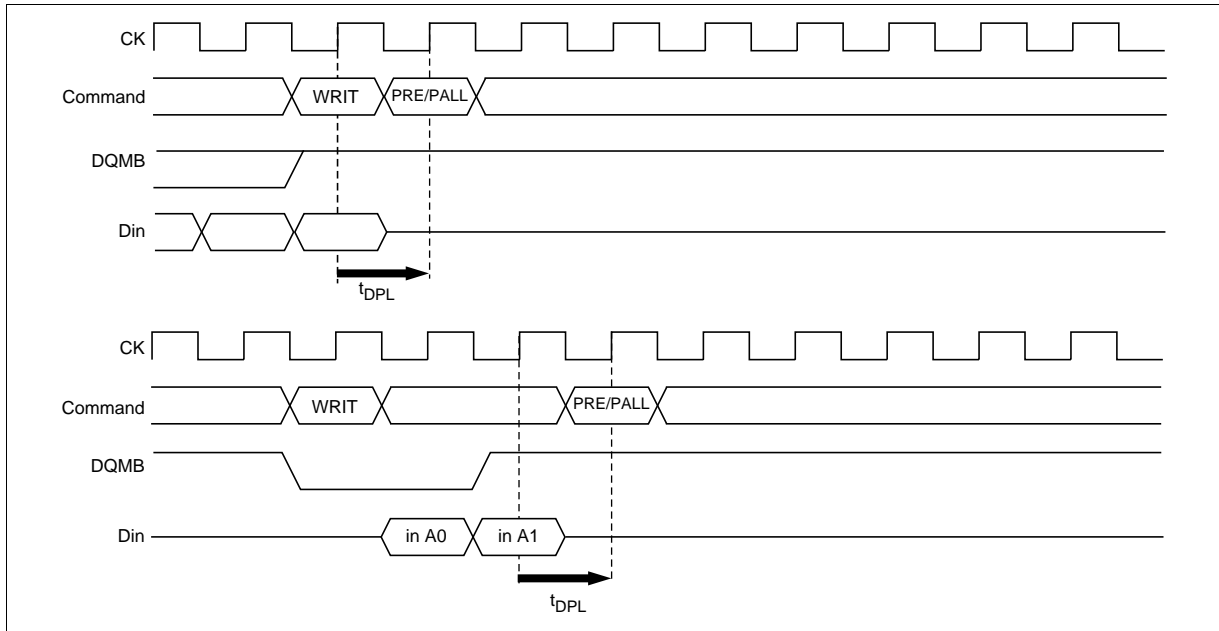
Burst Length = 4 (To write all data)
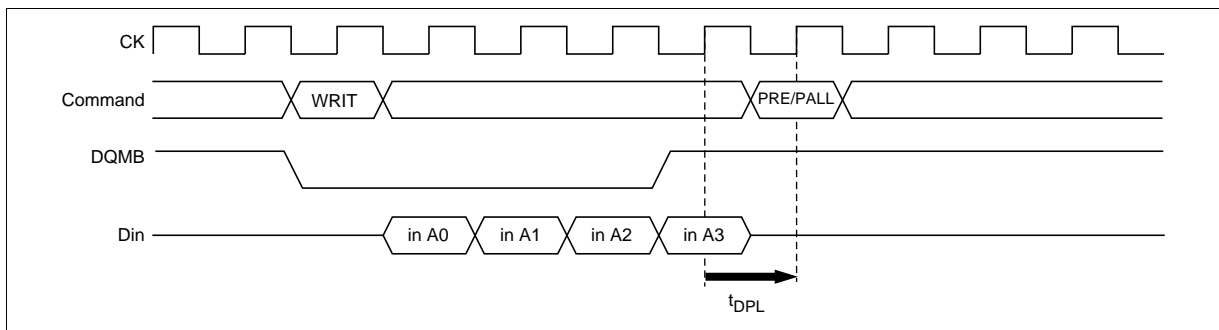
Bank active command interval:

1. Same bank: The interval between the two bank-active commands must be no less than t_{RC}.

Bank Active to Bank Active for Same Bank
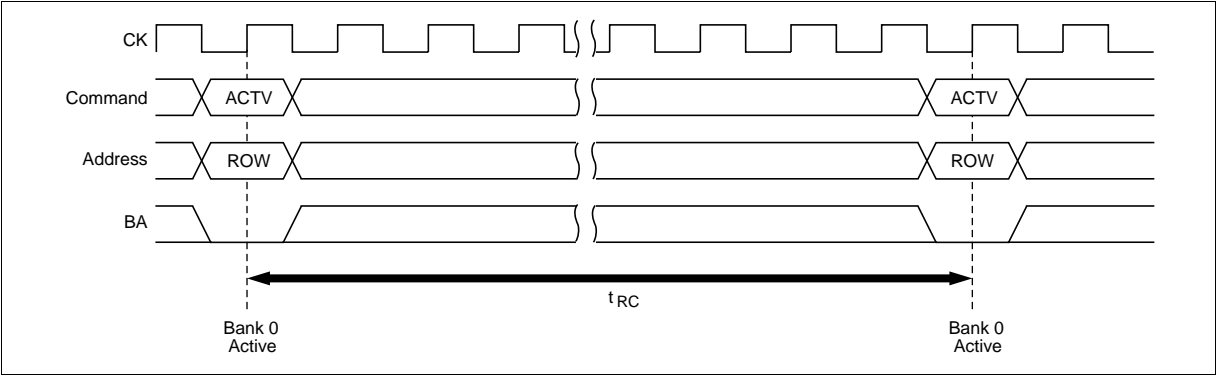
2. In the case of different bank-active commands: The interval between the two bank-active commands must be no less than t_{RRD}.

Bank Active to Bank Active for Different Bank
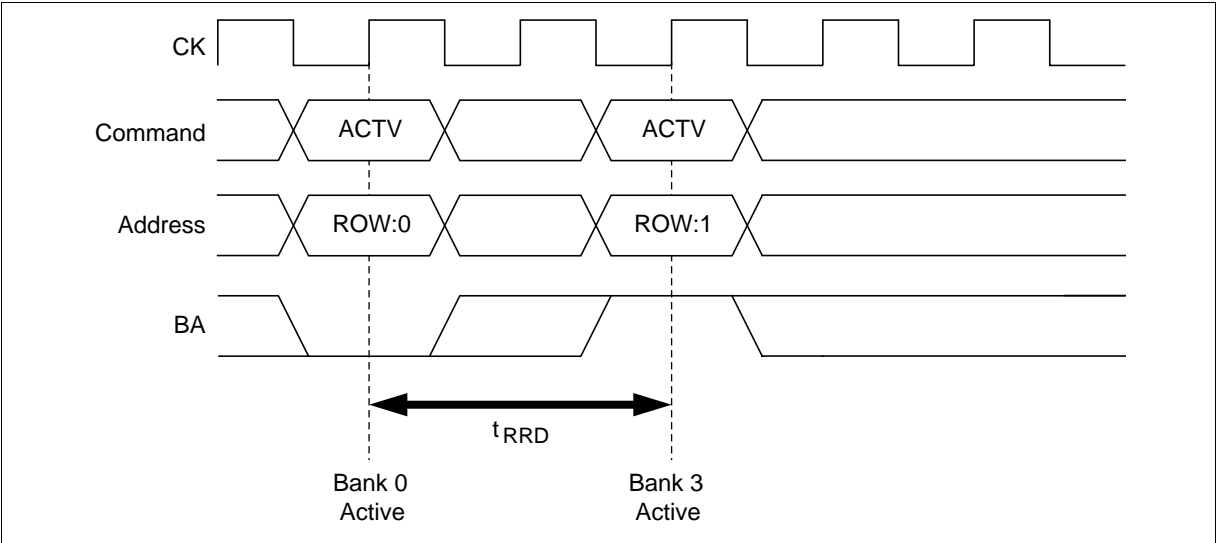
Mode register set to Bank-active command interval: The interval between setting the mode register and executing a bank-active command must be no less than l_{RSA}.
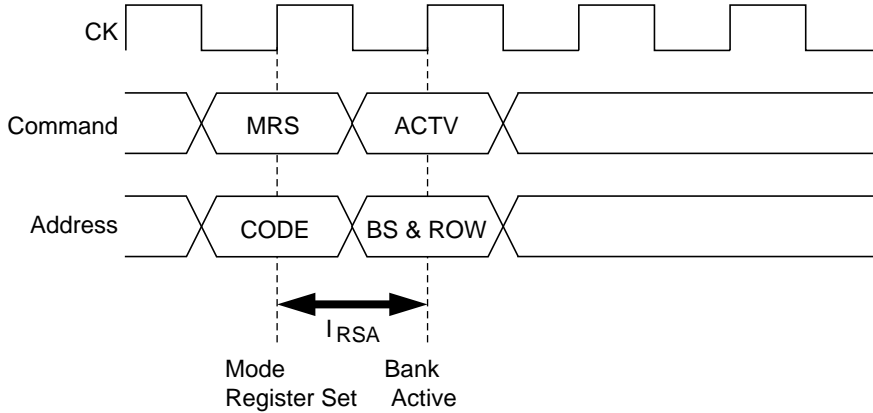
DQMB Control

The DQMB mask the DQ data. The timing of DQMB is different during reading and writing.

Reading: When data is read, the output buffer can be controlled by DQMB. By setting DQMB to Low, the output buffer becomes Low-Z, enabling data output. By setting DQMB to High, the output buffer becomes High-Z, and the corresponding data is not output. However, internal reading operations continue. The latency of DQMB during reading is 3 clocks.

Writing: Input data can be masked by DQMB. By setting DQMB to Low, data can be written. In addition, when DQMB is set to High, the corresponding data is not written, and the previous data is held. The latency of DQMB during writing is 1 clock.

HITACHI

Reading

CK

DQMB

Dout

out 0 out 1 High-Z out 3

I_{DOD} = 3 Latency

Writing

CK

DQMB

Din

in 0 in 1 in 3

I_{DID} = 1 Latency

HITACHI
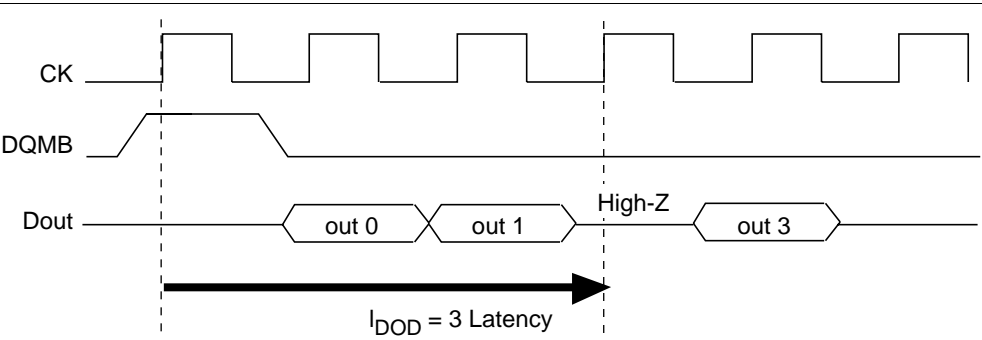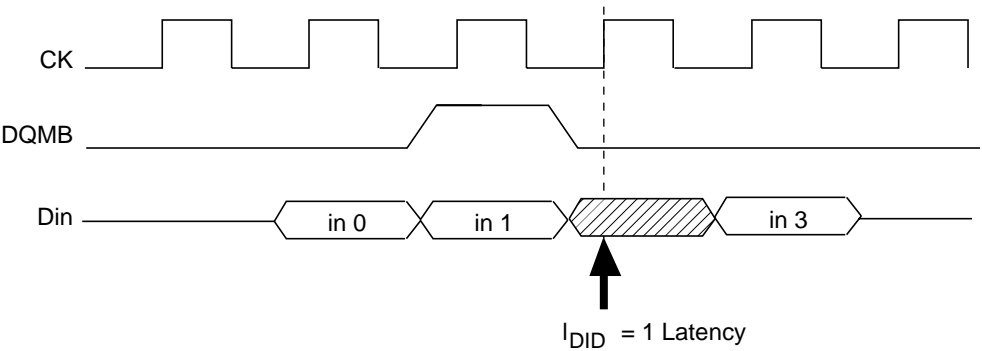
Refresh

Auto-refresh: All the banks must be precharged before executing an auto-refresh command. Since the auto-refresh command updates the internal counter every time it is executed and determines the banks and the ROW addresses to be refreshed, external address specification is not required. The refresh cycle is 4096 cycles/64 ms. (4096 cycles are required to refresh all the ROW addresses.) The output buffer becomes High-Z after auto-refresh start. In addition, since a precharge has been completed by an internal operation after the auto-refresh, an additional precharge operation by the precharge command is not required.

Self-refresh: After executing a self-refresh command, the self-refresh operation continues while CKE is held Low. During self-refresh operation, all ROW addresses are refreshed by the internal refresh timer. A self-refresh is terminated by a self-refresh exit command. Before and after self-refresh mode, execute auto-refresh to all refresh addresses in or within 64 ms period on the condition (1) and (2) below.

(1) Enter self-refresh mode within 15.6 µs after either burst refresh or distributed refresh at equal interval to all refresh addresses are completed.
(2) Start burst refresh or distributed refresh at equal interval to all refresh addresses within 15.6 µs after exiting from self-refresh mode.

Others

Power-down mode: The SDRAM module enters power-down mode when CKE goes Low in the IDLE state. In power down mode, power consumption is suppressed by deactivating the input initial circuit. Power down mode continues while CKE is held Low. In addition, by setting CKE to High, the SDRAM module exits from the power down mode, and command input is enabled from the next clock. In this mode, internal refresh is not performed.

Clock suspend mode: By driving CKE to Low during a bank-active or read/write operation, the SDRAM module enters clock suspend mode. During clock suspend mode, external input signals are ignored and the internal state is maintained. When CKE is driven High, the SDRAM module terminates clock suspend mode, and command input is enabled from the next clock. For details, refer to the "CKE Truth Table".

Power-up sequence: The SDRAM module should be gone on the following sequence with power up.

The CK, CKE, $\overline{S}$, DQMB and DQ pins keep low till power stabilizes.
The CK pin is stabilized within 100 µs after power stabilizes before the following initialization sequence.
The CKE and DQMB is driven to high between power stabilizes and the initialization sequence.

This SDRAM module has V_{CC} clamp diodes for CK, CKE, $\overline{S}$, DQMB and DQ pins. If these pins go high before power up, the large current flows from these pins to V_{CC} through the diodes.

Initialization sequence: When 200 µs or more has past after the above power-up sequence, all banks must be precharged using the precharge command (PALL). After t_{RP} delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. We recommend that by keeping DQM, DQMU/DQML to High, the output buffer becomes High-Z during Initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.

HITACHI

Initialization sequence: When 200 µs or more has past after the above power-up sequence, all banks must be precharged using the precharge command (PALL). After t_{RP} delay, set 8 or more auto refresh commands (REF). Set the mode register set command (MRS) to initialize the mode register. We recommend that by keeping DQMB to High, the output buffer becomes High-Z during Initialization sequence, to avoid DQ bus contention on memory system formed with a number of device.

Stabilization time: The PLL requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required following power-up. So this SDRAM module needs dammy cycle for 50 µs after power-up.
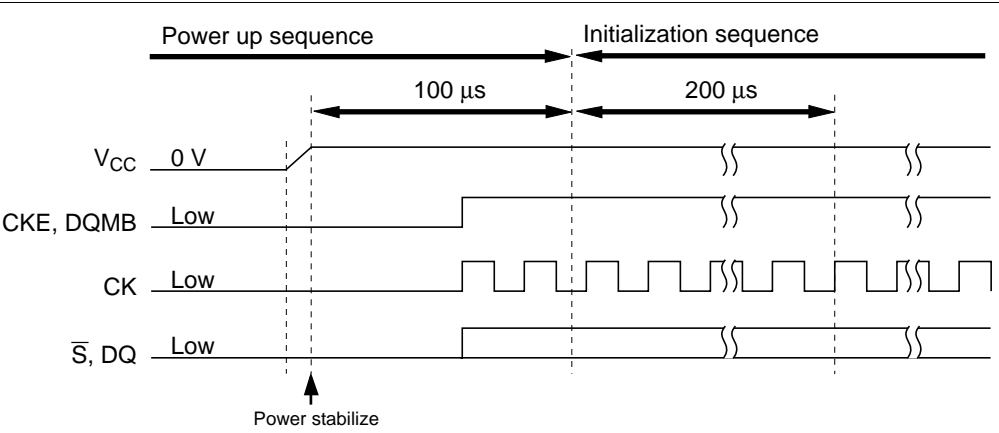
Timing Waveforms

Read Cycle

Write Cycle

HITACHI
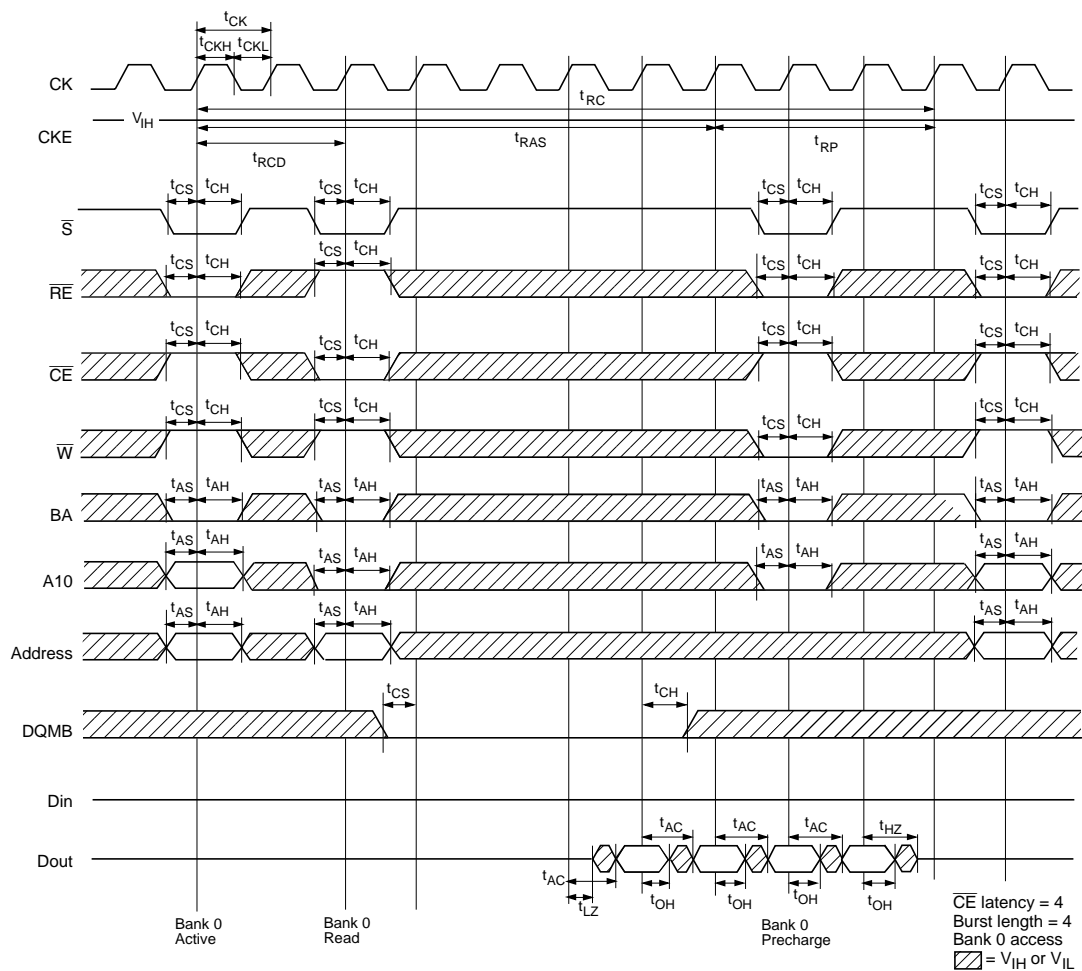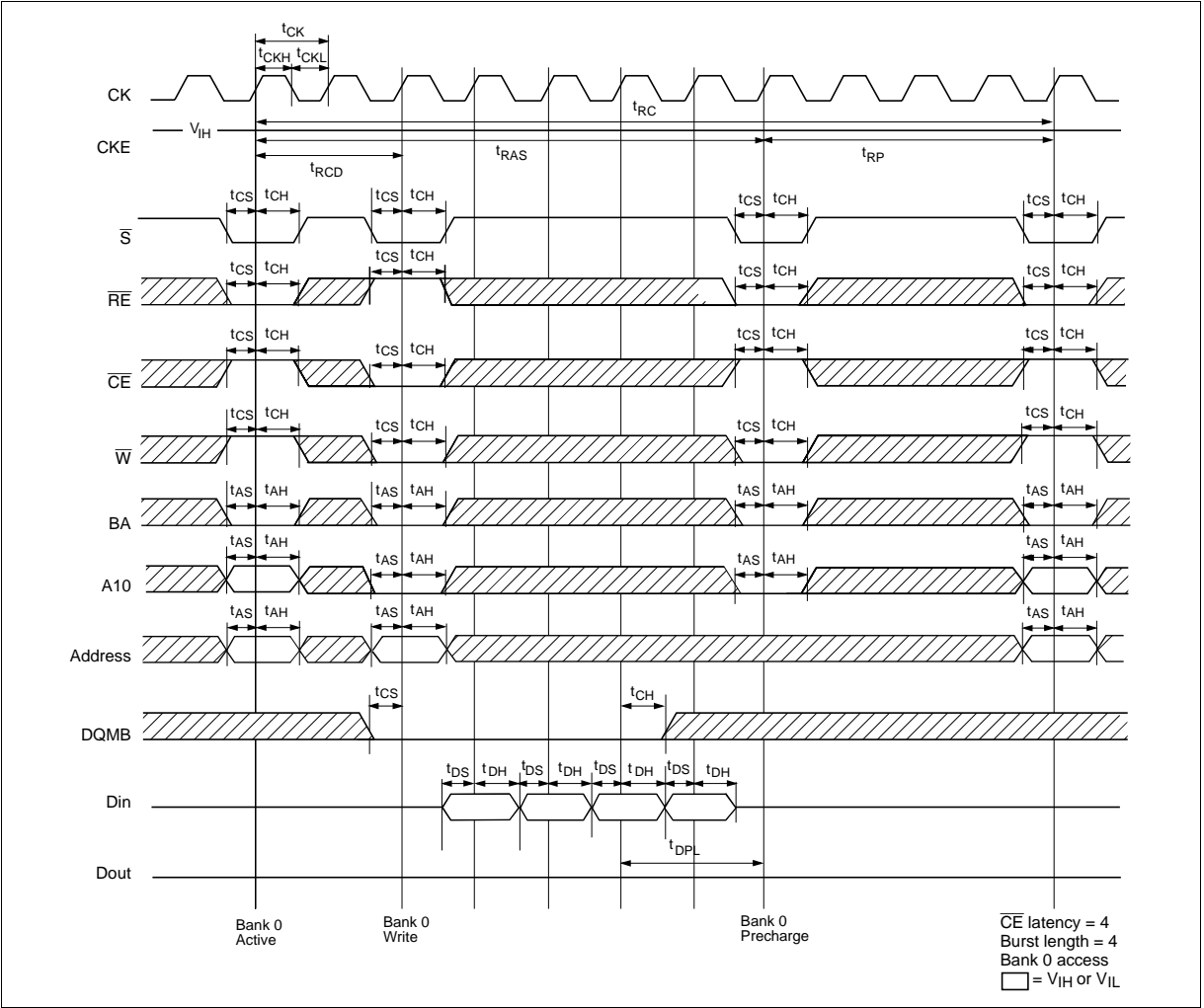
Mode Register Set Cycle

Read Cycle/Write Cycle

HITACHI
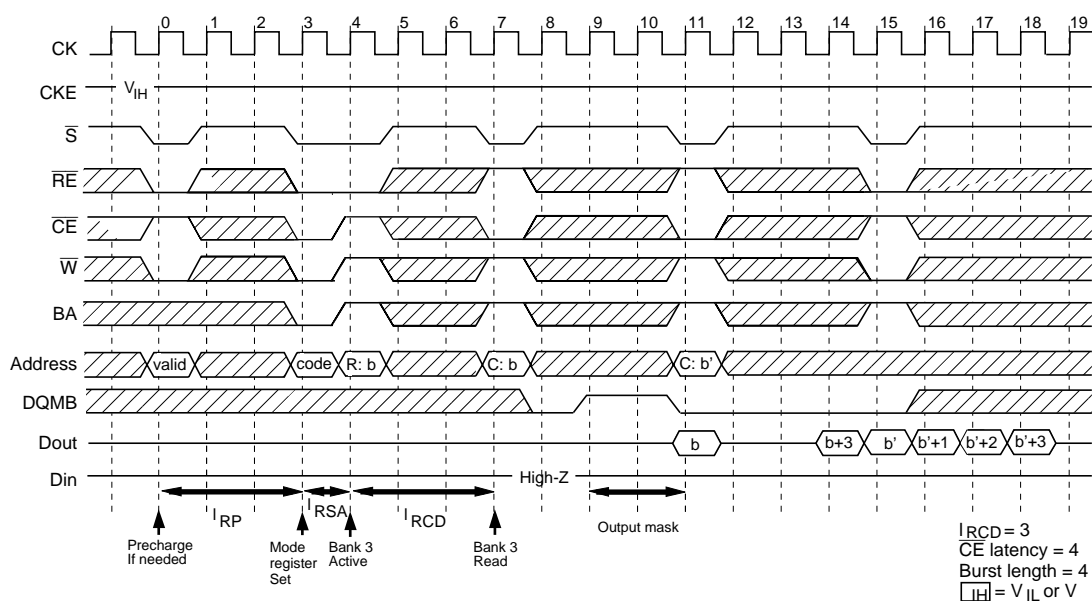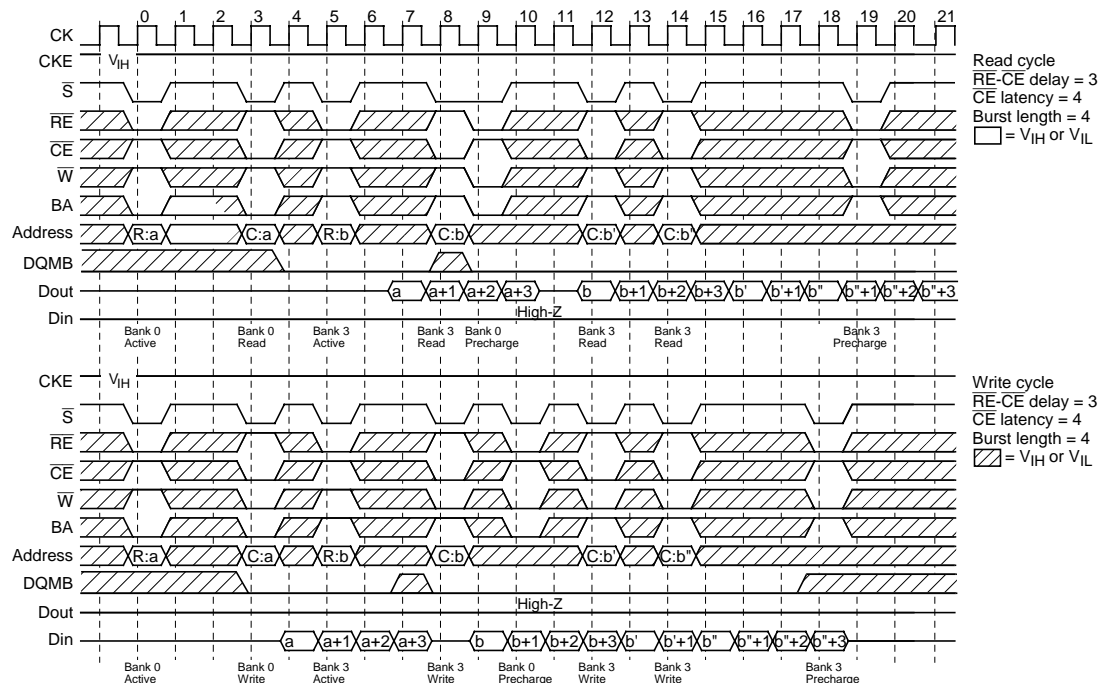
Read/Single Write Cycle

Read/Single write
$\overline{RE}$, $\overline{CE}$ delay = 3
$\overline{CE}$ latency = 4
Burst length = 4
⬡ = V_{IH} or V_{IL}

Read/Burst Write Cycle

Read/Burst write
$\overline{RE}$, $\overline{CE}$ delay = 3
$\overline{CE}$ latency = 4
Burst length = 4
☐ = V$_{IH}$ or V$_{IL}$

HITACHI

HB52RF329E2-75F
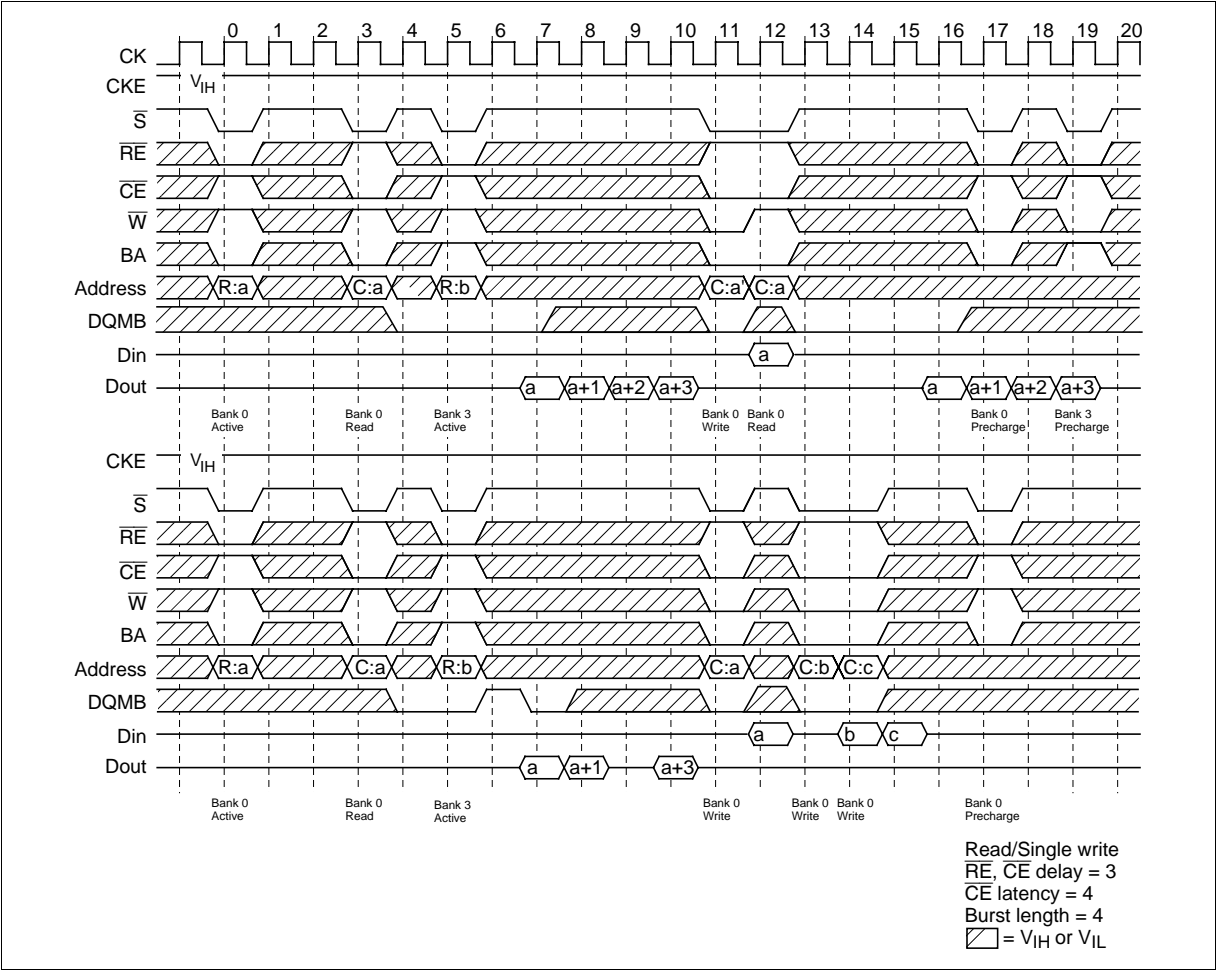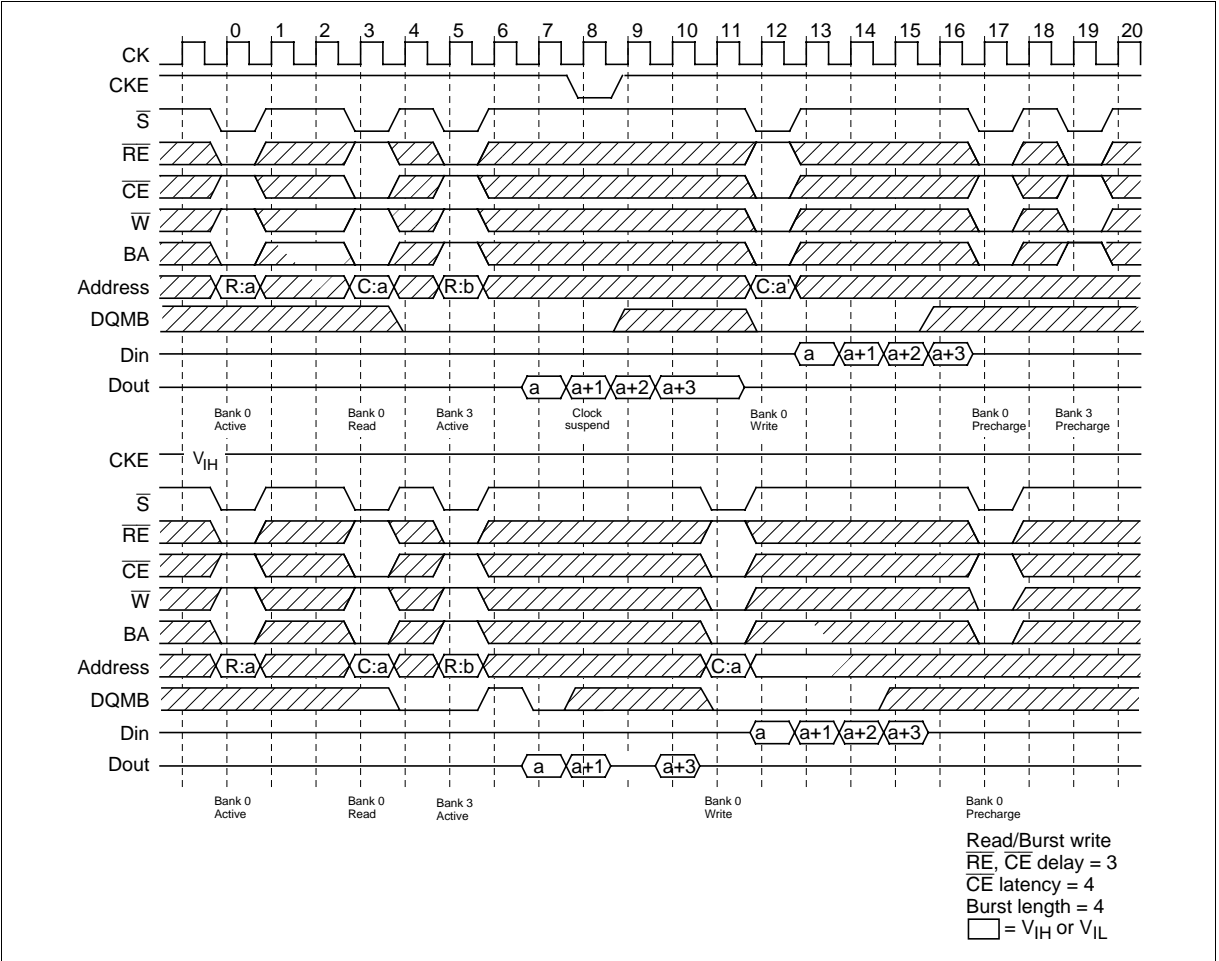
Full Page Read/Write Cycle
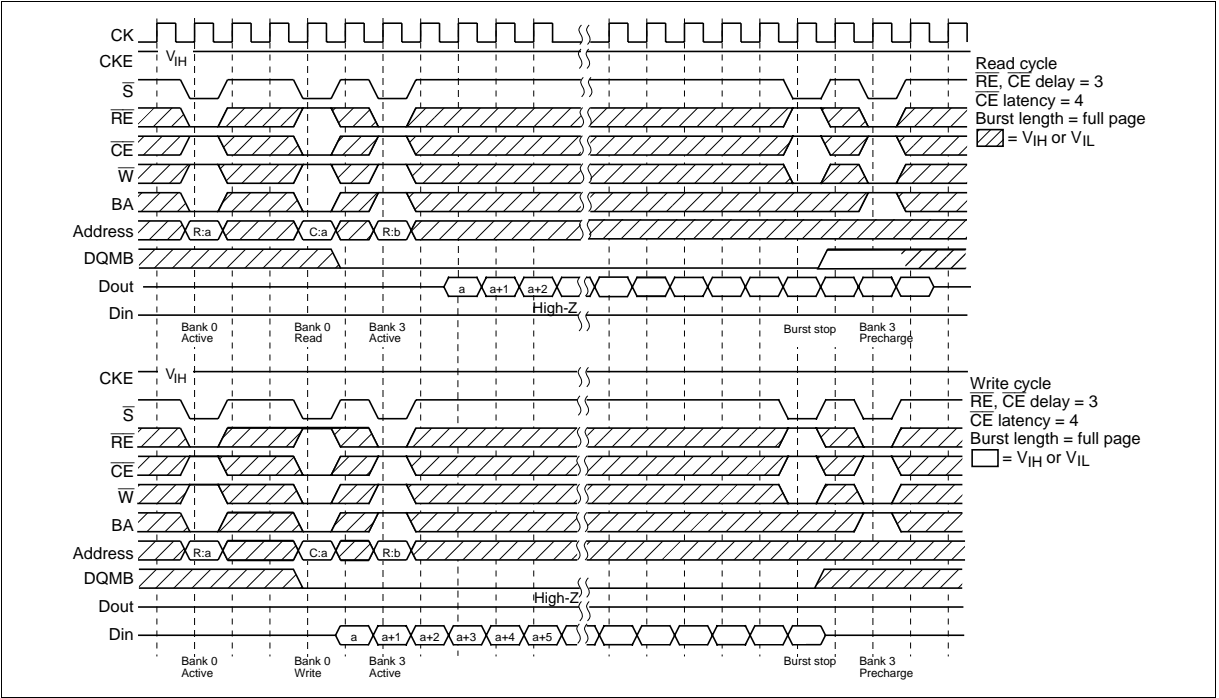
HITACHI
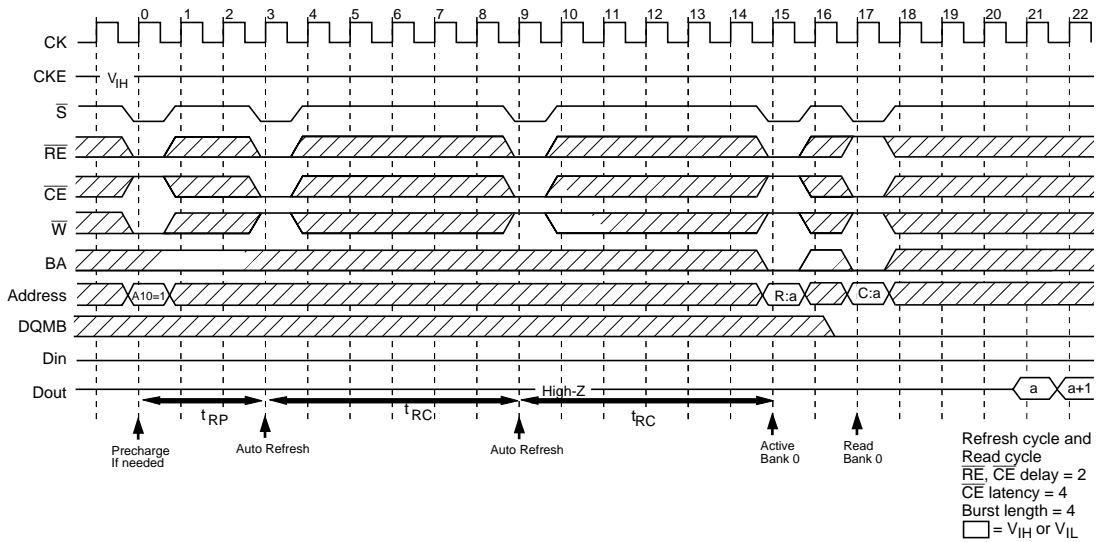
Auto Refresh Cycle

Self Refresh Cycle
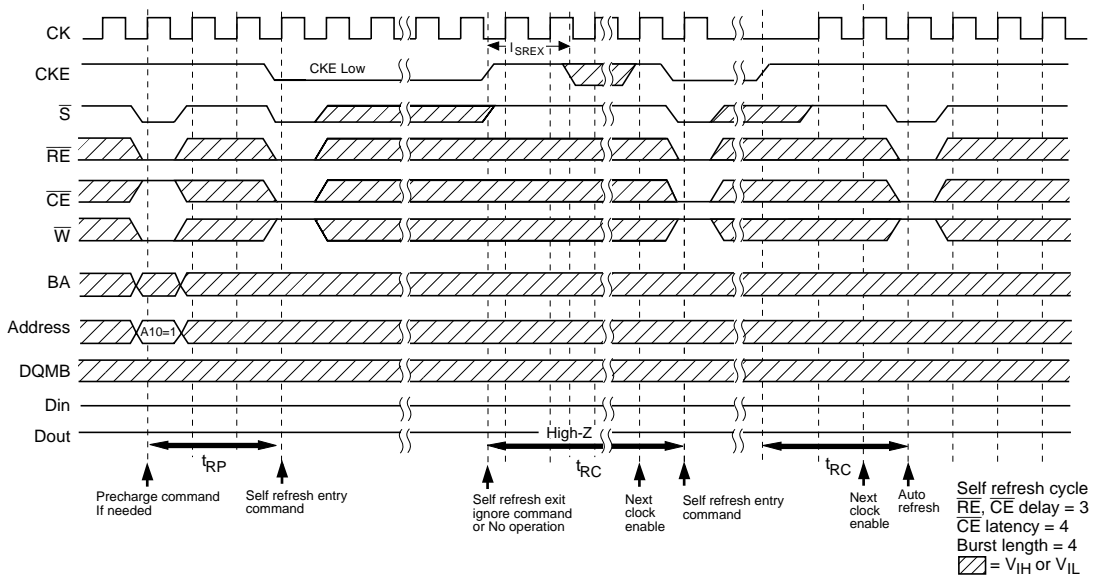
HITACHI

Clock Suspend Mode

HITACHI

Power Down Mode

Initialization Sequence

HITACHI

Physical Outline

Front side

Unit: mm/inch

133.37
5.251

3.00
0.118

127.35
5.014

4.80
0.189

Component area
(Front)

3.00
0.118

4.00 min
0.157 min

1
84

C
B
A

8.89
0.350

11.43
0.450

36.83
1.450

54.61
2.150

1.27 ± 0.10
0.050 ± 0.004

Back side

2 − φ 3.00
2 − φ 0.118

98
89

Component area
(Back)

4.00
0.157

17.78
0.700

38.10
1.500

Detail A

2.54 min
0.100 min

1.27
0.050

0.25 max
0.010 max

1.00 ± 0.05
0.039 ± 0.002

Detail B

3.175
0.125

6.35
0.250

2.00 ± 0.10
0.079 ± 0.004

3.125 ± 0.125
0.123 ± 0.005

Detail C

4.175
0.164

6.35
0.250

2.00 ± 0.10
0.079 ± 0.004

3.125 ± 0.125
0.123 ± 0.005

Note: Tolerance on all dimensions ± 0.15/0.006 unless otherwise specified.

HITACHI

Cautions

1. Hitachi neither warrants nor grants licenses of any rights of Hitachi's or any third party's patent, copyright, trademark, or other intellectual property rights for information contained in this document. Hitachi bears no responsibility for problems that may arise with third party's rights, including intellectual property rights, in connection with use of the information contained in this document.

2. Products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.

3. Hitachi makes every attempt to ensure that its products are of high quality and reliability. However, contact Hitachi's sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

4. Design your application so that the product is used within the ranges guaranteed by Hitachi particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. Hitachi bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail-safes, so that the equipment incorporating Hitachi product does not cause bodily injury, fire or other consequential damage due to operation of the Hitachi product.

5. This product is not designed to be radiation resistant.

6. No one is permitted to reproduce or duplicate, in any form, the whole or part of this document without written approval from Hitachi.

7. Contact Hitachi's sales office for any questions regarding this document or Hitachi semiconductor products.

HITACHI

HITACHI

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 30, 1999	Initial issue (referred to HM5264165F/HM5264805F HM5264405F-75/A60/B60 rev 0.1)	S. Tsukui	K. Tsuneda
1.0	Jan. 18, 2000	(referred to HM5264165F/HM5264805F/HM5264405F-75/A60/B60 rev 1.0) CKE Truth Table Clock suspend mode entry ($\overline{\text{S}}$): H to ×		

HITACHI