FAIRCHILD SEMICONDUCTOR®

July 2008

FDB024N06

N-Channel PowerTrench® MOSFET

60V, 265A, 2.4mΩ

Features

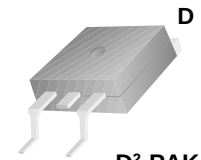
- $R_{DS(on)}$ = 1.8mΩ (Typ.) @ V_{GS} = 10V, I_D = 75A
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low $R_{DS(on)}$
- High power and current handling capability
- RoHS compliant

General Description

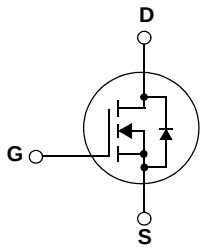
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Application

- DC to DC convertors / Synchronous Rectification



D²-PAK
FDB Series



MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V_{DSS}	Drain to Source Voltage		60	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current - Continuous (T_C = 25°C, Silicon Limited)		265*	A
	- Continuous (T_C = 100°C, Silicon Limited)		190*	A
	- Continuous (T_C = 25°C, Package Limited)		120	A
I_{DM}	Drain Current	- Pulsed (Note 1)	1060	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	2531	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	3.5	V/ns
P_D	Power Dissipation	(T_C = 25°C)	395	W
		- Derate above 25°C	2.6	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300	°C

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	Ratings	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.38	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	

Package Marking and Ordering Information $T_C = 25^oC$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB024N06	FDB024N06	D2-PAK	330mm	24mm	800

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, T_C= 25°C	60	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.04	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 60V, V_{GS} = 0V	-	-	1	μA
		V_{DS} = 60V, V_{GS} = 0V, T_C = 150°C	-	-	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20V, V_{DS} = 0V	-	-	±100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	2.5	3.5	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 75A	-	1.8	2.4	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10V, I_D = 75A (Note 4)	-	200	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	11190	14885	pF
C_{oss}	Output Capacitance		-	1610	2140	pF
C_{rss}	Reverse Transfer Capacitance		-	750	1125	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 48V, I_D = 75A, V_{GS} = 10V (Note 4, 5)	-	174	226	nC
Q_{gs}	Gate to Source Gate Charge		-	54	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	50	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 30V, I_D = 75A, V_{GS} = 10V, R_{GEN} = 25Ω (Note 4, 5)	-	134	278	ns
t_r	Turn-On Rise Time		-	324	658	ns
$t_{d(off)}$	Turn-Off Delay Time		-	348	706	ns
t_f	Turn-Off Fall Time		-	250	510	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	265	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	1060	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 75A	-	-	1.3	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 75A, dI_F/dt = 100A/μs (Note 4)	-	69	-	ns
Q_{rr}	Reverse Recovery Charge		-	152	-	nC

Notes:
1: Repetitive Rating: Pulse width limited by maximum junction temperature
2: L = 0.9mH, I_{AS} = 75A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3: I_{SD} ≤ 75A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4: Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5: Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

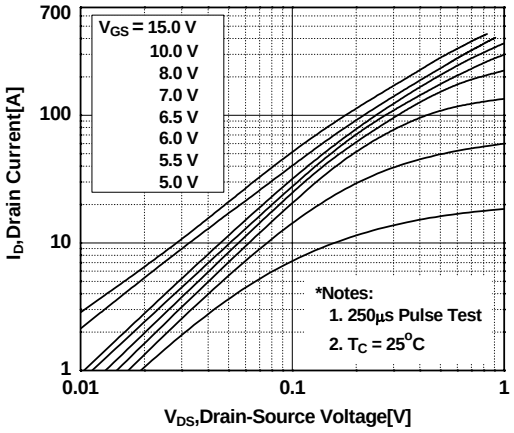


Figure 2. Transfer Characteristics

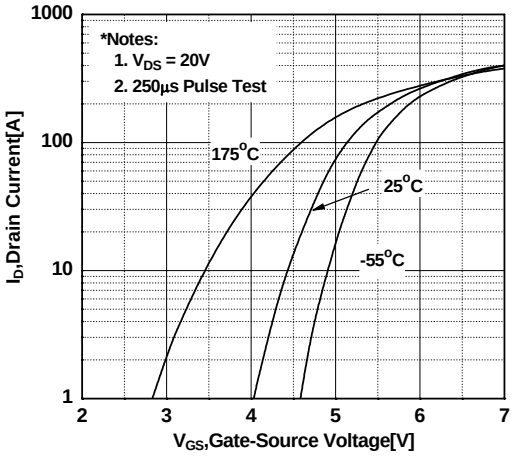


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

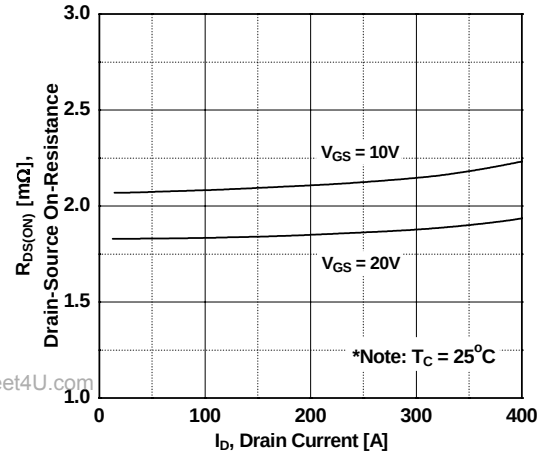


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

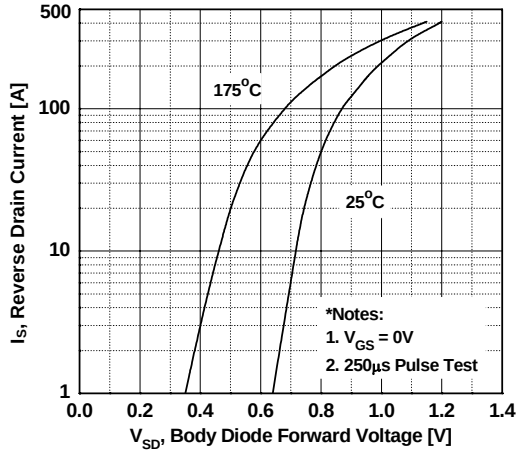


Figure 5. Capacitance Characteristics

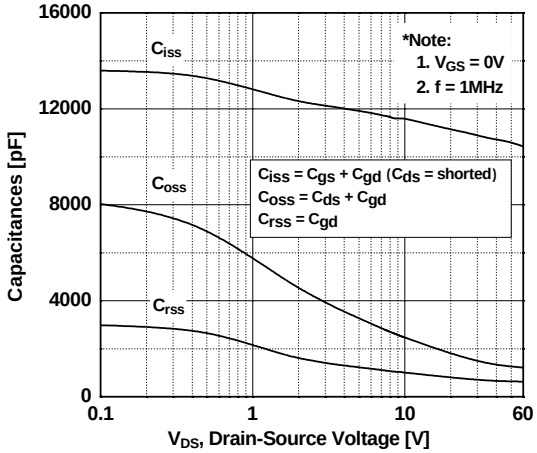
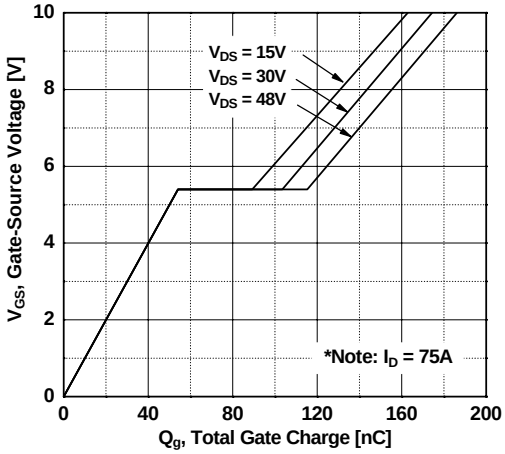


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

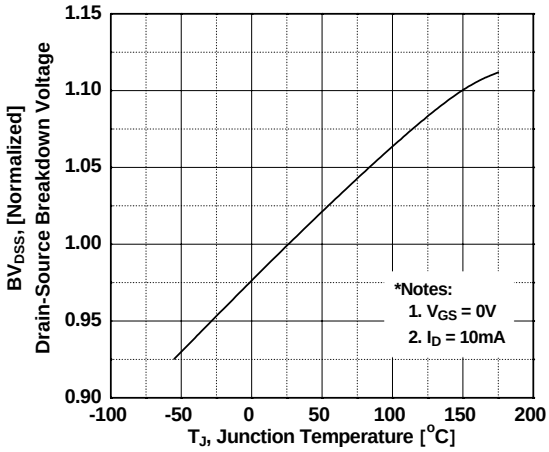


Figure 8. On-Resistance Variation vs. Temperature

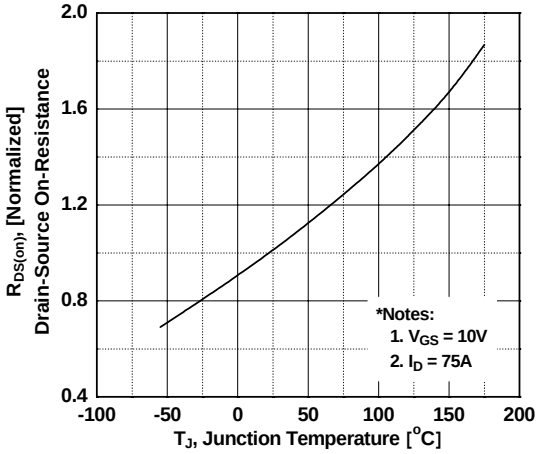


Figure 9. Maximum Safe Operating Area

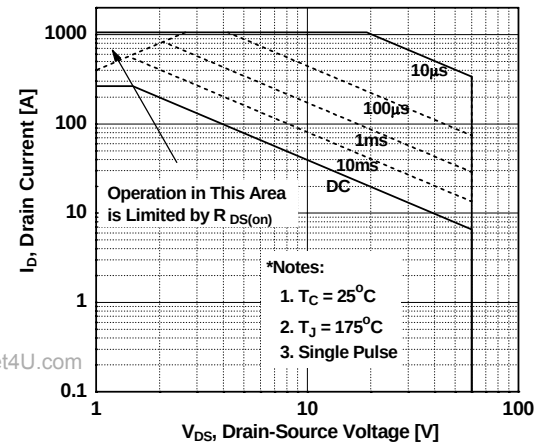


Figure 10. Maximum Drain Current vs. Case Temperature

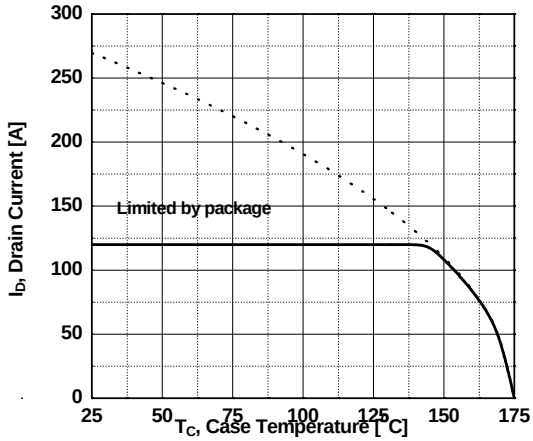
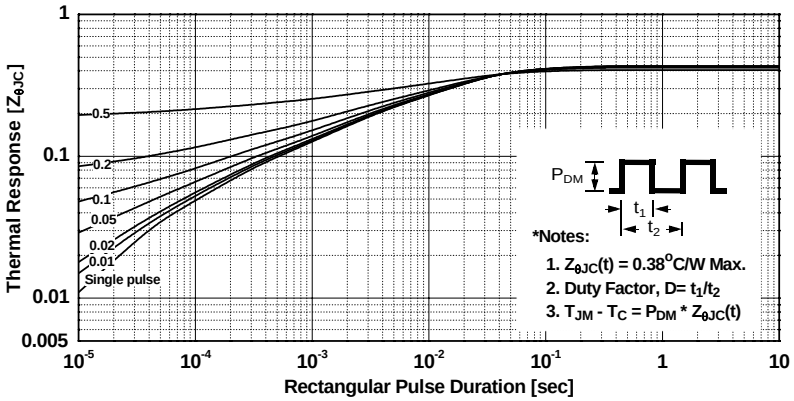
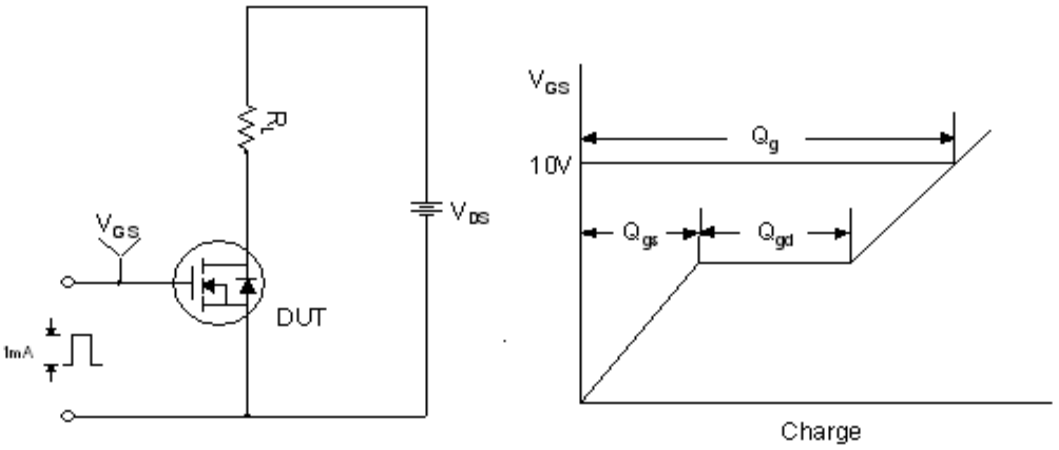


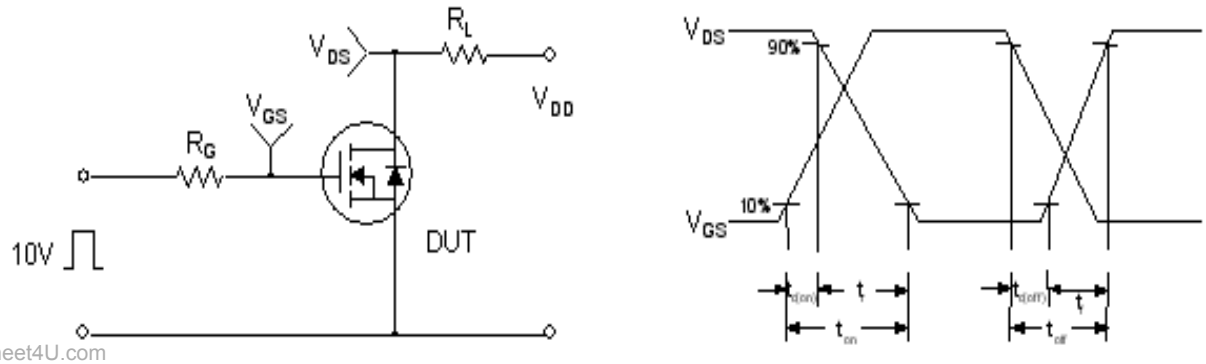
Figure 11. Transient Thermal Response Curve



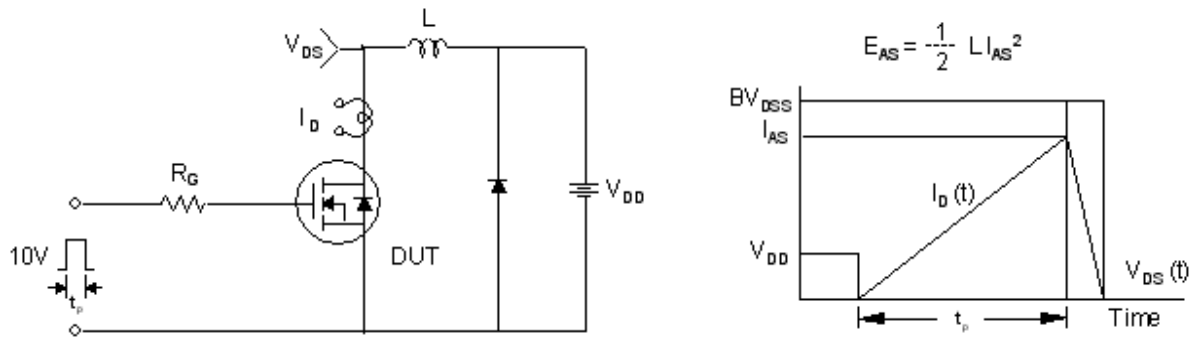
Gate Charge Test Circuit & Waveform



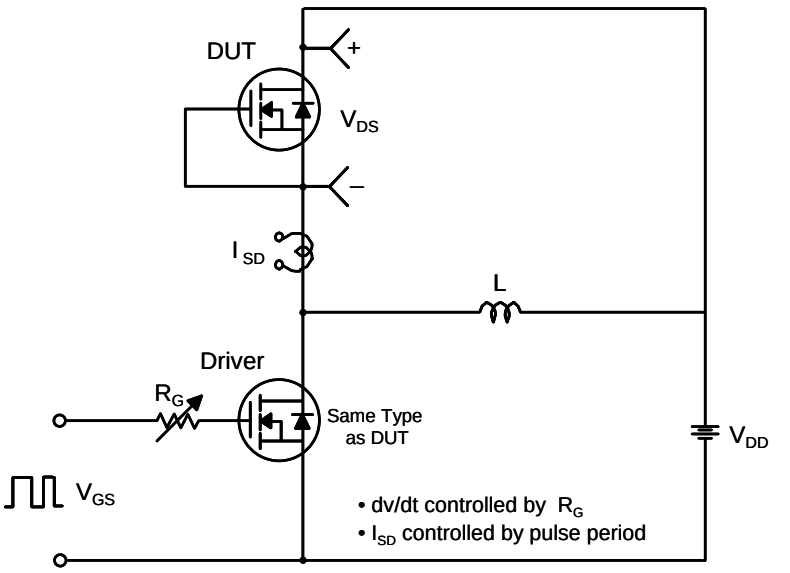
Resistive Switching Test Circuit & Waveforms

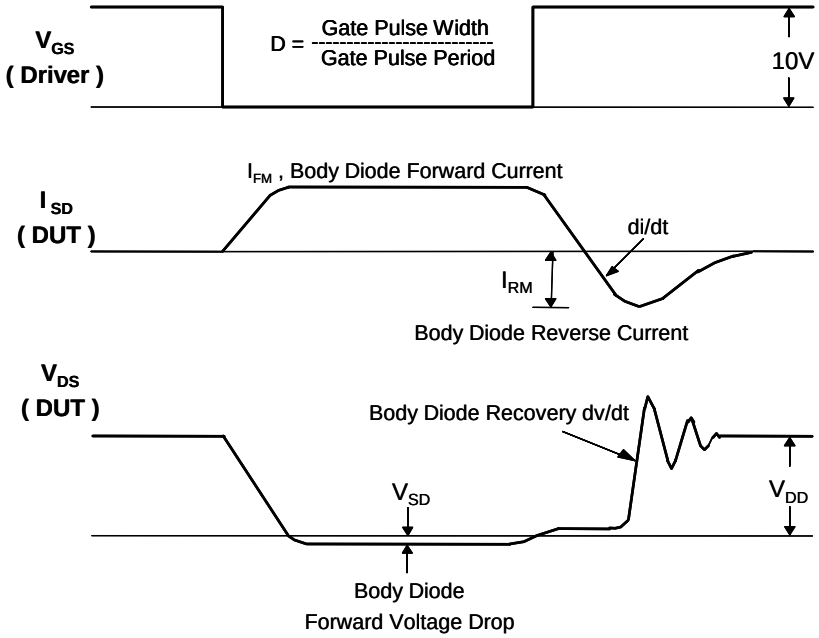


Unclamped Inductive Switching Test Circuit & Waveforms



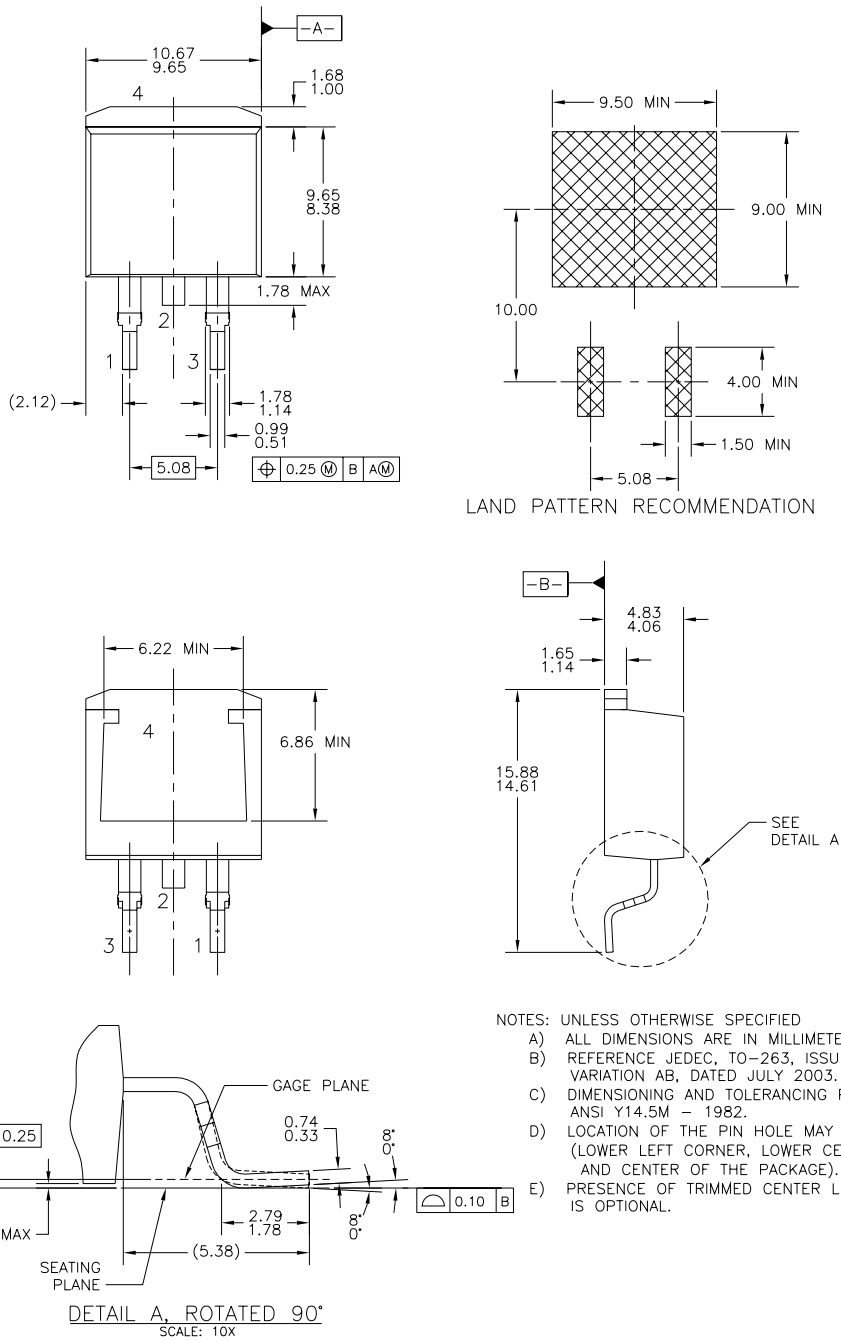
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Mechanical Dimensions

D2-PAK



NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.

B) REFERENCE JEDEC, TO-263, ISSUE D, VARIATION AB, DATED JULY 2003.

C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5M – 1982.

D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).

E) PRESENCE OF TRIMMED CENTER LEAD IS OPTIONAL.

TO263A02REVD

Dimensions in Millimeters

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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