High Performance
128K×8 3.3V
CMOS SRAM

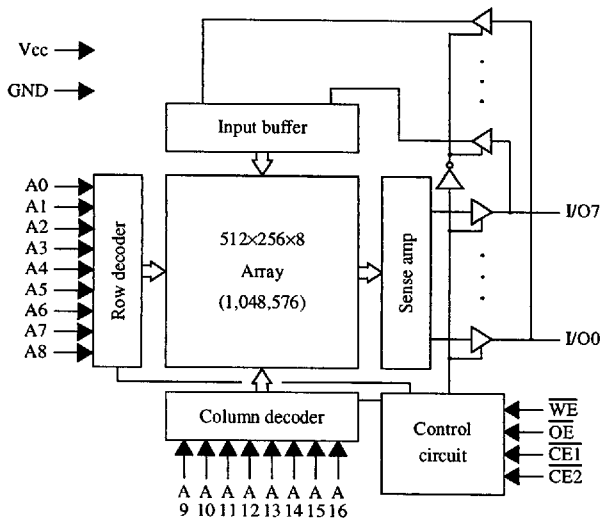
AS7C3102+
AS7C3102+L

Low voltage 128K×8 CMOS SRAM (Common I/O)

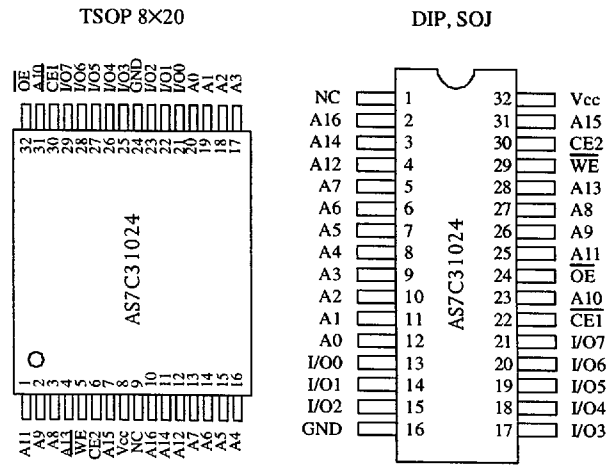
Features

- Organization: 131,072 words × 8 bits
- Single 3.3 ±0.3V power supply
- 5V tolerant I/O specification
- High speed
  - 12/15/20/25/35 ns address access time
  - 3/4/5/6/8 ns output enable access time
- Very low power consumption
- Active:270 mW max, (12 ns cycle)
  - Standby: 18. mW max, CMOS I/O
    3.6 mW max, CMOS I/O, L version
- 2.0V data retention
- Equal access and cycle times
- Easy memory expansion with $\overline{CE1}$, CE2 and $\overline{OE}$ inputs
- TTL-compatible, three-state I/O
- Ideal for cache, modem, portable computing
  - 75% power reduction during CPU idle mode
- 32-pin JEDEC standard packages
  - 300 mil PDIP and SOJ
  - 8 × 20 TSOP
- ESD protection >2000 volts
- Latch-up current >200 mA

Logic block diagram



Pin arrangement



Selection guide

		7C31024-12	7C31024-15	7C31024-20	7C31024-25	7C31024-35	Unit
Maximum address access time		12	15	20	25	35	ns
Maximum output enable access time		3	4	5	6	8	ns
Maximum operating current		75	70	65	60	55	mA
Maximum CMOS standby current		5.0	5.0	5.0	5.0	5.0	mA
	L	1.0	1.0	1.0	1.0	1.0	mA

Shaded areas contain advance information.

Functional description

The AS7C31024 is a 3.3V high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) organized as 131,072 words × 8 bits. It is designed for memory applications requiring fast data access at low voltage, including Pentium™, PowerPC™, and portable computing. Alliance's advanced circuit design and process techniques permit 3.3V operation without sacrificing performance or operating margins.

The device enters standby mode when $\overline{CE1}$ is HIGH or CE2 is LOW. CMOS standby mode consumes ≤18. mW (≤3.6mW for the L version). Normal operation offers 75% power reduction after initial access, resulting in significant power savings during CPU idle, suspend, and stretch mode. Both versions of the AS7C31024 offer 2.0V data retention.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 12/15/20/25/35 ns with output enable access times (t_{OE}) of 3/4/5/6/8 ns are ideal for high performance applications. The active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank memory systems.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) HIGH. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and 5V tolerant. Operation is from a single 3.3±0.3V supply. The AS7C31024 is packaged in all high volume industry standard packages.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{CC}	−0.5	+4.6	V
Input voltage relative to GND	V_{IN}	−0.5	+6.0	V
Power dissipation	P_D	–	1.0	W
Storage temperature (plastic)	T_{stg}	−55	+150	°C
Temperature under bias	T_{bias}	−10	+85	°C
DC output current	I_{out}	–	20	mA

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB}, I_{SB1})
X	L	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	H	High Z	Output disable
L	H	H	L	D_{out}	Read
L	H	L	X	D_{in}	Write

Key: X = Don't Care, L = LOW, H = HIGH

Recommended operating conditions

T_a = 0°C to +70°C

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	3.0	3.3	3.6	V
	GND	0.0	0.0	0.0	V
Input voltage	V_{IH}	2.0	–	5.5	V
	V_{IL}	−0.5†	–	0.8	V

†V_{IL} min = −2.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics[1]

V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C

				-12		-15		-20		-25		-35		
Parameter	Symbol	Test Conditions		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max, V_{in} = GND to V_{CC}		–	1	–	1	–	1	–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{CC} = Max, V_{out} = GND to V_{CC}		–	1	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, f = f_{max}, I_{out} = 0 mA		–	75	–	70	–	65	–	60	–	55	mA
Standby power supply current	I_{SB}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, f = f_{max}		–	35	–	30	–	25	–	25	–	20	mA
	I_{SB1}	$\overline{CE1}$ ≥ V_{CC}−0.2V or CE2 ≤ 0.2V, V_{in} ≤ 0.2V or V_{in} ≥ V_{CC}−0.2V, f = 0		–	5.0	–	5.0	–	5.0	–	5.0	–	5.0	mA
			L	–	1.0	–	1.0	–	1.0	–	1.0	–	1.0	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = −4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	2.4	–	V

Capacitance[2]

f = 1 MHz, T_a = Room temperature, V_{CC} = 3.3V

Parameter	Symbol	Signals	Test Conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{in} = V_{out} = 0V	7	pF

Read cycle[3,9,12]

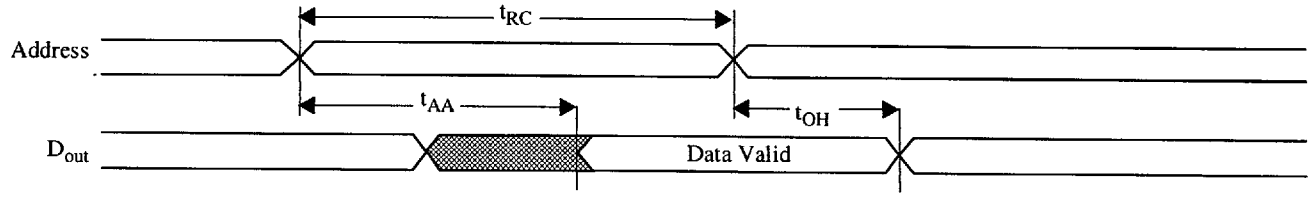
(V_{CC} = 3.3±0.3V, GND = 0V, T_a = 0°C to +70°C)

		-12		-15		-20		-25		-35			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Read cycle time	t_{RC}	12	–	15	–	20	–	25	–	35	–	ns	
Address access time	t_{AA}	–	12	–	15	–	20	–	25	–	35	ns	3
Chip enable ($\overline{CE1}$) access time	t_{ACE1}	–	12	–	15	–	20	–	25	–	35	ns	3, 12
Chip enable (CE2) access time	t_{ACE2}	–	12	–	15	–	20	–	25	–	35	ns	3, 12
Output enable ($\overline{OE}$) access time	t_{OE}	–	3	–	4	–	5	–	6	–	8	ns	
Output Hold from address change	t_{OH}	3	–	3	–	3	–	3	–	3	–	ns	5
$\overline{CE1}$ LOW to output in Low Z	t_{CLZ1}	3	–	3	–	3	–	3	–	3	–	ns	4, 5, 12
CE2 HIGH to output in Low Z	t_{CLZ2}	3	–	3	–	3	–	3	–	3	–	ns	4, 5, 12
$\overline{CE1}$ HIGH to output in High Z	t_{CHZ1}	–	3	–	4	–	5	–	6	–	8	ns	4, 5, 12
CE2 LOW to output in High Z	t_{CHZ2}	–	3	–	4	–	5	–	6	–	8	ns	4, 5, 12
$\overline{OE}$ LOW to output in Low Z	t_{OLZ}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ HIGH to output in High Z	t_{OHZ}	–	3	–	4	–	5	–	6	–	8	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	0	–	ns	4, 5, 12
Power down time	t_{PD}	–	12	–	15	–	20	–	25	–	35	ns	4, 5, 12

Shaded areas contain advance information.

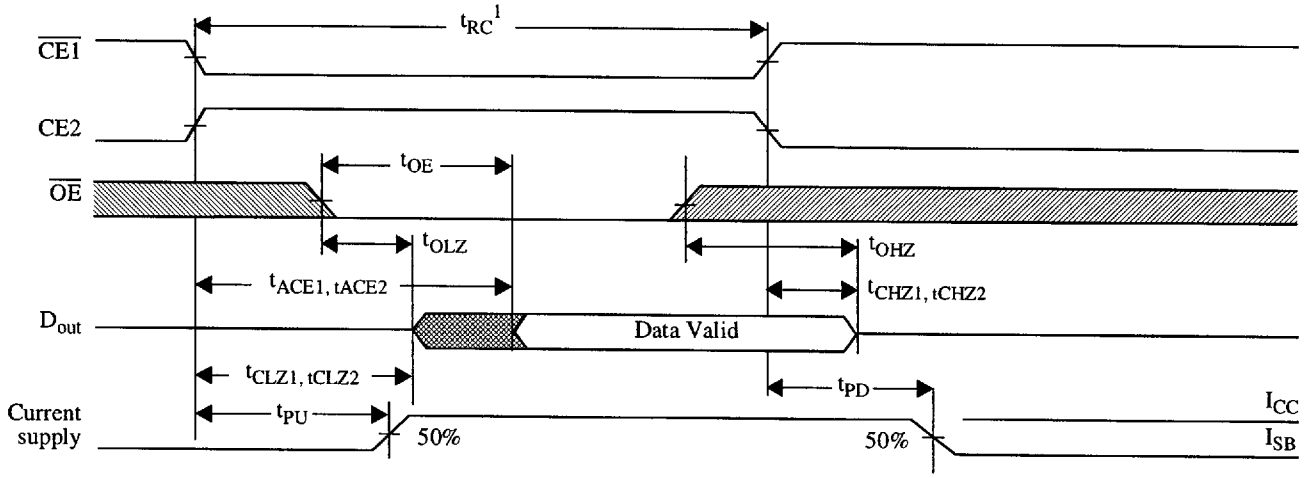
Read waveform 1[3,6,7,9,12]

Address controlled



Read waveform 2[3,6,8,9,12]

$\overline{CE1}$ and CE2 controlled



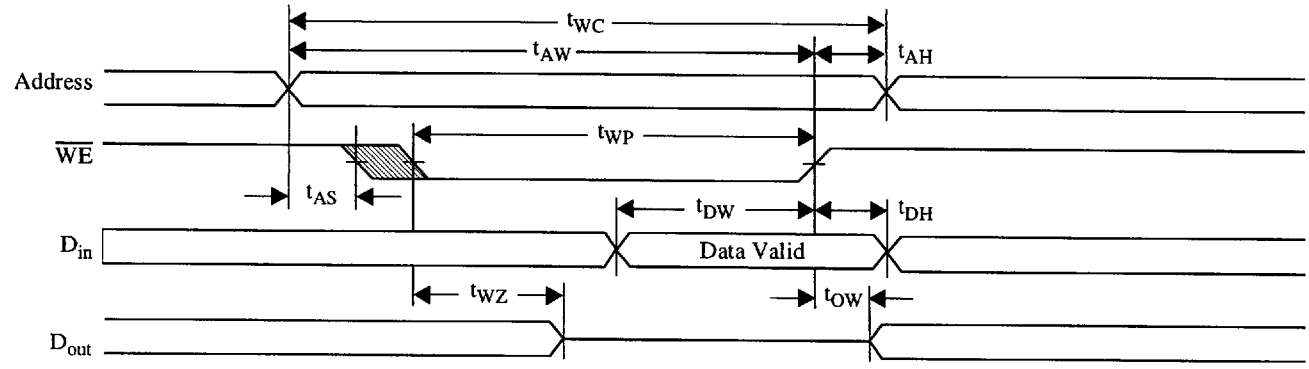
Write cycle[11,12]

(V_{CC} = 3.3±0.3V, GND = 0V, Ta = 0°C to +70°C)

		-12		-15		-20		-25		-35			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Write cycle Time	t_{WC}	12	–	15	–	20	–	20	–	30	–	ns	
Chip enable ($\overline{CE1}$) to write end	t_{CW1}	10	–	12	–	12	–	15	–	20	–	ns	12
Chip enable (CE2) to write end	t_{CW2}	10	–	12	–	12	–	15	–	20	–	ns	12
Address setup to write end	t_{AW}	10	–	12	–	12	–	15	–	20	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	0	–	ns	12
Write pulse width	t_{WP}	8	–	9	–	12	–	15	–	17	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	6	–	8	–	10	–	12	–	15	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in High Z	t_{WZ}	–	5	–	5	–	5	–	5	–	5	ns	4, 5
Output active from write end	t_{OW}	3	–	3	–	3	–	3	–	3	–	ns	4, 5

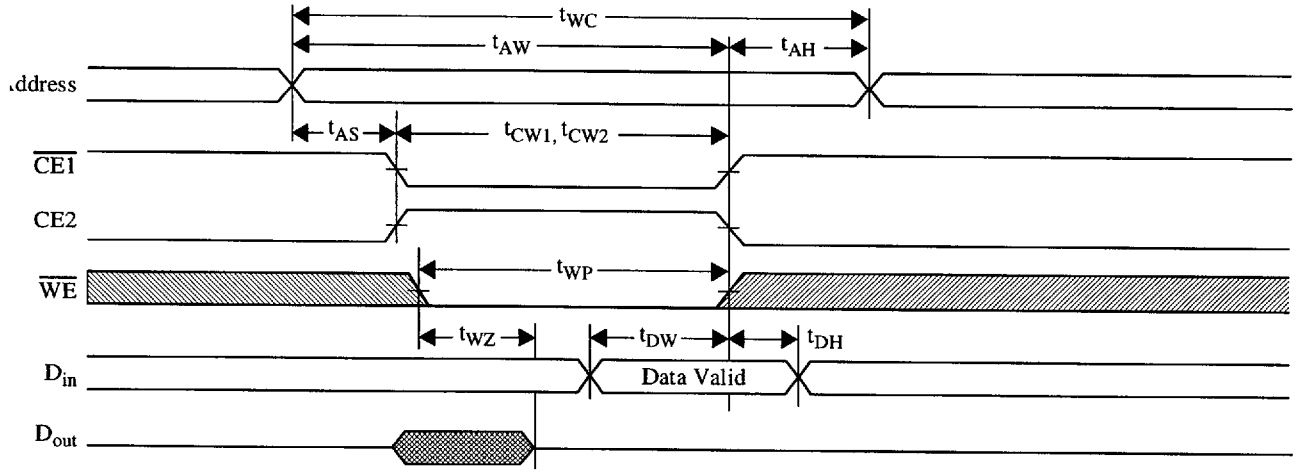
Write waveform 1[10,11,12]

$\overline{WE}$ controlled



Write waveform 2[10,11,12]

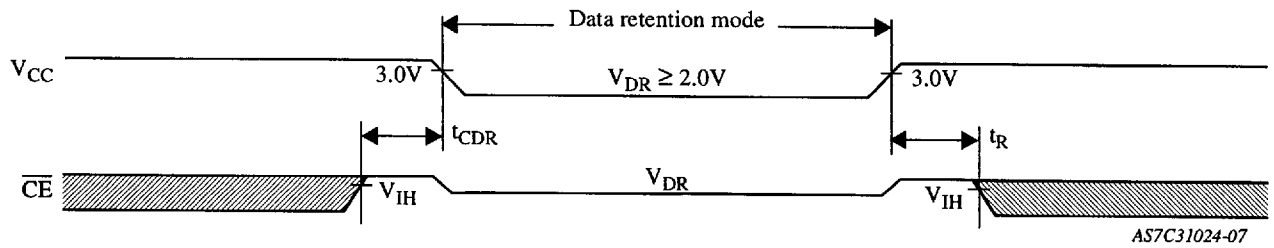
$\overline{CE1}$ and CE2 controlled



Data retention characteristics

Parameter	Symbol	Test Conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V	2.0	–	V
Data retention current	I_{CCDR}	$\overline{CE1} \geq V_{CC}-0.2V$ or CE2 ≤ 0.2V	–	2500	µA
			–	500	µA
Chip enable to data retention time	t_{CDR}	$V_{in} \geq V_{CC}-0.2V$ or $V_{in} \leq 0.2V$	0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B, except for t_{CLZ} and t_{CHZ} see Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 5 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

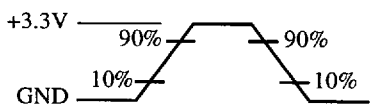


Figure A: Input waveform

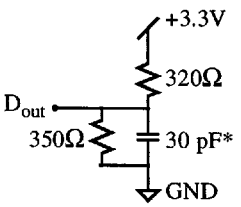


Figure B: Output load

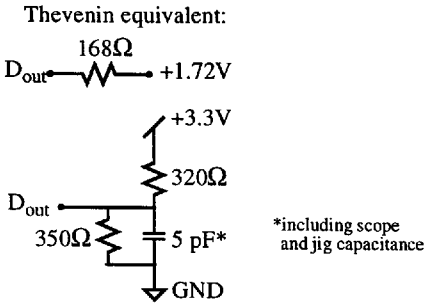


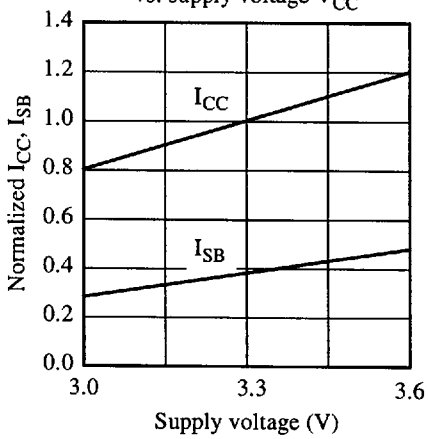
Figure C: Output load for t_{CLZ}, t_{CHZ}

Notes

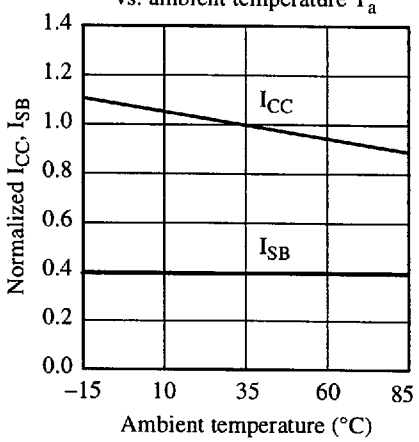
1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed but not tested.
6 $\overline{WE}$ is HIGH for read cycle.
7 $\overline{CE1}$ and $\overline{OE}$ are LOW and CE2 is HIGH for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition LOW.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE1}$ or $\overline{WE}$ must be HIGH or CE2 LOW during address transitions.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 $\overline{CE1}$ and CE2 have identical timing.

Typical DC and AC characteristics

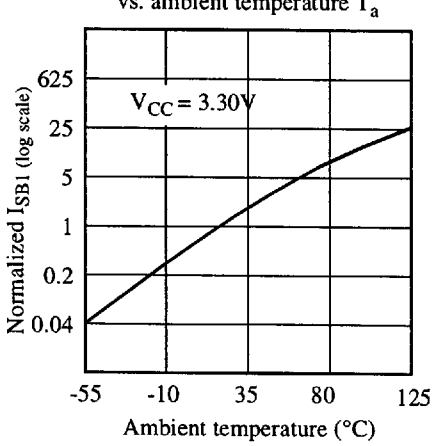
Normalized supply current I_{CC}, I_{SB} vs. supply voltage V_{CC}



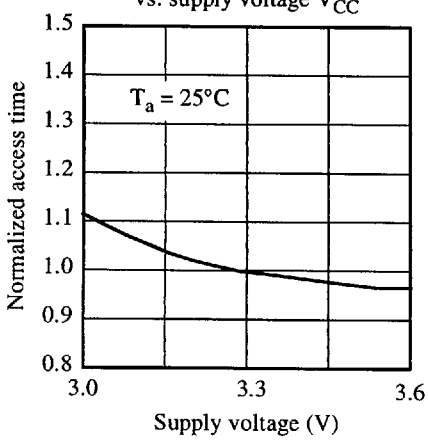
Normalized supply current I_{CC}, I_{SB} vs. ambient temperature T_a



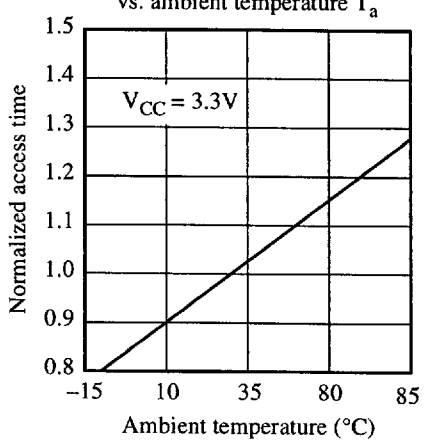
Normalized supply current I_{SB1} vs. ambient temperature T_a



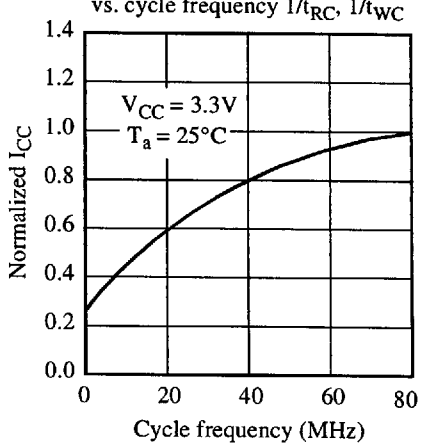
Normalized access time t_{AA} vs. supply voltage V_{CC}



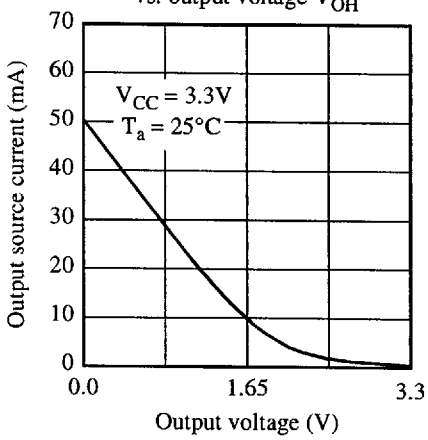
Normalized access time t_{AA} vs. ambient temperature T_a



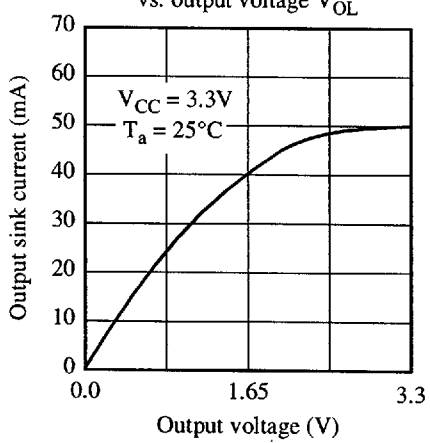
Normalized supply current I_{CC} vs. cycle frequency $1/t_{RC}$, $1/t_{WC}$



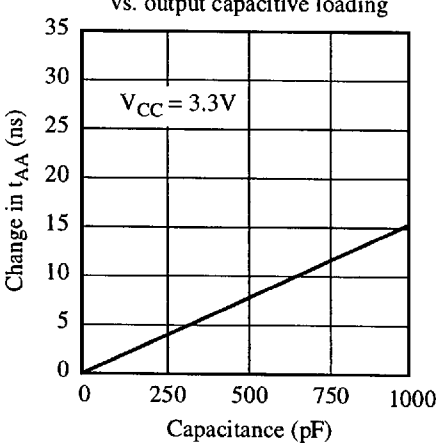
Output source current I_{OH} vs. output voltage V_{OH}



Output sink current I_{OL} vs. output voltage V_{OL}



Typical access time change Δt_{AA} vs. output capacitive loading



Ordering information

Package \ Access Time	12 ns	15 ns	20 ns	25 ns	35 ns
Plastic DIP, 300 mil	AS7C31024-12PC	AS7C31024-15PC	AS7C31024-20PC	AS7C31024-25PC	AS7C31024-35PC
	AS7C31024L-12PC	AS7C31024L-15PC	AS7C31024L-20PC	AS7C31024L-25PC	AS7C31024L-35PC
Plastic SOJ, 300 mil	AS7C31024-12JC	AS7C31024-15JC	AS7C31024-20JC	AS7C31024-25JC	AS7C31024-35JC
	AS7C31024L-12JC	AS7C31024L-15JC	AS7C31024L-20JC	AS7C31024L-25JC	AS7C31024L-35JC
TSOP 8x20	AS7C31024-12TC	AS7C31024-15TC	AS7C31024-20TC	AS7C31024-25TC	AS7C31024-35TC
	AS7C31024L-12TC	AS7C31024L-15TC	AS7C31024L-20TC	AS7C31024L-25TC	AS7C31024L-35TC

Part numbering system

AS7C	3	1024	–XX	X	C
SRAM prefix	Blank = 5V supply 3 = 3.3V supply	Device number	Access time	Package: P = PDIP 300 mil J = SOJ 300 mil T = TSOP 8x20	Commercial tmperature range, 0°C to 70°C

Representatives, distributors, and sales offices

DOMESTIC REPS

ALABAMA
Concord Component
(205) 772-8883

ARIZONA
Southern States Marketing
(214) 238-7500

CALIFORNIA
North
Brooks Technical
(415) 960-3880
LA Area
Competitive Tech.
(714) 450-0170
San Diego
ATS
(619) 634-1488

COLORADO
Technology Sales
(303) 692-8835

CONNECTICUT
Kitchen & Kutchin
(203) 239-0212

DELAWARE
Electro Tech
(610) 272-2125

FLORIDA
Micro-Electronic Comp.
Deerfield Beach
(954) 426-8944
Orlando
(407) 682-9602
Tampa
(813) 393-5011

GEORGIA
Concord Component
(770) 416-9597

HAWAII
Brooks Technical
(415) 960-3880

IDAHO
ES/Chase
(503) 684-8500

ILLINOIS
North
El-Mech
(312) 794-9100
South
CenTech
(314) 291-4230

INDIANA
CC Electro Sales
(317) 921-5000

KANSAS
CenTech
(816) 358-8100

KENTUCKY
CC Electro Sales
(317) 921-5000

LOUISIANA
Southern States Marketing
North
(214) 238-7500
South
(713) 895-8533

MAINE
Kitchen & Kutchin
(617) 229-2660

MARYLAND
Chesapeake Tech.
(301) 236-0530

MASSACHUSETTS
Kitchen & Kutchin
(617) 229-2660

MICHIGAN
Enco Group
(810) 338-8600

MINNESOTA
D. A. Case Associates
(612) 831-6777

MISSOURI
CenTech
East
(314) 291-4230
West
(816) 358-8100

MISSISSIPPI
Concord Component
(205) 772-8883

MONTANA
ES/Chase
(503) 684-8500

NEBRASKA
CenTech
(816) 358-8100

NEVADA
Brooks Technical
(415) 960-3880

NEW HAMPSHIRE
Kitchen & Kutchin
(617) 229-2660

NEW JERSEY
North
ERA Associates
(800) 645-5500
South
Electro Tech
(610) 272-2125

NEW YORK
NYC
ERA Associates
(516) 543-0510
Upstate
Tri-Tech
Rochester
(716) 385-6500
Binghamton
(607) 722-3580

NORTH CAROLINA
Concord Component
(919) 846-3441

NORTH DAKOTA
D. A. Case Associates
(612) 831-6777

OHIO
Midwest Marketing Assoc.
Lyndhurst
(216) 381-8575
Dayton
(513) 433-2511

OKLAHOMA
Southern States Marketing
(214) 238-7500

OREGON
ES/Chase
(503) 684-8500

PENNSYLVANIA
East
Electro Tech
(610) 272-2125
West
Midwest Marketing
(216) 381-8575

RHODE ISLAND
Kitchen & Kutchin
(617) 229-2660

SOUTH CAROLINA
Concord Component
(919) 846-3441

SOUTH DAKOTA
D. A. Case Associates
(612) 831-6777

TENNESSEE
Concord Component
(205) 772-8883

TEXAS
Southern States Marketing
Austin
(512) 835-5822
Dallas
(214) 238-7500
Houston
(713) 895-8533

UTAH
Charles Fields & Assoc.
(801) 299-8228

VERMONT
Kitchen & Kutchin
(617) 229-2660

VIRGINIA
Chesapeake Tech.
(301) 236-0530

WASHINGTON
ES/Chase
(206) 823-9535

WEST VIRGINIA
Chesapeake Tech.
(301) 236-0530

WISCONSIN
D. A. Case Associates
(612) 831-6777

WYOMING
Technology Sales
(303)692-8835

INTERNATIONAL REPS

AUSTRALIA
Dingley
R&D Electronics
+61-3-9558-0444
Bayswater
ACD
+61-3-9762-7644

CANADA
J Squared Technologies
Ottawa
(613) 592-9540
Toronto
(905) 672-2030
Montreal
(514) 747-1211
Vancouver
(604) 473-4666
Calgary
(403) 291-6755

EUROPE
Britcomp Sales
Surrey, England
+44-1932 347077
+44-1932 346256
Munich, Germany
+49-894488496
Athismons, France
+33-1-69387678

interACTIVE
Great Britain, Ireland
+44-1773-740263

Ramtec Int'l B.V.
Holland, Spain, Italy, Belgium, Hungary, Russia
+31-2526-21222

HONG KONG
Eastele Technology
+852-2798-8860

INDIA
Priya Electronics, Inc.
San Jose, CA USA
(408) 954-1866

Satcom Sales & Srvcs.
+91-40-761-4675

ISRAEL
Eldis Technology
+972-9-562-666

JAPAN
Tokyo
Bussan Micro Electronics
+81-3-5421-1730
Kyoto
Rohm Co. Ltd.
+81-75-311-2121

KOREA
FM Korea
+822-596-3880
fm@ktnet.co.kr

Woo Young Tech
+822-369-7099

MALAYSIA
Exer Technologies
+60-4-657-9592

PUERTO RICO
Micro-Electronic Comp.
(787) 746-9897

SINGAPORE
Exer Technologies
+65-749-1349

TAIWAN
Asian Specific Tech.
+886-2-521-2363

Golden Way Electronics
+886-2-698-1868 x505

Puteam International
+886-2-729-0373

DISTRIBUTORS

All American
HQ: (305) 621-8282

Axis: Components, Inc.
HQ: (800) 556-0225

Future Electronics
HQ: (514) 594-7710

Interface Electronics
HQ: (800) 632-7792

Please contact your rep to locate a distributor near you

SALES OFFICES

HEADQUARTERS
Alliance Semiconductor
San Jose, CA
(408) 383-4900

NORTHEAST AREA
Alliance Semiconductor
Boston, MA
(617) 239-8127

TECHNICAL CENTER

TAIWAN
Alliance Semiconductor

ALLIANCE SEMICONDUCTOR
3099 North First Street San Jose, CA 95134 Tel (408) 383-4900 Fax (408) 383-4999 www.alsc.com

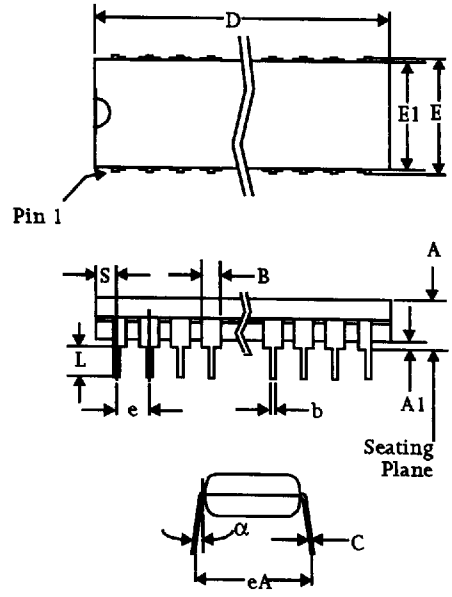
June 1996

Package diagrams

Plastic dual in-line package (PDIP)

	20-pin 300 mil		28-pin 300 mil		32-pin 300 mil		32-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.175	-	0.175	-	0.180	-	0.200
A1	0.010	-	0.010	-	0.015	-	0.015	-
B	0.046	0.054	0.058	0.064	0.045	0.055	0.045	0.065
b	0.018	0.024	0.016	0.022	0.015	0.021	0.014	0.022
C	0.008	0.014	0.008	0.014	0.008	0.012	0.009	0.015
D	-	0.980	-	1.400	-	1.571	-	1.620
E	0.290	0.310	0.295	0.320	0.300	0.325	0.390	0.425
E1	0.263	0.293	0.278	0.298	0.280	0.295	0.340	0.390
e	0.100 BSC		0.100 BSC		0.100 BSC		0.100 BSC	
eA	0.310	0.350	0.330	0.370	0.330	0.370	0.430	0.470
L	0.110	0.130	0.120	0.140	0.110	0.142	0.118	0.162
α	0°	15°	0°	15°	0°	15°	0°	15°
S	-	0.040	-	0.055	-	0.043	-	0.065

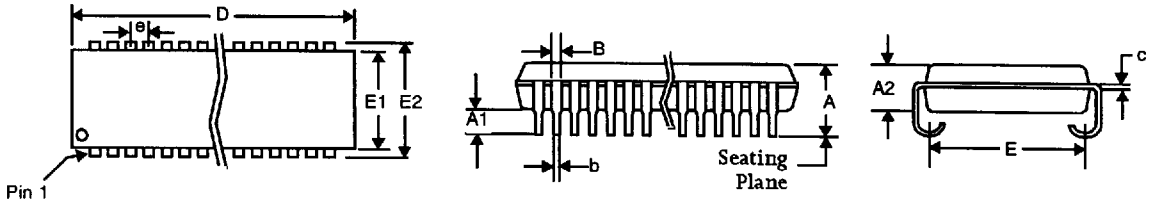
Dimensions in inches



Plastic small outline J-bend (SOJ)

	20/26-pin 300 mil		28-pin 300 mil		32-pin 300 mil		28-pin 400 mil		32-pin 400 mil		36-pin 400 mil		40-pin 400 mil		42-pin 400 mil		44-pin 400 mil	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
A	-	0.140	-	0.140	-	0.145	0.132	0.146	-	0.145	-	-	-	0.145	0.128	0.148	0.128	0.148
A1	0.020	-	0.025	-	0.025	-	0.062	-	0.025	-	-	-	0.025	-	0.025	-	0.025	-
A2	0.095	0.105	0.095	0.105	0.086	0.105	0.105	115	0.086	0.115	0.102 NOM		0.086	0.115	1.105	1.115	1.105	1.115
B	0.025	0.032	0.028 TYP		0.026	0.032	0.024	0.032	0.026	0.032	-	0.032	0.026	0.032	0.026	0.032	0.026	0.032
b	0.016	0.022	0.018 TYP		0.014	0.020	0.013	0.021	0.015	0.020	0.013	0.021	0.015	0.022	0.015	0.020	0.015	0.020
c	0.008	0.014	0.010 TYP		0.006	0.013	0.005	0.012	0.007	0.013	-	-	0.007	0.014	0.007	0.013	0.007	0.013
D	-	0.686	-	0.730	0.820	0.830	0.720	0.729	0.820	0.830	0.920	0.930	1.015	1.035	1.070	1.080	1.120	1.130
E	0.327	0.347	0.327	0.347	0.330	0.340	0.430	0.440	0.435	0.445	0.350	0.390	0.435	0.445	0.370 NOM		0.370 NOM	
E1	0.295	0.305	0.295	0.305	0.292	0.305	0.395	0.405	0.395	0.405	0.400 NOM		0.395	0.405	0.395	0.405	0.395	0.405
E2	0.245	0.285	0.245	0.285	0.250	0.275	0.354	0.378	0.360	0.380	0.435	0.445	0.348	0.390	0.435	0.445	0.435	0.445
e	0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.050 BSC		0.045	0.055	0.050 BSC		0.050 NOM		0.050 NOM	

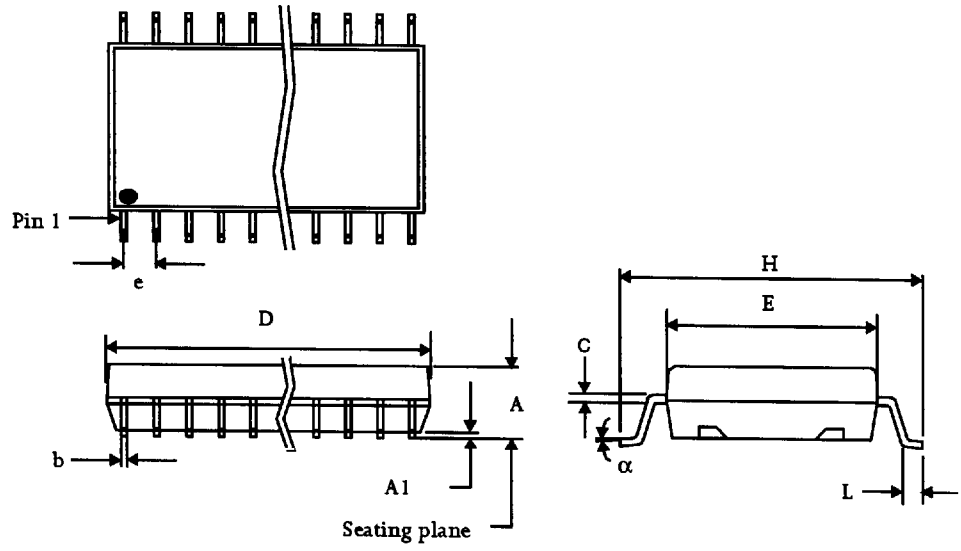
Dimensions in inches



Plastic small outline gull wing IC (SOIC)

	28-pin 330 mil	
	Min	Max
A	-	0.112
A1	0.004	-
b	0.014	0.020
C	0.008	0.014
D	-	0.733
e	0.050 nominal	
E	0.326	0.336
H	0.453	0.477
L	0.028	0.044
α	0°	10°

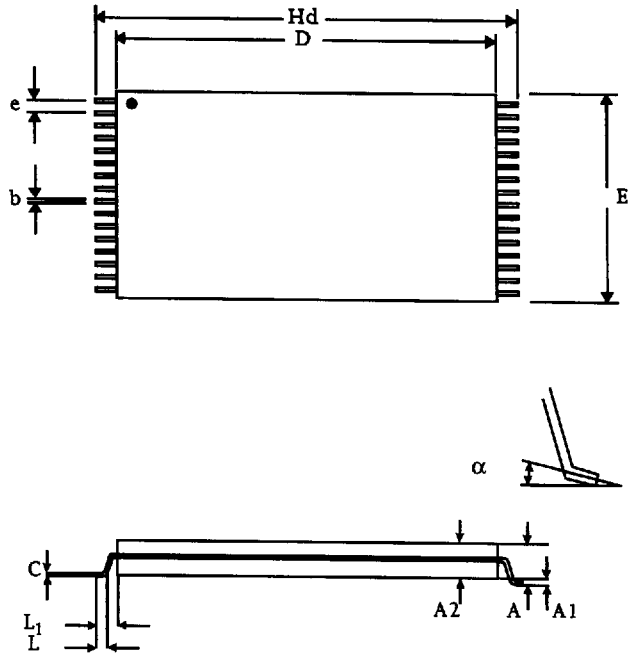
Dimensions in inches

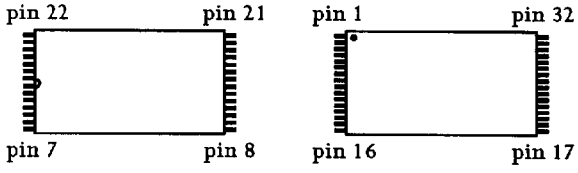


Thin small outline package (TSOP-I)

	28-pin 8×13.4		32-pin 8×20		40-pin 10×20	
	Min	Max	Min	Max	Min	Max
A	-	1.20	-	1.20	-	1.20
A1	0.05	0.15	0.05	0.15	0.05	0.15
A2	0.90	1.05	0.90	1.05	0.95	1.05
b	0.17	0.27	0.17	0.23	0.17	0.27
C	0.10	-	0.10	-	0.10	0.20
D	11.70	11.90	18.20	18.60	18.30	18.50
e	0.55 nominal		0.50 nominal		0.50 nominal	
E	8.0 nominal		7.80	8.20	9.90	10.10
Hd	13.20	13.60	19.80	20.20	19.80	20.20
L	0.30	0.70	0.40	0.60	0.50	0.70
α	0°	5°	1°	5°	0°	5°

Dimensions in millimeters





28-pin 32-pin