

Charge Pump Super DC-to-DC Voltage Converter

FEATURES

- Oscillator Boost from 10kHz to 45kHz
- Converts +5V Logic Supply to $\pm 5V$ System
- Wide Input Voltage Range 1.5V to 12V
- Efficient Voltage Conversion 99.9%
- Excellent Power Efficiency 98%
- Low Power Supply 80 μ A @ 5 V_{IN}
- Low Cost and Easy to Use
- Only Two External Capacitors Required
- Available in Small Outline (SO) Package
- Similar to Industry Standard LTC1044/7660S
- Improved ESD Protection Up to 10kV
- No External Diode Required for High Voltage Operation

APPLICATIONS

- Conversion of 5V to $\pm 5V$ Supplies
- Precise Voltage Division: $V_{OUT} = \pm V_{IN}/2 \pm 20\text{ppm}$
- Voltage Multiplication: $V_{OUT} = \pm nV_{IN}$
- Supply Splitter: $V_{OUT} = \pm V_S/2$
- Automotive Applications
- Battery Systems with 9V Wall Adapters/Chargers

PRODUCT DESCRIPTION

The ALPHA Semiconductor AS1044S DC-to-DC voltage converter is the improved Super Voltage Converter version of LTC1044. Added features include extended operating supply voltage range up to 12V, and frequency boost pin for higher operating frequency to lower output impedance with smaller capacitors. The AS1044S can generate a negative voltage from a positive source. With two external capacitors, the AS1044S will convert a 1.5V to 12V input signal to a -1.5V to -12V level. The AS1044S easily generates -5V in +5V digital systems. Many A/D converters, D/A converters, operational amplifiers, and multiplexers require negative supply voltages. The AS1044S allows +5V digital logic systems to incorporate these analog components without adding an additional main power source.

The AS1044S charges a capacitor to the applied supply voltage. Internal analog switches connect the capacitor across the output. Charge is transferred to an output storage capacitor completing the voltage conversion. Operation requires only two external capacitors for full supply voltage range.

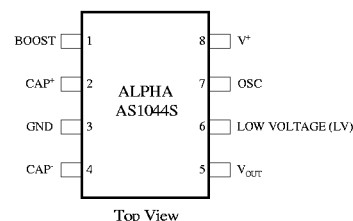
The oscillator can be boosted from 10kHz to 45kHz. If operation below 10kHz is desired, a capacitor may be added to OSC pin 7 with boost pin 1 open. The oscillator may also be overdriven by an external clock. The low voltage (LV) terminal (pin 6) may be tied to GND (pin 3) to bypass the internal series regulator and improve low voltage (LV) operation. At medium-to-high voltages (+3.5V to +12V), the LV pin is left floating to prevent device latch-up.

The AS1044S open-circuit output voltage is equal to the input voltage to within 0.1%. The AS1044S has a 98% power conversion efficiency for 2mA to 5mA load currents. Designed to be pin-for-pin and functionally compatible with the popular AS7660 and LTC1044, the AS1044S provides significant features and improvements over earlier 7660 designs.

ORDERING INFORMATION

Part Number	Temperature Range	Package Type
AS1044SCP	0°C to +70°C	8-Pin Plastic DIP
AS1044SIP	-40°C to +85°C	8-Pin Cer DIP
AS1044SCS	0°C to 70°C	8 Pin SO
AS1044SIS	-40°C to 85°C	8-Pin SO

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+13V
LV, Boost, OSC Inputs	
Voltage (Note 1)	-0.3V to ($V^+ + 0.3V$)
for $V^+ < 5.5V$	
($V^+ - 5.5V$) to ($V^+ + 0.3V$)	
for $V^+ > 5.5V$	
Current into LV (Note 1)	20 μA for $V^+ > 3.5V$
Output Short Duration ($V_{SUPPLY} \leq 5.5V$)	Continuous

Power Dissipation (Note 2)

CER DIP	500mW
Plastic DIP	375mW

Operating Temperature Range

C Suffix	0°C to +70°C
I Suffix	-25°C to +85°C
E Suffix	-40°C to +85°C
M Suffix	-55°C to +125°C

Storage Temperature Range..... -65°C to +150°C

Lead Temperature (Soldering, 10 sec.)+300°C

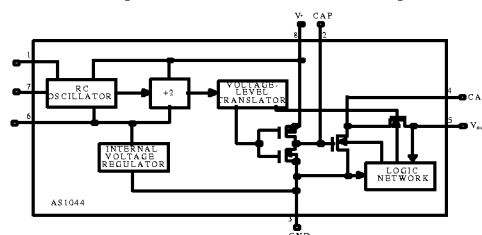
Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS Specifications Measured Over Operating Temperature Range With $V^+ = 5V$, $C_{OSC} = 0$, Test Circuit (Figure 1), unless otherwise specified.

Parameter	Conditions	AS1044S			Units
		Min	Typ	Max	
Supply Current (Boost pin OPEN or GND)	$R_L = \infty$, 25°C 0°C $\leq T_A \leq$ +70°C -40°C $\leq T_A \leq$ +85°C -55°C $\leq T_A \leq$ +125°C		80	160 180 180 200	μA
Supply Current (Boost pin = V^+)	0°C $\leq T_A \leq$ 70°C -40°C $\leq T_A \leq$ +85°C -55°C $\leq T_A \leq$ +125°C			300 350 400	μA
Supply Voltage Range, High	Min $\leq T_A \leq$ Max $R_L = 10k\Omega$, LV Open	3		12	V
Supply Voltage Range, Low	Min $\leq T_A \leq$ Max $R_L = 10k\Omega$, LV to GND	1.5		3.5	V
Output Source Resistance	$I_{OUT} = 20mA$, $T_A = 25^\circ C$		60	100	Ω
	$I_{OUT} = 20mA$, 0°C $\leq T_A \leq$ +70°C.		70	120	Ω
	$I_{OUT} = 20mA$, -40°C $\leq T_A \leq$ +85°C.		70	120	Ω
	$I_{OUT} = 20mA$, -55°C $\leq T_A \leq$ +125°C		105	150	Ω
	$V^+ = 2V$, $I_{OUT} = 3mA$, LV to GND 0°C $\leq T_A \leq$ +70°C -55°C $\leq T_A \leq$ +125°C			250 400	Ω Ω
Oscillator Frequency	Pin 7 open; Pin 1 open or GND		10		kHz
	Pin 1 = V^+		45		kHz
Power Efficiency	$R_L = 5k\Omega$	96	98		%
	$T_{MIN} \leq T_A \leq T_{MAX}$	95	98		%
Voltage Conversion Efficiency	$R_L = \infty$	99	99.9		%
Oscillator Impedance	$V^+ = 2V$		1		M Ω
	$V^+ = 5V$		100		k Ω

NOTES:

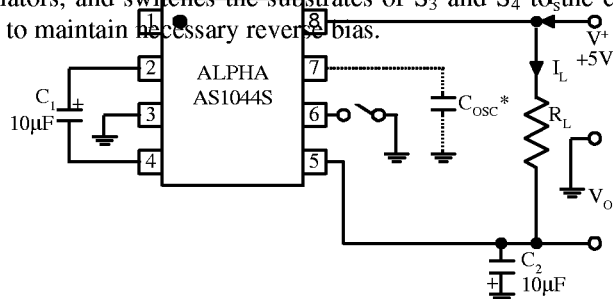
1. Connecting any input terminal to voltages greater than V^+ or less than GND may cause destructive latch-up. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of the AS1044S.
2. Derate linearly above 50°C by 5.5mW/°C



CIRCUIT DESCRIPTION

The AS1044S contains all the necessary circuitry to complete a voltage doubler, with the exception of two external capacitors, which may be inexpensive 10 μF polarized electrolytic capacitors. Operation is best understood by considering Figure 2, which shows an idealized voltage doubler. Capacitor C_1 is charged to a voltage, V^+ , for the half cycle when switches S_1 and S_3 are closed. (Note: Switches S_2 and S_4 are open during this half cycle.) During the second half cycle of operation, switches S_2 and S_4 are closed, with S_1 and S_3 open, thereby shifting capacitor C_1 negatively by V^+ volts. Charge is then transferred from C_1 to C_2 , such that the voltage on C_2 is exactly V^+ , assuming ideal switches and no load on C_2 .

The four switches in Figure 2 are MOS power switches, S_1 is a P-channel device, and S_2 , S_3 and S_4 are N-channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of S_3 and S_4 must always remain reverse-biased with respect to their sources, but not so much as to degrade their ON resistance's. In addition, at circuit start-up, and under output short circuit conditions ($V_{\text{OUT}} = V^+$), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this will result in high power losses and probable device latch-up. This problem is eliminated in the AS1044S by a logic network which senses the output voltage (V_{OUT}) together with the level translators, and switches the substrates of S_3 and S_4 to the correct level to maintain necessary reverse bias.



NOTES: *For large values of C_{osc} (>1000 pF), the values of C_1 and C_2 should be increased to 100 μF .

Figure 1. AS1044S Test Circuit

The voltage regulator portion of the AS1044S is an integral part of the anti-latch-up circuitry. Its inherent voltage drop can, however, degrade operation at low voltages.

To improve low-voltage operation, the "LV" pin should be connected to GND, disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latch-up-proof operation and prevent device damage.

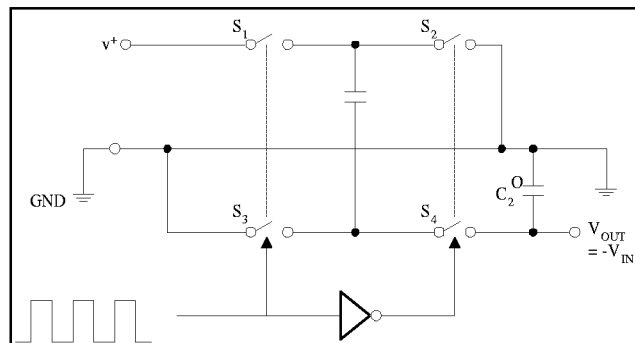


Figure 2. Idealized Switched Capacitor

THEORETICAL POWER EFFICIENCY CONSIDERATIONS

In theory, a voltage multiplier can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedances of the pump and reservoir capacitors are negligible at the pump frequency.

The AS1044S approaches these conditions for negative voltage multiplication if large values of C_1 and C_2 are used. Energy is lost only in the transfer of charge between capacitors if a change in voltage occurs. The energy lost is defined by:

$$E = 1/2 C_1 (V_1^2 - V_2^2)$$

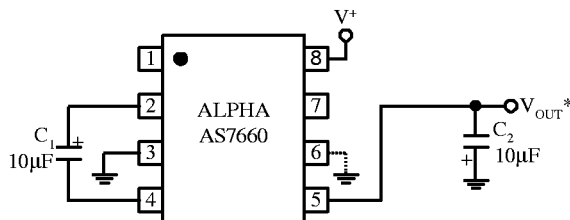
V_1 and V_2 are the voltages on C_1 during the pump and transfer cycles. If the impedances of C_1 and C_2 are relatively high at the pump frequency (refer to Figure 2) compared to the value of R_L , there will be a substantial difference in voltages V_1 and V_2 . Therefore, it is desirable not only to make C_2 as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for C_1 in order to achieve maximum efficiency of operation.

DOS AND DON'TS

- Do not exceed maximum supply voltages.
- Do not connect the LV terminal to GND for supply voltages greater than 3.5V.
- Do not short circuit the output to V⁺ supply for voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
- When using polarized capacitors in the inverting mode, the + terminal of C₁ must be connected to pin 2 of the AS1044S and the + terminal of C₂ must be connected to GND.

SIMPLE NEGATIVE VOLTAGE CONVERTER

Figure 3 shows typical connections to provide a negative supply where a positive supply is available. A similar scheme may be employed for supply voltages anywhere in the operating range of +1.5V to +12V, keeping in mind that pin 6 (LV) is tied to the supply negative (GND) only for supply voltages below 3.5V.



*NOTES: $V_{OUT} = -n V^+$ for $1.5V \leq V^+ \leq 12V$

Figure 3. Simple Negative Converter

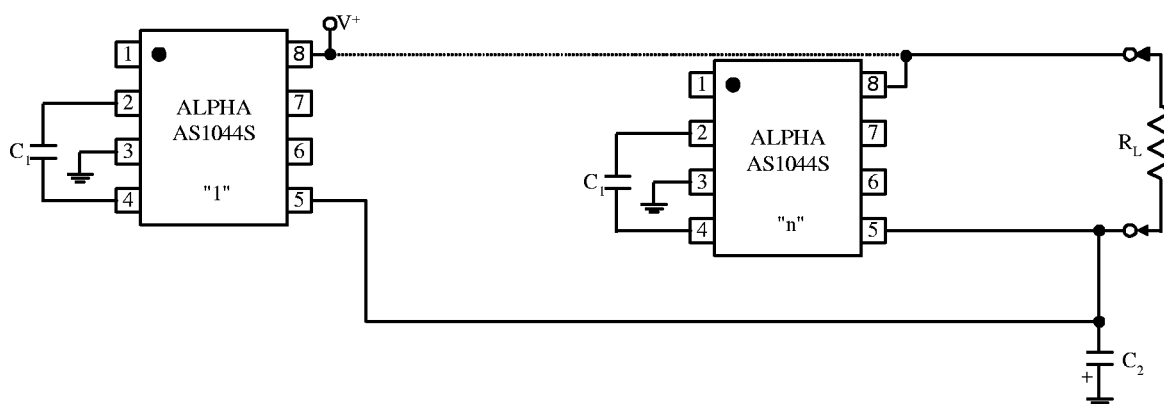


Figure 4. Paralleling Devices Lowers Output Impedance

The output characteristics of the circuit in Figure 3 are those of a nearly ideal voltage source in series with 70Ω. Thus, for a load current of -10 mA and a supply voltage of +5V, the output voltage would be -4.3V

The dynamic output impedance of the AS1044S is due, primarily, to capacitive reactance of the charge transfer capacitor (C₁). Since this capacitor is connected to the output for only 1/2 of the cycle, the equations is:

$$X_C = \frac{2}{2\pi f C_1} = 3.18\Omega,$$

where $f = 10 \text{ kHz}$ and $C_1 = 10\mu\text{F}$.

PARALLELING DEVICES

Any number of AS1044S voltage converters may be paralleled to reduce output resistance (Figure 4). The reservoir capacitor, C₂, serves all devices, while each device requires its own pump capacitor, C₁. The resultant output resistance would be approximately:

$$R_{OUT} = \frac{R_{OUT} \text{ (of AS1044S)}}{n \text{ (number of devices)}}$$

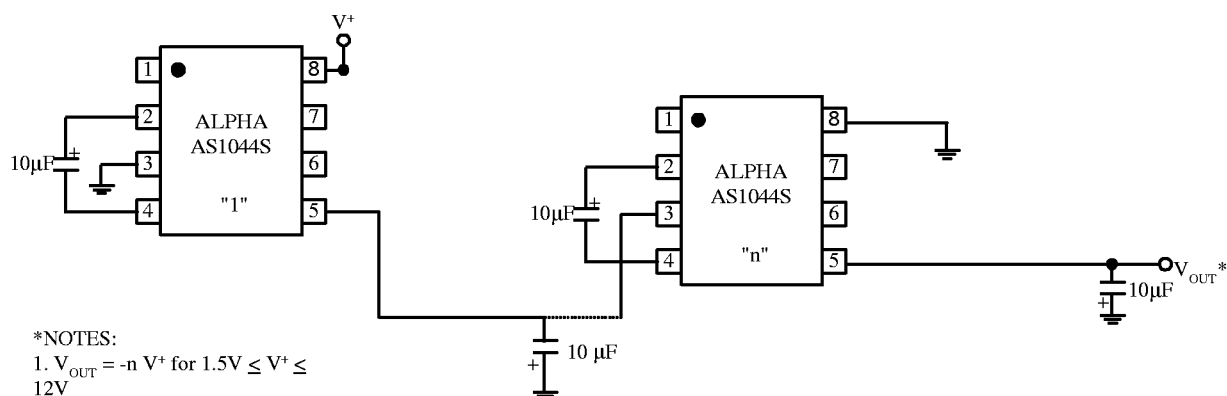


Figure 5. Increased Output Voltage by Cascading Devices

CASCADING DEVICES

The AS1044S may be cascaded as shown (Figure 5) to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined by:

$$V_{OUT} = -n (V_{IN})$$

where n is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual AS1044S R_{OUT} values.

CHANGING THE AS1044S OSCILLATOR FREQUENCY

It may be desirable in some applications (due to noise or other considerations) to increase the oscillator frequency. Pin 1, frequency boost pin may be connected to V^+ to increase oscillator frequency to 45 kHz from a nominal of 10 kHz for an input supply voltage of 5.0 volts. The oscillator may also be synchronized to an external clock as shown in Figure 6. In order to prevent possible device latch-up, a 1 k Ω resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10k Ω pull-up resistor to V^+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be 1/2 of the clock frequency. Output transitions occur on the positive-going edge of the clock.

It is also possible to increase the conversion efficiency of the AS1044S at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is achieved by connecting an additional capacitor, C_{OSC} , as shown in Figure 7. Lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump (C_1) and the reservoir (C_2) capacitors. To overcome this, increase the values of C_1 and C_2 by the same factor

that the frequency has been reduced. For example, the addition of a 100 pF capacitor between pin 7 (OSC) and pin 8 (V^+) will lower the oscillator frequency to 1 kHz from its nominal frequency of 10 kHz (a multiple of 10), and necessitate a corresponding increase in the values of C_1 and C_2 (from 10 μ F to 100 μ F).

POSITIVE VOLTAGE MULTIPLICATION

The AS1044S may be employed to achieve positive voltage multiplication using the circuit shown in Figure 8. In this application, the pump inverter switches of the AS1044S are used to charge C_1 to a voltage level of $V^+ - V_F$ (where V^+ is the supply voltage and V_F is the forward voltage drop of diode D_1). On the transfer cycle, the voltage on C_1 plus the supply voltage (V^+) is applied through diode D_2 to capacitor C_2 . The voltage thus created on C_2 becomes $(2 V^+) - (2 V_F)$, or twice the supply voltage minus the combined forward voltage drops of diodes D_1 and D_2 .

The source impedance of the output (V_{OUT}) will depend on the output current, but for $V^+ = 5V$ and an output current of 10 mA, it will be approximately 60 Ω .

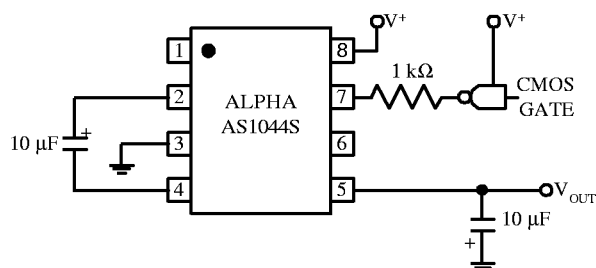


Figure 6. External Clocking

COMBINED NEGATIVE VOLTAGE CONVERSION AND POSITIVE SUPPLY MULTIPLICATION

Figure 9 combines the functions shown in Figures 3 and 8 to provide negative voltage conversion and positive voltage multiplication simultaneously. This approach would be for example, suitable for generating +9V and -5V from an existing +5V supply. In this instance, capacitors C_1 and C_3 perform the pump and reservoir function, respectively, for the generation of the negative voltage, while capacitors C_2 and C_4 are pump and reservoir, respectively, for the multiplied positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher due to the finite impedance of the common charge pump driver at pin 2 of the device.

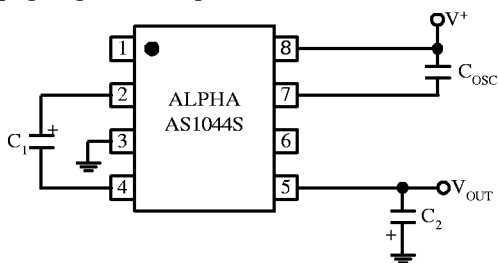


Figure 7. Lowering Oscillator Frequency

EFFICIENT POSITIVE VOLTAGE MULTIPLICATION/CONVERSION

Since the switches that allow the charge pumping operation are bi-directional, the charge transfer can be performed backwards as easily as forwards. Figure 10 shows a AS1044S transforming -5V to +5V (or +5V to +10V, etc.). The only problem here is that the internal clock and switch-drive section will not operate until some positive voltage has been generated. An initial inefficient pump, as shown in Figure 9, could be used to start this circuit up, after which it will bypass the other (D_1 and D_2 in Figure 9 would never turn on), or else the diode and resistor shown dotted in Figure 10 can be used to “force” the internal regulator on.

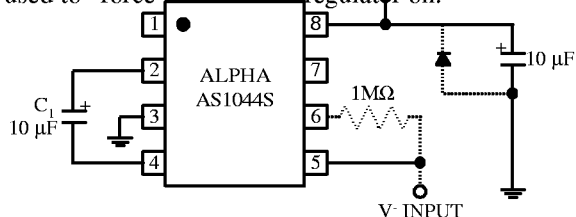


Figure 10. Positive Voltage Conversion

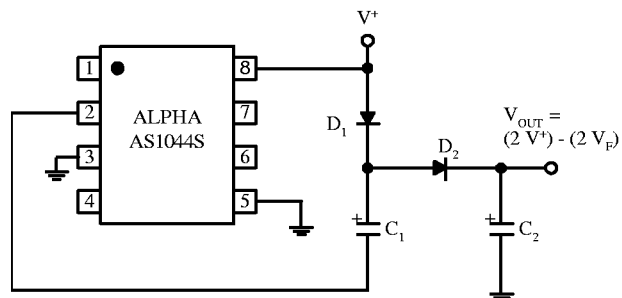


Figure 8. Positive Voltage Multiplier

VOLTAGE SPLITTING

The same bi-directional characteristics used in Figure 10 can also be used to split a higher supply in half, as shown in Figure 11. The combined load will be evenly shared between the two sides. Once again, a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 5, +15V can be converted (via +7.5V and -7.5V) to a nominal -15V, though with rather high series resistance ($\sim 250\Omega$).

NEGATIVE VOLTAGE GENERATION FOR DISPLAY ADCs

The AS1044S is designed to work from a 9V battery. With a fixed power supply system, the AS1044S will perform conversions with input signal referenced to power supply ground.

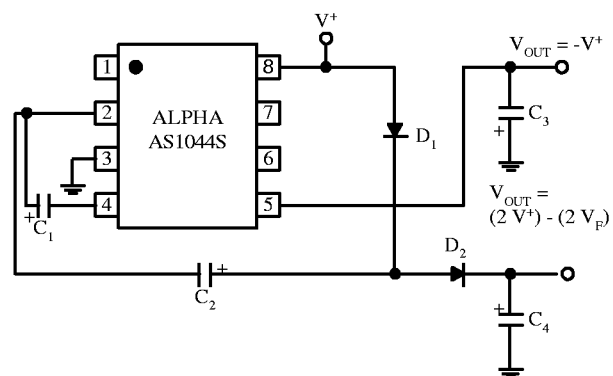


Figure 9. Combined Negative Converter and Positive Multiplier

TYPICAL CHARACTERISTICS

