REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R119-93	93-04-12	M. L. Poelking
B	Changes in accordance with NOR 5962-R122-94	94-03-03	M. L. Poelking
C	Add device class level V. Update boilerplate	97-06-06	M. L. Poelking

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Christopher A. Rauch

DEFENSE SUPPLY CENTER COLUMBUS

COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Charles Reusing

APPROVED BY
William K. Heckman

DRAWING APPROVAL DATE
5 December 1989

REVISION LEVEL
C

MICROCIRCUIT, DIGITAL, DRIVER-RECEIVER, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-88644**

SHEET 1 OF 31

DSCC FORM 2233
APR 97

5962-E109-97

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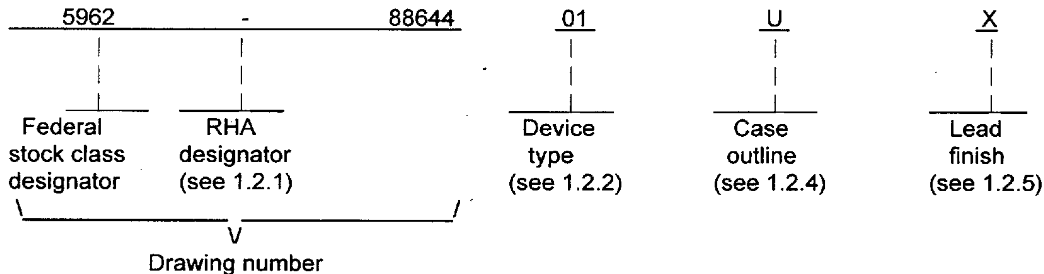
1. SCOPE

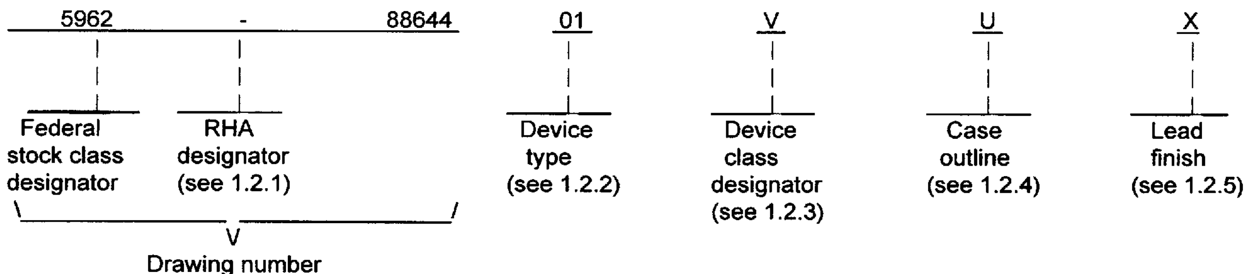
1.1 Scope. This drawing documents has two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following examples.

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	VCC	VEE	Idle
01	UT63M105	Single transceiver	+5 to +15 V	-15 V	Low
02	UT63M107	Single transceiver	+5 to +12 V	-12 V	Low
03	UT63M115	Single transceiver	+5 to +15 V	-15 V	High
04	UT63M117	Single transceiver	+5 to +12 V	-12 V	High
05	UT63M125	Multichip dual transceiver	+5 to +15 V	-15 V	Low
06	UT63M127	Multichip dual transceiver	+5 to +12 V	-12 V	Low
07	UT63M135	Multichip dual transceiver	+5 to +15 V	-15 V	High
08	UT63M137	Multichip dual transceiver	+5 to +12 V	-12 V	High

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

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Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
U	See figure 1	24	dual-in-line package
X	See figure 1	36	dual-in-line package
Y	See figure 1	36	flat package
Z	See figure 1	36	flat package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{DD} -- 7.0 V
V_{EE} -- -22 V
V_{CC} -- +22 V
Input voltage range (receiver) ---------------------------- 42 V_{PP} line to line
Logic input voltage -- -0.3 V to +5.5 V
Output current (transmitter) ------------------------------- 190 mA
Power dissipation (P_D) (per channel) ------------------------ 4 W
Maximum thermal resistance junction-to-heatsink (θ_{JS}) ------------ 6°C/W 2/
Storage temperature ------------------------------------- -65°C to +150°C
Maximum junction temperature (T_J) ------------------------- +150°C

1.4 Recommended operating conditions.

Case operating temperature range (T_C) ------------------------ -55°C to +125°C
Operating temperature junction ----------------------------- -55°C to +150°C
Supply voltage (V_{DD}) ------------------------------------ 4.5 V dc to 5.5 V dc
Supply voltage (V_{EE})
  Device types 01, 03, 05, and 07 ---------------------------- -14.25 V dc to -15.75 V dc
  Device types 02, 04, 06, and 08 ---------------------------- -11.4 V dc to -12.6 V dc
Supply voltage (V_{CC})
  Device types 01, 03, 05, and 07 ---------------------------- 4.75 V dc to 15.75 V dc
  Device types 02, 04, 06, and 08 ---------------------------- 4.75 V dc to 12.6 V dc
Input high voltage (V_{IH}) ------------------------------------ 2.0 V dc minimum
Input low voltage (V_{IL}) ------------------------------------- 0.8 V dc maximum
Radiation features:
  Total dose:
  Devices 01 and 05 -------------------------------------- ≤ 100k Rads
  Single event phenomenon (SEP) effective
    linear energy threshold, no upsets or latchup (see 4.4.4.4) --------- 3/
  Neutron fluence (TM1017) ---------------------------------- 3/

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
  logic tests (MIL-STD-883, test method 5012) ---------------------- XX percent 4/

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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.
MIL-STD-1553 - Aircraft Internal Time Division Command/Response Multiplex Data Bus.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All packages should mount to or contact a heat removal rail located in the printed circuit board. To insure proper heat transfer between the package and the heat removal rail, use a thermally conductive material between the package and the heat removal rail.
3/ Values will be added when they become available. Rad hard devices have not yet been tested for Neutron or SEP.
4/ Values will be added when they become available.

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3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 5.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55°C ≤ T_C ≤+125°C 4.5 V ≤ V_{DD} ≤ 5.5 V 2/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input low voltage RXEN, $\overline{RXEN}$ TXIHB, TXIN, $\overline{TXIN}$	V_{IL}		1, 2, 3	All		0.8	V
Input high voltage RXEN, $\overline{RXEN}$ TXIHB, TXIN, $\overline{TXIN}$	V_{IH}		1, 2, 3	All	2.0		V
Input low current RXEN, $\overline{RXEN}$ TXIHB, TXIN, $\overline{TXIN}$	I_{IL}	V_{IL} = 0.4 V	1, 2, 3	All	-1.6		mA
Input high current RXEN, $\overline{RXEN}$ TXIHB, TXIN, $\overline{TXIN}$	I_{IH}	V_{IH} = 2.4 V	1, 2, 3	All		40	µA
Output low voltage RXOUT, $\overline{RXOUT}$	V_{OL}	I_{OL} = 4.0 mA	1, 2, 3	All		0.55	V
Output high voltage RXOUT, $\overline{RXOUT}$	V_{OH}	I_{OH} = 0.4 mA	1, 2, 3	All	2.4		V
V_{DD} supply current for each channel	I_{DD}	0 percent duty cycle nontransmitting	1, 2, 3	All		60	mA
		50 percent duty cycle f = 1 MHz		All		60	
		100 percent duty cycle f = 1 MHz		All		60	
V_{CC} supply current for each channel	I_{CC}	0 percent duty cycle nontransmitting	1, 2, 3	All		10	mA
		50 percent duty cycle f = 1 MHz		All		10	
		100 percent duty cycle f = 1 MHz		All		10	

See footnotes at end of table

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{DD} \leq 5.5 V$ 2/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
V_{EE} supply current for each channel	I_{EE}	0 percent duty cycle nontransmitting	1, 2, 3	02, 04 06, 08		40	mA
		50 percent duty cycle f = 1 MHz				140	
		100 percent duty cycle f = 1 MHz				230	
		0 percent duty cycle nontransmitting	1, 2, 3	01, 03 05, 07		40	mA
		50 percent duty cycle f = 1 MHz				140	
		100 percent duty cycle f = 1 MHz				230	
Power dissipation for each channel	P_{CD}	0 percent duty cycle nontransmitting	1, 2, 3	02, 04 06, 08		0.9	W
		50 percent duty cycle f = 1 MHz				2.1	
		100 percent duty cycle f = 1 MHz				3.3	
		0 percent duty cycle nontransmitting		01, 03 05, 07		1.0	W
		50 percent duty cycle f = 1 MHz				2.5	
		100 percent duty cycle f = 1 MHz				3.8	
Input threshold voltage (no response) 3/	V_{TH1}	Transformer-coupled stub, input at f = 1MHz, rise/ fall time 200 ns at receiver 0→ 1 transition	4, 5, 6	All		0.20	V_{PP} L-L

See footnotes at end of table

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{DD} \leq 5.5 V$ 2/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input threshold voltage (no response)	V_{TH2}	Direct-coupled stub, input at f = 1MHz, rise/ fall time 200 ns at receiver 0→ 1 transition	4, 5, 6	All		0.28	V_{PP} L-L
Input threshold voltage (response) 3/	V_{TH3}	Transformer-coupled stub, input at f = 1MHz, rise/ fall time 200 ns at receiver 0→ 1 transition			.86	14.0	
Input threshold voltage (response)	V_{TH4}	Direct-coupled stub, input at f = 1MHz, rise/ fall time 200 ns at receiver 0→ 1 transition			1.20	20.0 2/	
Differential (receiver) input impedance 3/	R_{IZ}	Input = 1 MHz, no transformer in circuit	4, 5, 6	All	15		kΩ
Input capacitance 3/	C_{IN}	TXIHB, TXIN, $\overline{TXIN}$ V_{IN} = 0 V, f = 1 MHz	4, 5, 6	All		10	pF
Common mode input voltage 3/	V_{IC}	Direct coupled stub, V_{IN} = 1.2 V_{PP}, 200 ns rise/fall time ±25 ns, f = 1 MHz	4, 5, 6	All	-10	+10	V
Common mode rejection ratio 3/ 4/	CMMR	Pass/fail	4, 5, 6				
Output voltage swing in accordance with MIL-STD-1553	V_{01} 3/ 5/	Transformer-coupled stub, f = 1 MHz, R_L = 70Ω	4, 5, 6	All	18	27	V_{PP} L-L
	V_{02}	Direct-coupled stub, f = 1 MHz, R_L = 35Ω	4, 5, 6	All	6	9	
	V_{03} 3/ 5/	Transformer-coupled stub, f = 1 MHz, R_L = 35Ω	4, 5, 6	All	6	20	
Output noise voltage differential 3/	V_{NS}	Transformer-coupled stub f = dc to 10 MHz, R_L = 70Ω	4, 5, 6	All		14	Mv-RMS L-L
		Direct-coupled stub, f = dc to 10 MHz, R_L= 35Ω	4, 5, 6	All		5	

See footnotes at end of table

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{DD} \leq 5.5 V$ 2/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output symmetry 3/	V_{OS}	Transformer-coupled stub, $R_L = 70\Omega$, measurement taken 2.5 µs after end of transmission	4, 5, 6	All	-250	+250	mV V_{PP} L-L
		Direct-coupled stub, $R_L = 35\Omega$, measurement taken 2.5 µs after end of transmission	4, 5, 6	All	-90	+90	
Output voltage distortion (overshoot or ring) 3/	V_{DIS}	Transformer-coupled stub, $R_L = 70\Omega$	4, 5, 6	All	-900	900	mV peak line to line
		Direct-coupled stub, $R_L = 35\Omega$	4, 5, 6	All	-300	300	
Terminal input impedance 3/	T_{IZ}	Transformer coupled stub, f = 75 kHz to 1 MHz, nontransmitting R_L removed from circuit	4, 5, 6	All	1		kΩ
		Direct coupled stub, f = 75 kHz to 1 MHz, nontransmitting R_L removed from circuit	4, 5, 6	All	2		
Functional test		See 4.4.1b	7,8	All			
Transmitter output rise/fall time	t_f, t_r	Input f = 1 MHz, 50 pecent duty cycle, direct-coupled, $R_L = 35\Omega$ output at 10 through 90 percent points, $\overline{TXOUT}$, TXOUT	9, 10, 11	All	100	300	ns

See footnotes at end of table

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TABLE IA. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \leq T_C \leq +125°C$ $4.5 V \leq V_{DD} \leq 5.5 V$ 2/ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Zero crossing distortion	t_{RZCD}	Direct coupled stub, Input f = 1 MHz, 3 V_{PP} skew input ±150 ns, rise/fall time = 200 ns	9, 10, 11	All	-150	150	ns
Zero crossing stability	t_{TZCS}	Input TXIN and $\overline{TXIN}$ should create transmitter output zero crossing at 500 ns, 1000 ns, 1500 ns, and 2000 ns (±25 ns)	9, 10, 11	All	-25	25	ns
RXOUT delay	t_{RXDD}	RXOUT to $\overline{RXOUT}$	9, 10, 11	All	-200	200	ns
TXIN skew 3/	t_{TXDD}	TXIN to $\overline{TXIN}$	9, 10, 11	All	-25	25	ns
Receiver saturation	R_{XSAT}	TXIN and $\overline{TXIN}$ @ 250 kHz, V_{CCA} = 4.75 V and 15.75 V, TXOUT = RXIN, $\overline{TXOUT}$ = $\overline{RXIN}$	9, 10, 11	All	+20	-20	ns

1/ Devices supplied to this drawing will meet all levels M, D, L and R of irradiation. However, this device is only tested at the 'R' level. Pre and Post irradiation values are identical unless otherwise specified in Table I. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

2/ V_{CC} = +4.75 V dc to +15.75 V dc and V_{EE} = -14.25 V dc to -15.75 V dc for device types 01, 03, 05, and 07.
V_{CC} = +4.75 V dc to +12.6 V dc and V_{EE} = -11.4 V dc to -12.6 V dc for device types 02, 04, 06, and 08.

3/ Guaranteed to the limit specified herein if not tested.

4/ Pass/fail criteria in accordance with MIL-HDBK-1553, appendix A, common mode rejection.

5/ Test supports all revisions of MIL-STD-1553.

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TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	T_A = Temperature ±10°C 4/	Memory pattern	V_{CC} = 4.5 V		Bias for latch-up test V_{CC} =5.5 V no latch-up LET 4/
			Effective LET no upsets [MEV/(mg/cm^2)]	Maximum device cross section (μm^2) (LET = 120)	
All	+25°C	5/	≥ 120	≤ 100	≥ 120

NOTE: Devices that contain cross coupled resistance must be tested at the maximum rated T_A

1/ For SEP test conditions, see 4.4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Values will be added when they become available. Rad hard devices have not yet been tested for SEP.

4/ Worst case temperature T_A = +125°C.

5/ For memories only.

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Case U

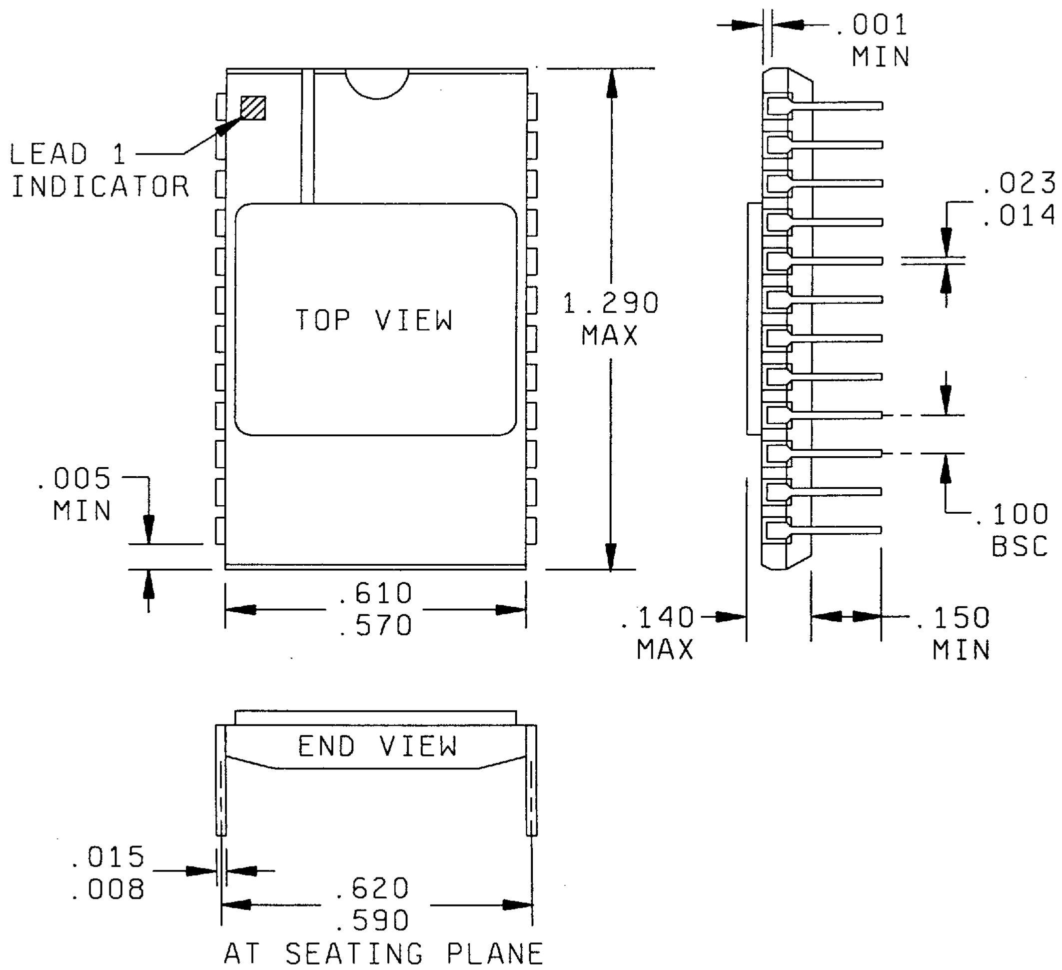

FIGURE 1. Dimensions and configurations.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-88644
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 12

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Case X

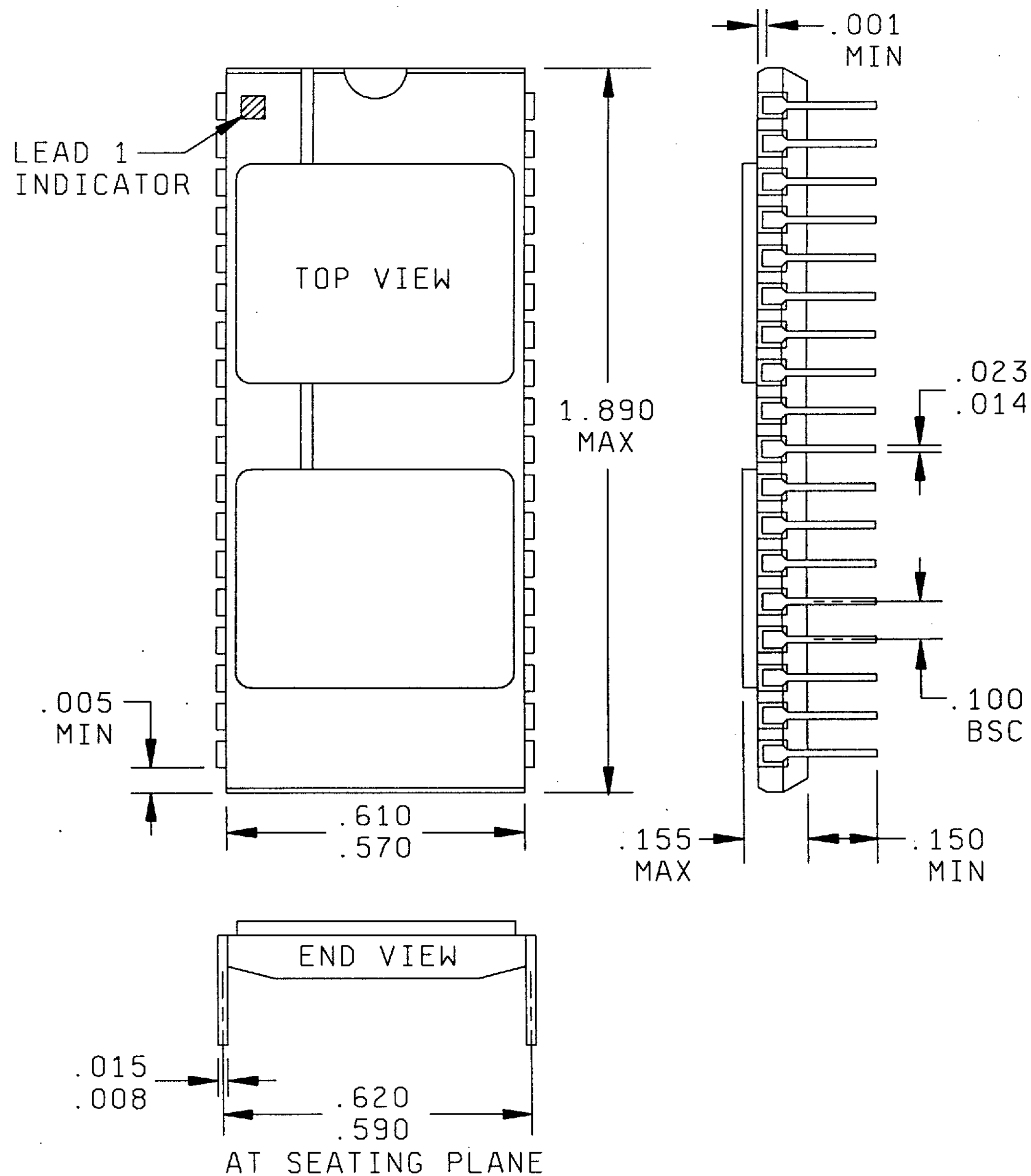

FIGURE 1. Dimensions and configurations. - Continued

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Case Y

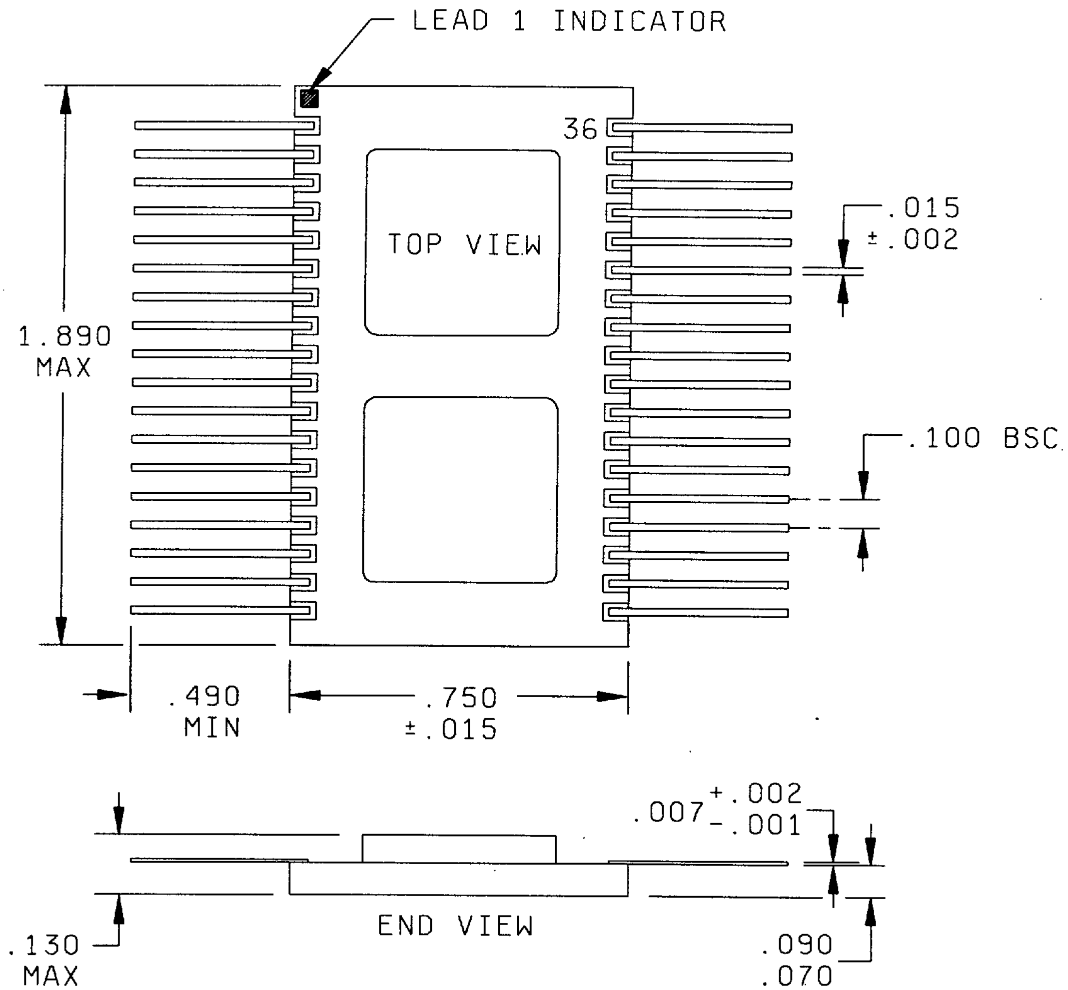

FIGURE 1. Dimensions and configurations. - Continued

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Case Z

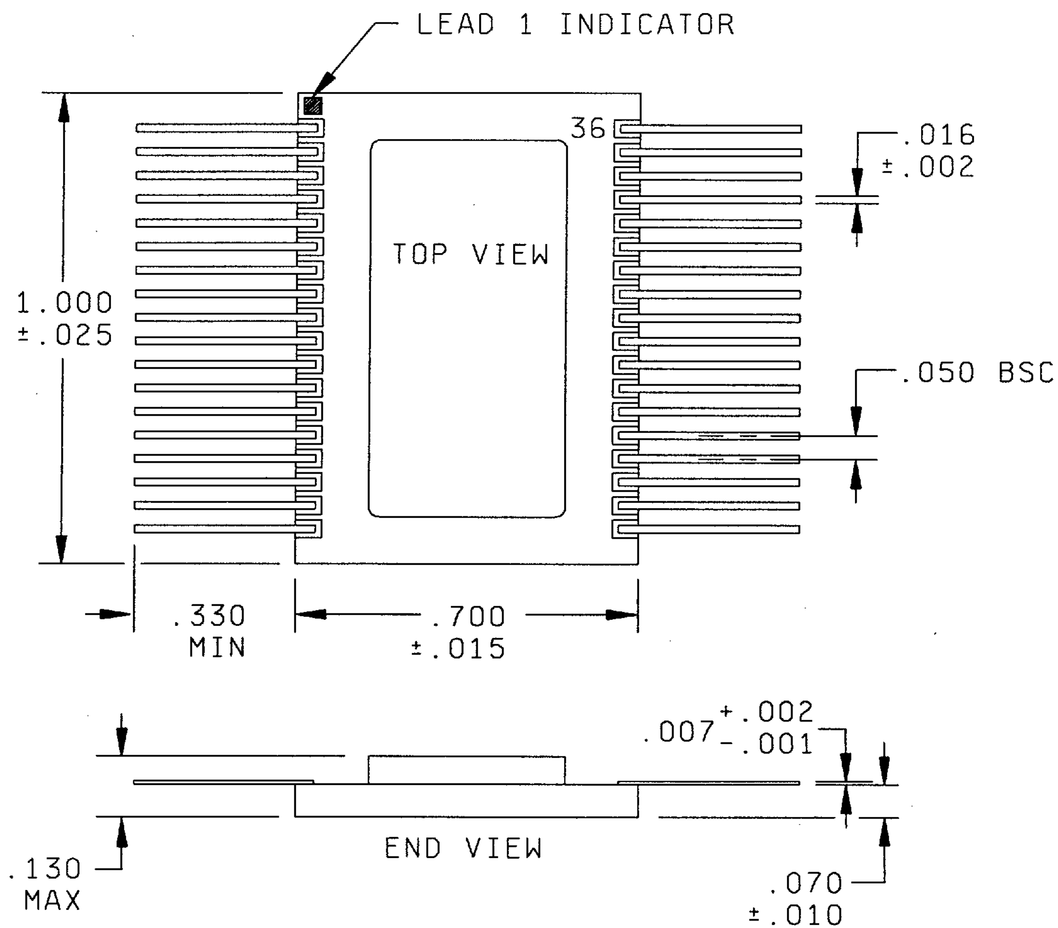

FIGURE 1. Dimensions and configurations. - Continued

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Device types 01, 02, 03, and 04
Case U

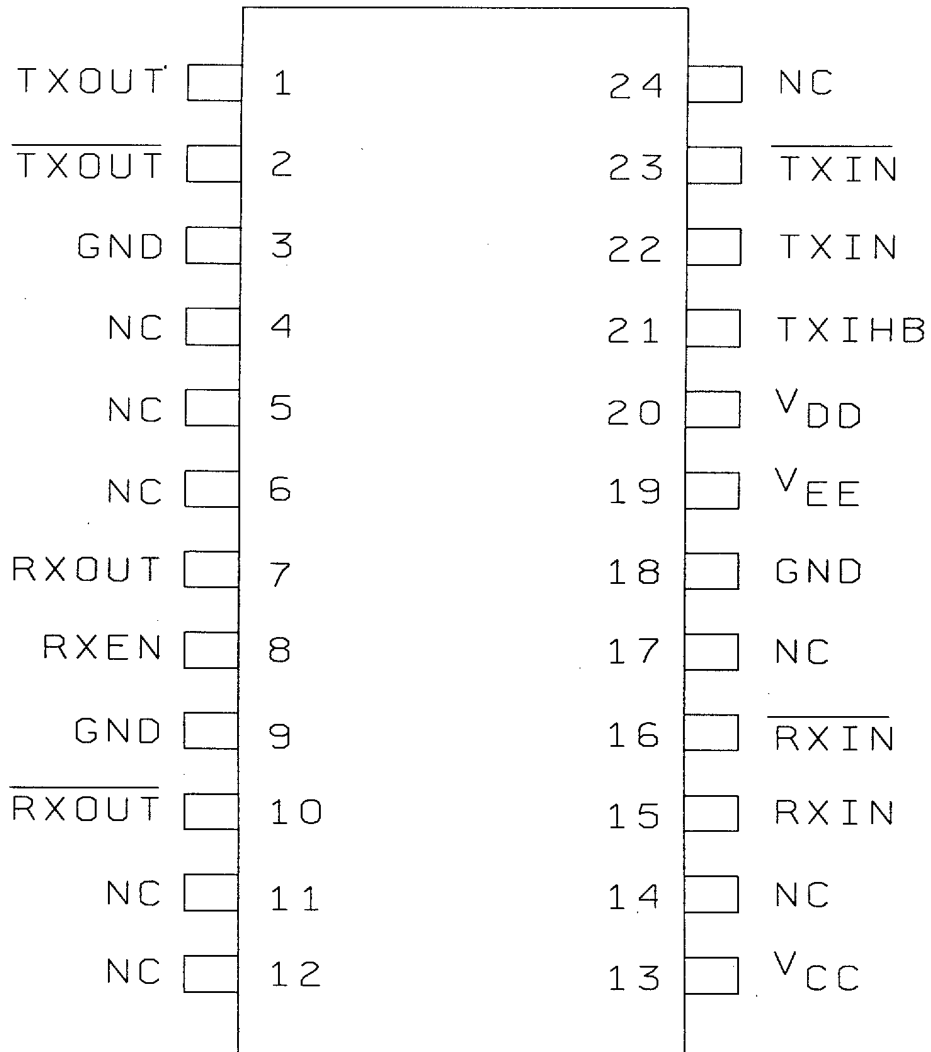

FIGURE 2. Terminal connections.

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Device types 05, 06, 07, and 08
Cases X, Y, and Z

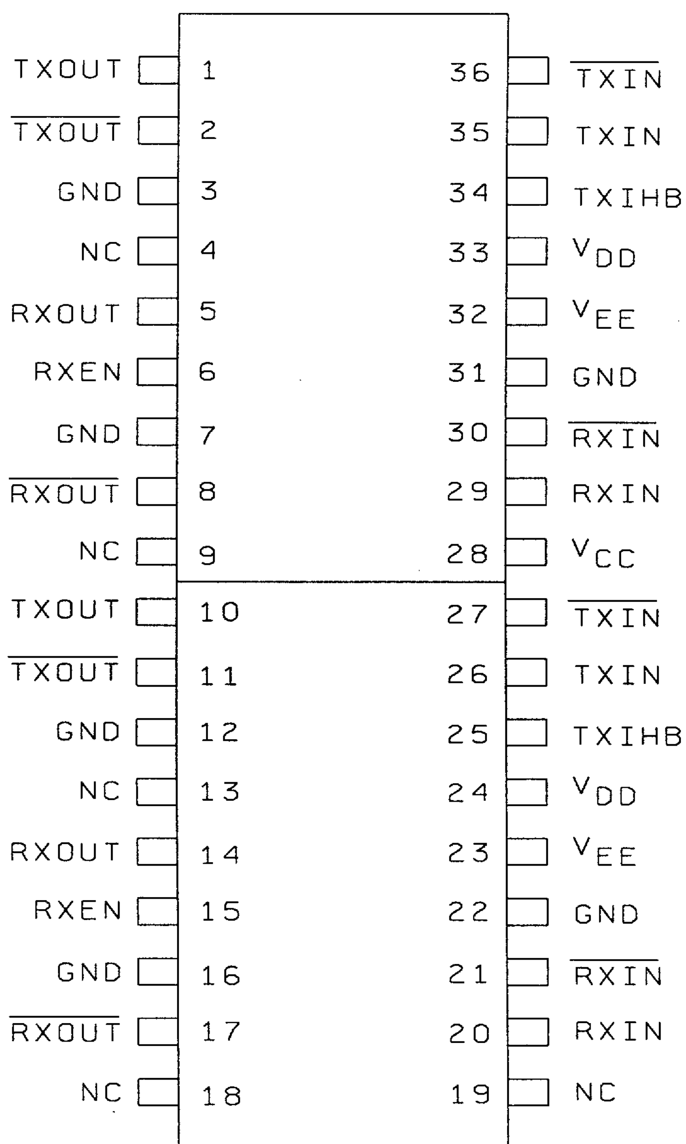

FIGURE 2. Terminal connections. - Continued

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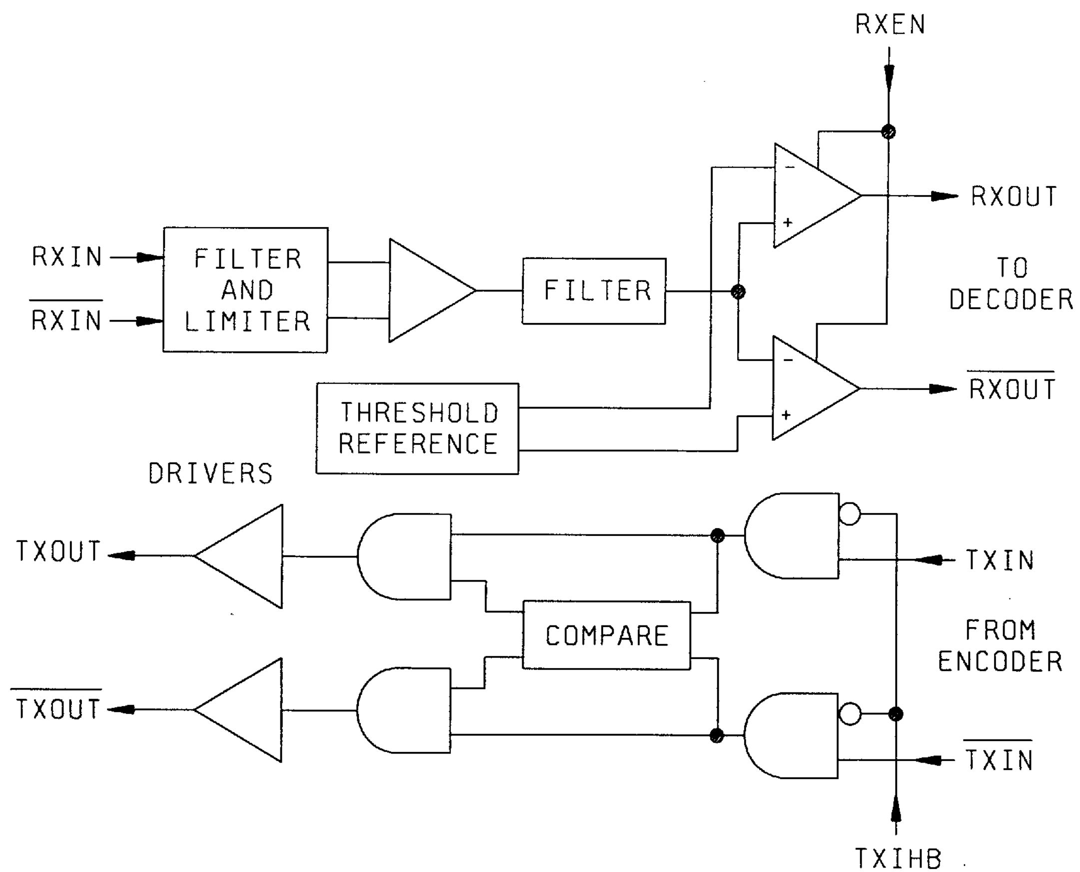

NOTE: One channel is shown for clarity.

FIGURE 3. Functional block diagram.

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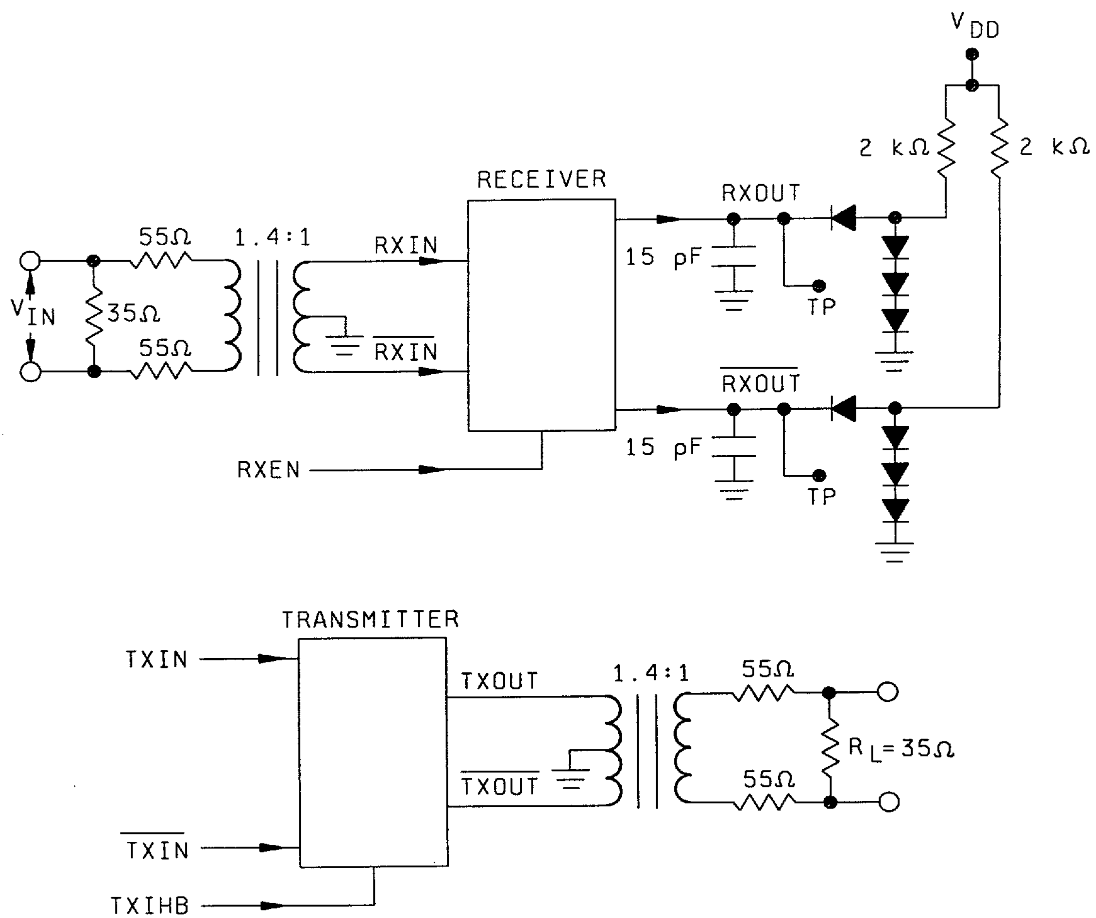
Direct coupled transceiver with load



NOTES: 1. TP = test point.
2. R_L removed for terminal.
3. TX and RX tied together.

FIGURE 4 Timing waveforms.

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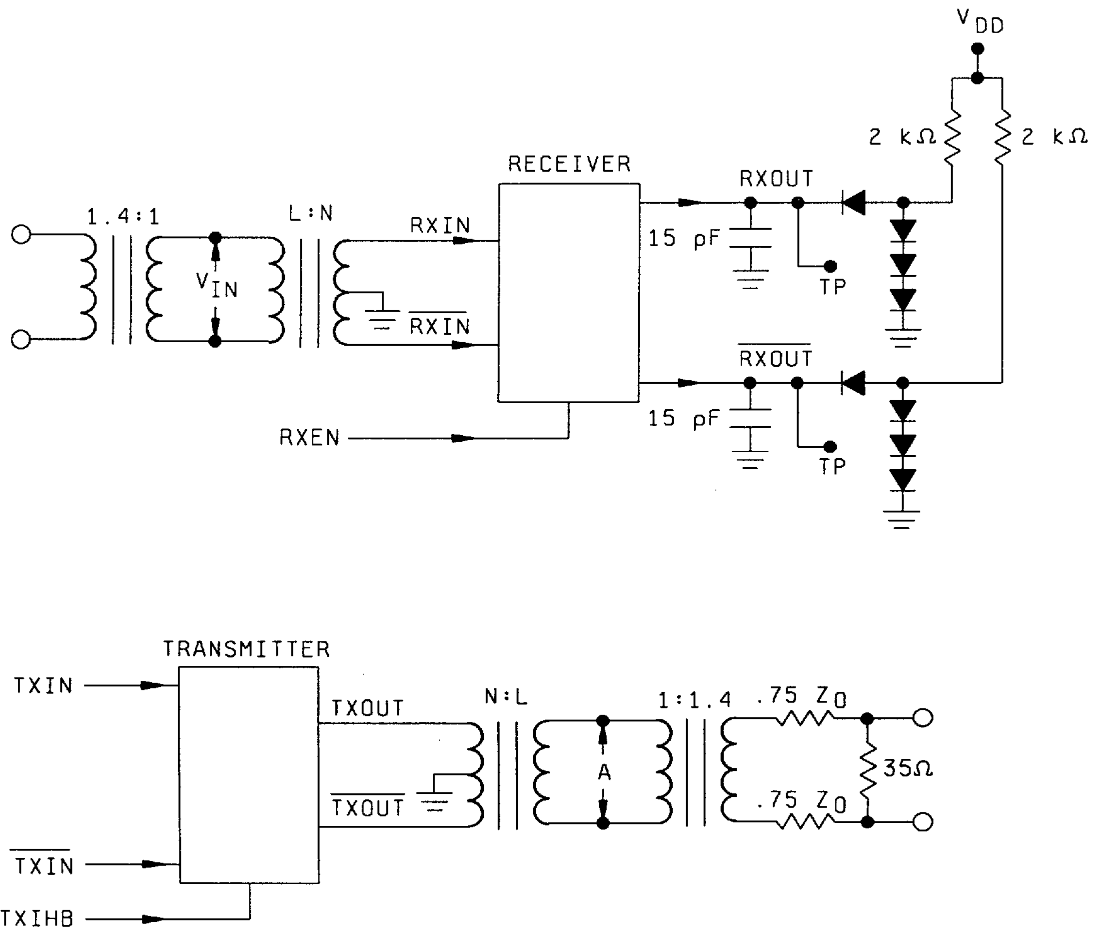
Transformer coupled transceiver with load



NOTES: 1. TP = test point.
2. N:L ratio is dependent on power supply voltage.
3. R_L removed for terminal input impedance test.
4. TX and RX tied together.

FIGURE 4 Timing waveforms. - Continued

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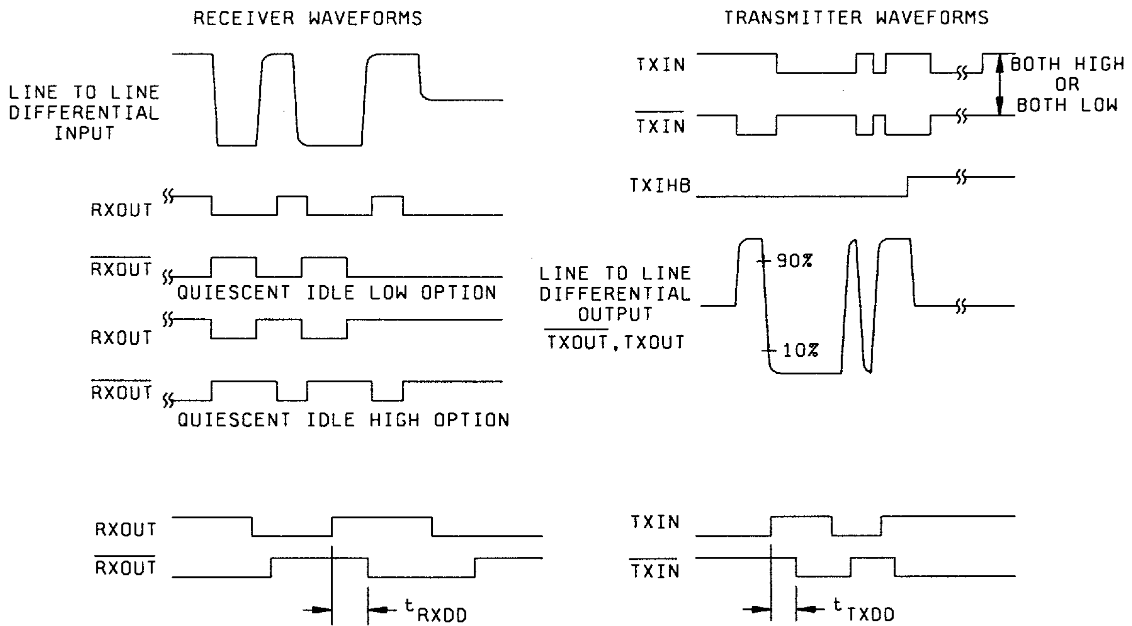

FIGURE 4 Timing waveforms. - Continued

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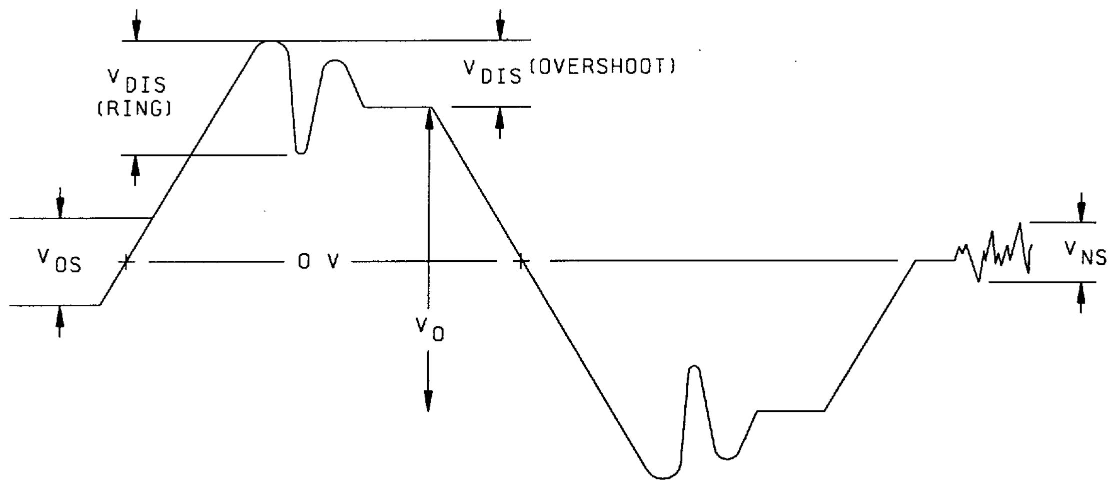
Transmitter output chacteristics (V_{DIS}, V_{OS}, V_{NS}, and V_O)



Transmitter output zero crossing stability (T_{TZCS}, t_r, and t_f)

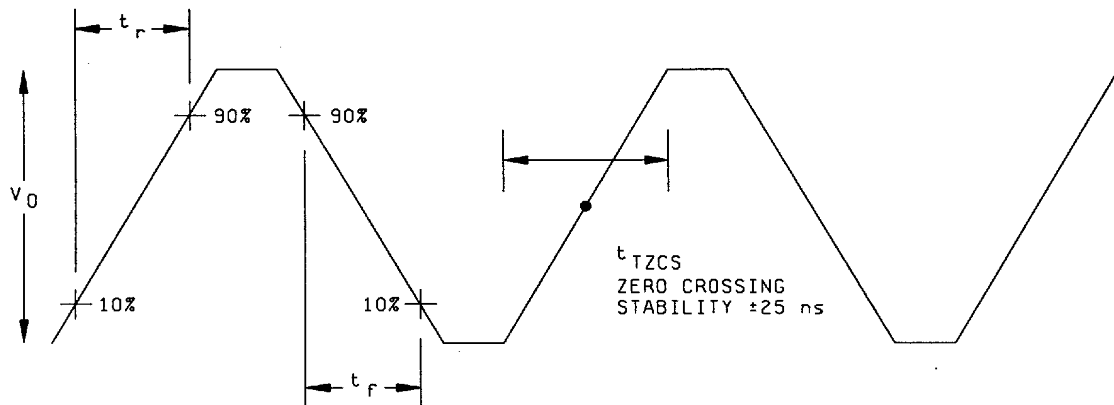


FIGURE 4 Timing waveforms. - Continued

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-88644
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 22

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Receiver input zero crossing distortion (t_{RZCD})

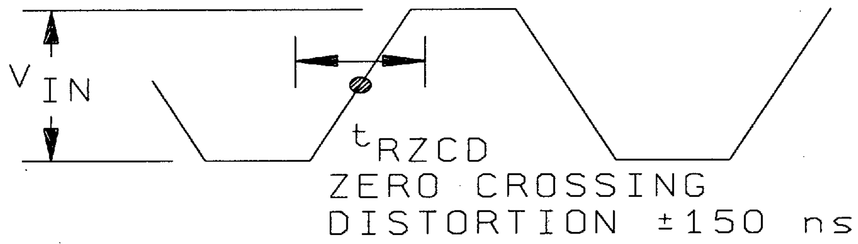

FIGURE 4 Timing waveforms. - Continued

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Device types	Open	Ground	V_{CC}	V_{CCA}	V_{EE}
01 and 05	1,2,4,5,6,7,10, 11,12,14,17,24	3,8,9,15,16,18,22	20,21,23	13	19

FIGURE 5. Radiation circuit.

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3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 053 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

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4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	----	----	----
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 4, 5, 6,8 9, 10, 11	1/ 1, 2, 3, 4, 5 6, 9, 10,11	2/ 3/ 1, 2, 3, 4, 5, 6, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8 ,9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2	1, 2	1,2
Group D end-point electrical parameters (see 4.4)	1, 2	1, 2	1, 2
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.
3/ Delta limits as specified in table IIB shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters (see Table I).

Table IIB. Burn-in Delta Parameters (+25°C)

Parameter	Symbol	Delta limits
V_{CC} supply current for each channel	I_{CC}	±0.5 mA
V_{EE} supply current for each channel	I_{EE}	±2 mA
V_{DD} supply current for each channel	I_{DD}	±3 mA
Output low voltage	V_{OL}	±60 mV
Output high voltage	V_{OH}	±100 mV

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelarated aging test. Accelaerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced lathup testing. Dose rate induced latchup testing shall be performed in accoradance with test method 1020 of MIL-STD-883 and as sprcified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accoradance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (See 1.4). SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehice as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upse or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25°C and the maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

h. For SEP test limits, see Table IB herein.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

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6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331 and as follows::

Pin description					
Name	Pin number Cases		1/ Type	1/ Active	Description
	U	X, Y, Z			
TXOUT (A)	1	1	DO		Transmitter outputs: TXOUT and $\overline{\text{TXOUT}}$ are differential data signals
TXOUT (B)	N/A	10	DO		
$\overline{\text{TXOUT}}$ (A)	2	2	DO		$\overline{\text{TXOUT}}$ is half-cycle complement of TXOUT
$\overline{\text{TXOUT}}$ (B)	N/A	11	DO		
TXIHB (A)	21	34	TI	AH	Transmitter inhibit
TXIHB (B)	N/A	25	TI	AH	
TXIN (A)	22	35	TI		Transmitter input: TXIN and $\overline{\text{TXIN}}$ are complementry TTL-level Manchester II encoder inputs
TXIN (B)	N/A	26	TI		
$\overline{\text{TXIN}}$ (A)	23	36	TI		$\overline{\text{TXIN}}$ is the complement of TXIN input
$\overline{\text{TXIN}}$ (B)	N/A	27	TI		
RXOUT (A)	7	5	TO		Receiver outputs: RXOUT and $\overline{\text{RXOUT}}$ are complementry Manchester II decoder outputs
RXOUT (B)	N/A	14	TO		
$\overline{\text{RXOUT}}$ (A)	10	8	TO		$\overline{\text{RXOUT}}$ is the complement of RXOUT output
$\overline{\text{RXOUT}}$ (B)	N/A	17	TO		
RXEN (A)	8	6	TI	AH	Receiver enable/disable
RXEN (B)	N/A	15	TI	AH	
RXIN (A)	15	29	DI		Receiver inputs: $\overline{\text{RXIN}}$ and $\overline{\text{RXIN}}$ are biphase modulated Manchester II bipolar inputs from MIL-STD-1553 data bus
RXIN (B)	N/A	20	DI		
$\overline{\text{RXIN}}$ (A)	16	30	DI		$\overline{\text{RXIN}}$ is half-cycle complement of RXIN input
$\overline{\text{RXIN}}$ (B)	N/A	21	DI		
V_{DD} (A)	20	33	PWR		+5 V dc power (±10%)
V_{DD} (B)	N/A	24	PWR		
V_{CC} (A)	13	28	PWR		+5 V dc to +12 V dc power or +5 V dc to +15 V dc power (±5%)
V_{CC} (B)	N/A	19	PWR		
V_{EE} (A)	19	32	PWR		-12 V dc to -15 V dc power (±5%)
V_{EE} (B)	N/A	23	PWR		
GND (A)	3,9,18	3,7,31	GND		Ground reference
GND (B)	N/A	12,16, 22	GND		

1/ Abbreviations: TI = TTL input, DO = Differential output, ( ) = Channel designator, TO = TTL output, DI = Differential input, AH = Active high

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6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurrence of latchup (SEP).

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-06-06

Approved sources of supply for SMD 5962-88644 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8864401UA	65342	UT63M105PBA
5962-8864401UC	65342	UT63M105PBC
5962R8864401VUA	65342	UT63M105PVA
5962R8864401VUC	65342	UT63M105PVC
5962-8864402UA	65342	UT63M107PBA
5962-8864402UC	65342	UT63M107PBC
5962-8864403UA	65342	UT63M115PBA
5962-8864403UC	65342	UT63M115PBC
5962-8864404UA	65342	UT63M117PBA
5962-8864404UC	65342	UT63M117PBC
5962-8864405XA	65342	UT63M125BBA
5962-8864405XC	65342	UT63M125BBC
5962R8864405VXA	65342	UT63M125BVA
5962R8864405VXC	65342	UT63M125BVC
5962-8864405YA	65342	UT63M125DBA
5962-8864405YC	65342	UT63M125DBC
5962R8864405VYA	65342	UT63M125DVA
5962R8864405VYC	65342	UT63M125DVC
5962-8864405ZA	65342	UT63M125CBA
5962-8864405ZC	65342	UT63M125CBC

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R8864405VZA	65342	UT63M125CVA
5962R8864405VZC	65342	UT63M125CVC
5962-8864406XA	65342	UT63M127BBA
5962-8864406XC	65342	UT63M127BBC
5962-8864406YA	65342	UT63M127DBA
5962-8864406YC	65342	UT63M127DBC
5962-8864406ZA	65342	UT63M127CBA
5962-8864406ZC	65342	UT63M127CBC
5962-8864407XA	65342	UT63M135BBA
5962-8864407XC	65342	UT63M135BBC
5962-8864407YA	65342	UT63M135DBA
5962-8864407YC	65342	UT63M135DBC
5962-8864407ZA	65342	UT63M135CBA
5962-8864407ZC	65342	UT63M135CBC
5962-8864408XA	65342	UT63M137BBA
5962-8864408XC	65342	UT63M137BBC
5962-8864408YA	65342	UT63M137DBA
5962-8864408YC	65342	UT63M137DBC
5962-8864408ZA	65342	UT63M137CBA
5962-8864408ZC	65342	UT63M137CBC

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	UTMC Microelectronics System Inc 4350 Centennial Boulevaerd Colorado Springs, Colorado 80907-3486

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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