REVISIONS			
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Defense Electronics Supply Center Dayton, Ohio	PREPARED BY Christopher A. Rauch	**MILITARY DRAWING** This drawing is available for use by all Departments and Agencies of the Department of Defense
	CHECKED BY DA DiCenzo	
Original date of drawing: 19 JAN 1988	APPROVED BY Robert P. Evans	TITLE: MICROCIRCUIT, DIGITAL, BIPOLAR, BUFFERED REGISTERS, MONOLITHIC SILICON
	SIZE: A; CODE IDENT. NO.: 67268	DWG NO. 5962-87755
AMSC N/A	REV	PAGE 1 OF 18

5962-E655

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

DESC FORM 193
MAY 86

1. SCOPE

1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".

1.2 Part number. The complete part number shall be as shown in the following example:

5962-87755	01	L	X
Drawing number	Device type (1.2.1)	Case outline (1.2.2)	Lead finish per MIL-M-38510

1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29821A	10-wide buffered register
02	29823A	9-wide buffered register
03	29825A	8-wide buffered register
04	29921A	10-wide buffered register with rotated die
05	29923A	9-wide buffered register with rotated die
06	29925A	8-wide buffered register with rotated die

1.2.2 Case outlines. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
L	D-9 (24-lead, 1/4" x 1 1/4"), dual-in-line package
K	F-6 (24-lead, 3/8" x 5/8"), flat package
3	C-4 (28-terminal, .450" x .450") square chip carrier package

1.3 Absolute maximum ratings.

Supply voltage range	-0.5 V dc to +7.0 V dc
Input voltage range	-1.5 V dc to +6.0 V dc
Storage temperature range	-65°C to +150°C
DC output voltage	-0.5 V dc to +5.5 V dc
DC output current into output	+100 mA
DC output current out of output	-50 mA
DC input current into input	-30 mA to +5.0 mA
Maximum power dissipation P_D (1/)	2.0 W
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC}):	See MIL-M-38510, appendix C
Junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Minimum high level input voltage (V_{IH})	2.0 V dc
Maximum low level input voltage (V_{IL})	0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1/ Must withstand the added P_D due to short circuit test, e.g., I_{OS}.

2. APPLICABLE DOCUMENTS

2.1 Government specification and standard. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.

3.2.4 Waveforms and test circuits. The waveforms and test circuits shall be as specified on figure 4.

3.2.5 Case outlines. The case outlines shall be in accordance with 1.2.2 herein.

3.3 Electrical performance characteristics. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full case operating temperature range.

3.4 Marking. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part number listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.

3.5 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shall state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
High level output voltage	V_{OH}	V_{CC} = 4.5 V V_{IL} = 0.8 V V_{IH} = 2.0 V	I_{OH} = -15 mA	1, 2, 3	All	2.4		V
			I_{OH} = -24 mA			2.0		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V V_{IL} = 0.8 V	I_{OL} = 32.0 mA V_{IH} = 2.0 V	1, 2, 3	All		0.5	V
Input clamp voltage	V_{IC}	V_{CC} = 4.5 V	I_{IN} = -18 mA	1, 2, 3	All		-1.2	V
Low level input current	I_{IL}	V_{CC} = 5.5 V	V_{IN} = 0.4 V	1, 2, 3	All		-0.5	mA
High level input current	I_{IH1}	V_{CC} = 5.5 V	V_{IN} = 2.7 V	1, 2, 3	All		50	µA
	I_{IH2}	V_{CC} = 5.5 V	V_{IN} = 5.5 V				100	µA
Offstate output current	I_{OZH}	V_{CC} = 5.5 V	V_{OUT} = 2.7 V	1, 2, 3	All		50	µA
	I_{OZL}	V_{CC} = 5.5 V	V_{OUT} = 0.4 V				-50	µA
Short circuit output current	I_{OS}	V_{CC} = 5.5 V	V_{OUT} = 0 V 1/	1, 2, 3	All	-75	-250	mA
Bus leakage current	I_{OFF}	V_{CC} = 0 V	V_O = 2.9 V	1, 2, 3	All		100	µA

See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Supply current	I_{CC}	V_{CC} = 5.5 V Outputs open V_{IL} = 0.8 V V_{IH} = 2.0 V	Outputs logic low	1,2,3	01,02 04,05		100	mA
					03,06		94	mA
			Outputs logic high	1,2,3	01,02 04,05		88	mA
					03,06		84	mA
			Outputs logic three-state	1,2,3	01,04		97	mA
					02,05		96	mA
					03,06		92	mA
Functional tests		See 4.3.1c		7, 8	All			
Propagation delay time from CLK to Yi	t_{PLH1}	V_{CC} = 5.0 V C_L = 50 pF ±10% R_{L1} = 500Ω ±5% R_{L2} = 500Ω ±5% (see figure 4)		9,10,11	All	3.5	9.0	ns
	t_{PHL1}			9,10,11	All	3.5	11.5	ns
Propagation delay time clear to Yi	t_{PHL2}			9,10,11	02,03 05,06		15	ns

See footnote at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output enable time $\overline{OE}$ to Yi	t_{PZH}	V_{CC} = 5.0 V C_L = 50 pF ±10% R_{L1} = 500Ω ±5% R_{L2} = 500Ω ±5% (see figure 4)	9,10,11	All		12	ns
	t_{PZL}		9,10,11	All		13	ns
Output disable time $\overline{OE}$ to Yi	t_{PHZ}		9,10,11	All		9	ns
	t_{PLZ}		9,10,11	All		9	ns
Clock pulse width	t_{PWH1} t_{PWL1}		9,10,11	All	8		ns
Data (Di) to CP setup time	t_{S1}		9,10,11	All	5		ns
Data (Di) to CP hold time	t_{H1}		9,10,11	All	2		ns

See footnote at end of table.

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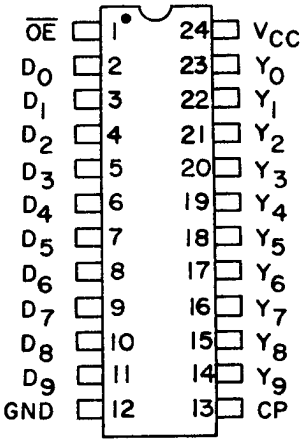
TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Enable ($\overline{EN}$ high to low) to CP setup time	t_{S2}	V_{CC} = 5.0 V C_L = 50 pF ±10% R_{L1} = 500Ω ±5% R_{L2} = 500Ω ±5% (see figure 4)	9,10,11	02,03 05,06	7		ns
Enable ($\overline{EN}$ low to high) to CP setup time	t_{S3}		9,10,11	02,03 05,06	5		ns
Enable ($\overline{EN}$) hold time	t_{H2}		9,10,11	02,03 05,06	2		ns
Clear ($\overline{CLR}$ low to high) to CP setup time	t_{S4}		9,10,11	02,03 05,06	8		ns
Clear ($\overline{CLR}$=low) pulse width	t_{PWL2}		9,10,11	02,03 05,06	7		ns

1/ Not more than one output should be shorted at a time, and the duration of the short circuit condition should not exceed 100 milliseconds.

Device type 01

Cases K and L



Device type 01

Case 3

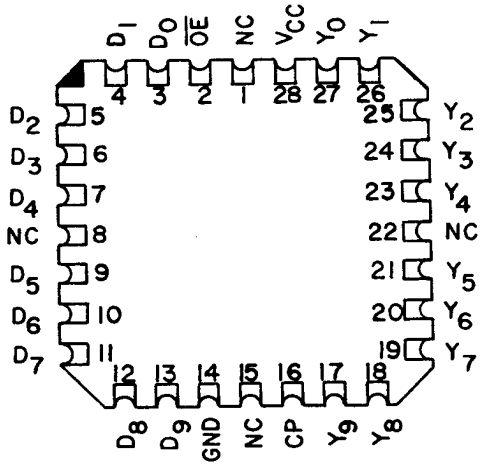
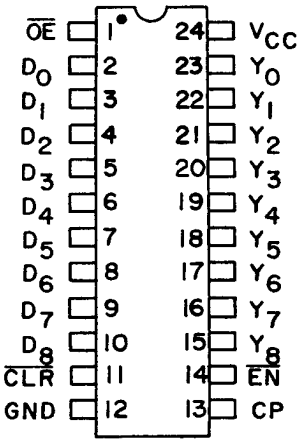


FIGURE 1. Terminal connections (top view).

Device type 02

Cases K and L



Device type 02

Case 3

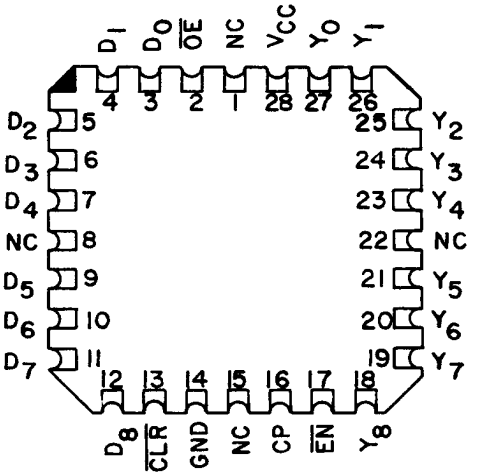


FIGURE 1. Terminal connections (top view) - Continued.

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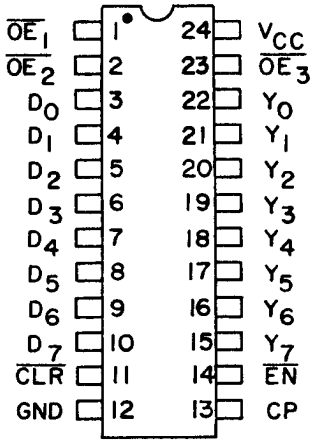
Device type 03

Cases K and L



Device type 03

Case 3

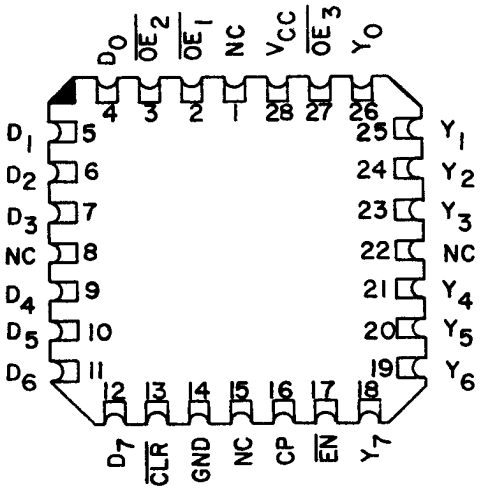
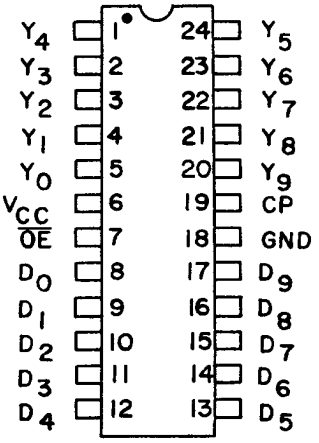


FIGURE 1. Terminal connections (top view) - Continued.

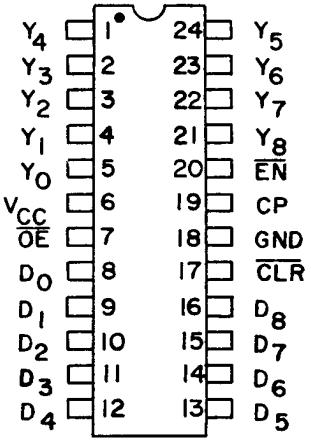
Device type 04

Case L



Device type 05

Case L



Device type 06

Case L

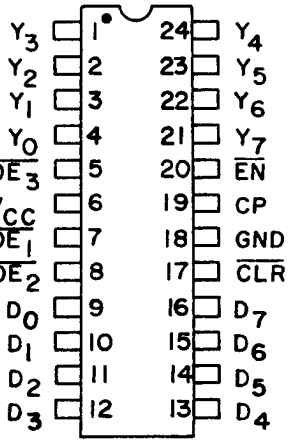


FIGURE 1. Terminal connections (top view) - Continued.

Device types 01 and 04

Inputs			Internal	Outputs
$\overline{OE}$	D_i	CP	$\overline{Q}_i$	Y_i
H	L	↑	H	Z
H	H	↑	L	Z
H	X	X	NC	Z
L	X	X	NC	NC
L	L	↑	H	L
L	H	↑	L	H

Device types 02 and 05

Inputs					Internal	Outputs
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i
H	H	L	L	↑	H	Z
H	H	L	H	↑	L	Z
H	L	X	X	X	H	Z
L	L	X	X	X	H	L
H	H	H	X	X	NC	Z
L	H	H	X	X	NC	NC
H	H	L	L	↑	H	Z
H	H	L	H	↑	L	Z
L	H	L	L	↑	H	L
L	H	L	H	↑	L	H

FIGURE 2. Truth tables.

Device types 03 and 06

Inputs					Internal	Outputs
OE*	$\overline{CLR}$	$\overline{EN}$	D_i	CP	$\overline{Q}_i$	Y_i
L	H	L	L	↑	H	Z
L	H	L	H	↑	L	Z
L	L	X	X	X	H	Z
H	L	X	X	X	H	L
L	H	H	X	X	NC	Z
H	H	H	X	X	NC	NC
L	H	L	L	↑	H	Z
L	H	L	H	↑	L	Z
H	H	L	L	↑	H	L
H	H	L	H	↑	L	H

*OE is an Active HIGH internal signal produced as follows:

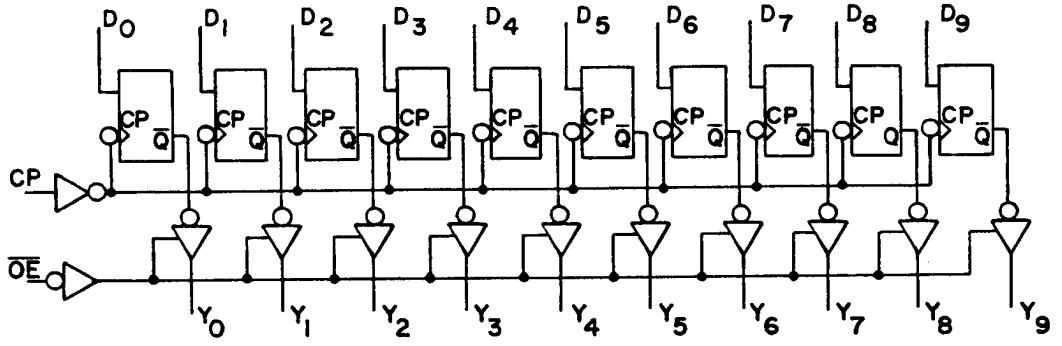
$\overline{OE}_1$	$\overline{OE}_2$	$\overline{OE}_3$	OE
H	X	X	L
X	H	X	L
X	X	H	L
L	L	L	H

H = High
L = Low
X = Don't care

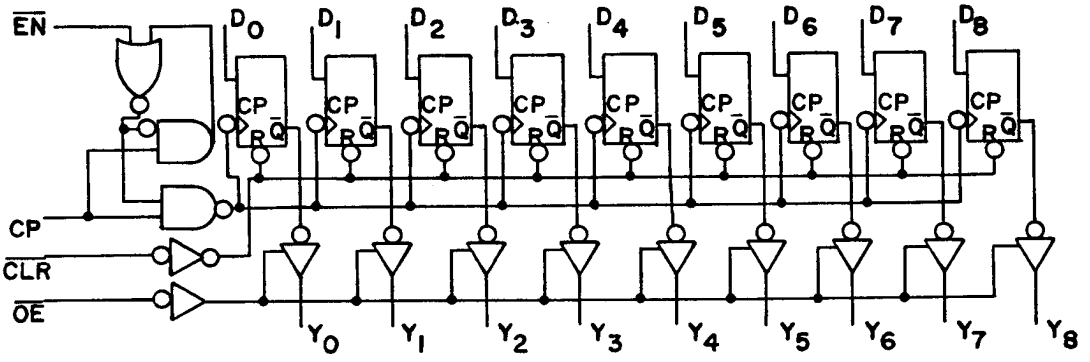
NC = No change
↑ = Low to high transition
Z = High impedance

FIGURE 2. Truth tables - Continued.

Device types 01 and 04



Device types 02 and 05



Device types 03 and 06

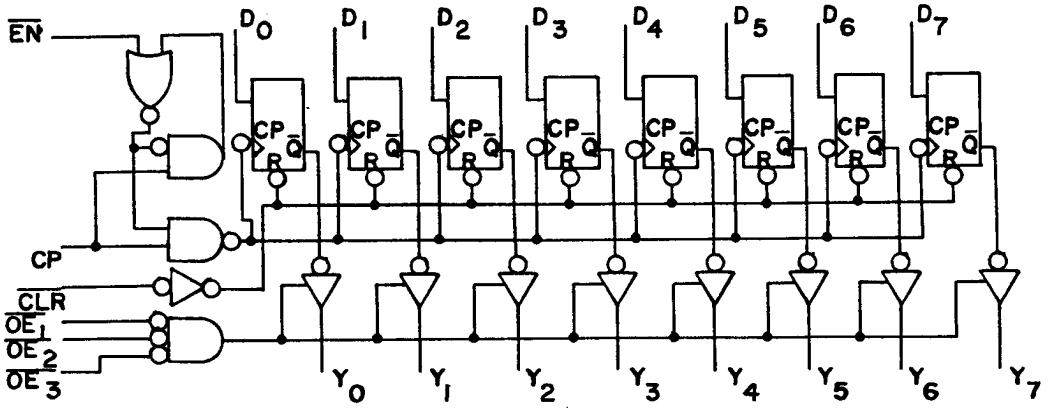


FIGURE 3. Logic diagrams.

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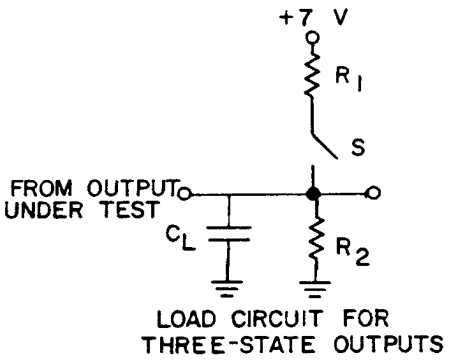
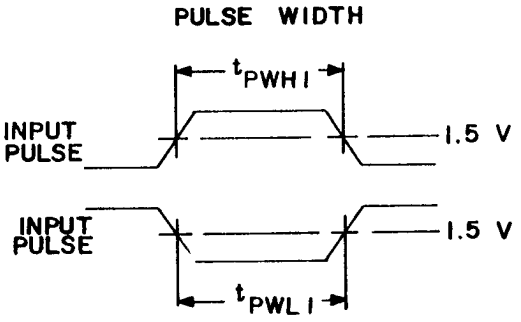
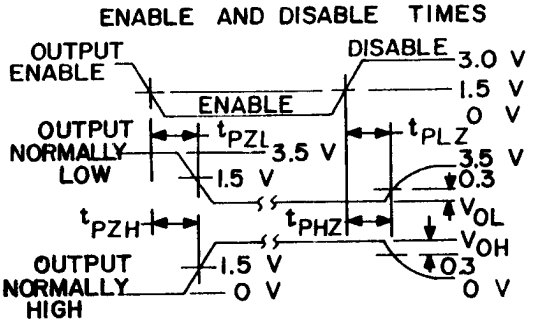


Parameter	S Position
t_{PLH}	Open
t_{PHL}	Open
t_{PHZ}	Open
t_{PZH}	Open
t_{PLZ}	Closed
t_{PZL}	Closed

Switch positions for parameter testing





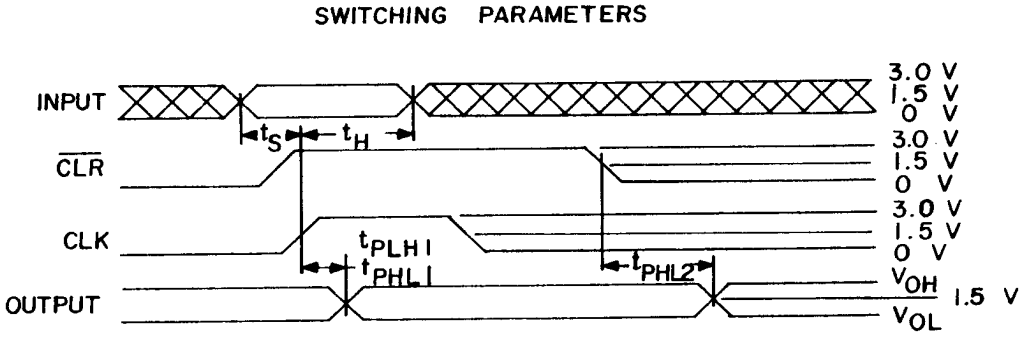


FIGURE 4. Waveforms and test circuit.

3.6 Certificate of conformance. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

3.7 Notification of change. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).

3.8 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test method 1015 of MIL-STD-883.

(1) Test condition A or C using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroups 7 and 8 tests shall verify the truth tables.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition A or C using the circuit submitted with the certificate of compliance (see 3.5 herein).

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	---
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,7,8, 9,10,11
Groups C and D end-point electrical parameters (method 5005)	1,2,3

* PDA applies to subgroups 1 and 7.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Comments. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

6.4 Approved source of supply. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor CAGE number	Vendor similar part number 1/
5962-8775501LX	34335	AM29821A/BLA
5962-8775501KX	34335	AM29821A/BKA
5962-87755013X	34335	AM29821A/B3A
5962-8775502LX	34335	AM29823A/BLA
5962-8775502KX	34335	AM29823A/BKA
5962-87755023X	34335	AM29823A/B3A
5962-8775503LX	34335	AM29825A/BLA
5962-8775503KX	34335	AM29825A/BKA
5962-87755033X	34335	AM29825A/B3A
5962-8775504LX	34335	AM29921A/BLA
5962-8775505LX	34335	AM29923A/BLA
5962-8775506LX	34335	AM29925A/BLA

1/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34335	Advanced Micro Devices, Inc. 901 Thompson Place PO Box 3453 Sunnyvale, CA 94088

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