Octal D Flip-Flop With Clear

Preliminary

Device Parameter	High Speed (74HCT)	Standard (74SC)	Military (54HCT)
Octal D flip-flop with Clear	74HCT273	74SC273	54HCT273
Operating temperature range (°C)	−40 to +85	−40 to +85	−55 to +125
Recommended operating voltage (V)	4.75 to 5.25	4.75 to 5.25	4.50 to 5.50
Maximum gate propagation delay (ns)	38	47	47

Features

- ☐ Pin and function compatible to 54/74LS equivalent circuits
- ☐ Typical DC operating supply current: 10μA
- ☐ MIL STD 883B Screening/Leadless chip carrier available
- ☐ Fast propagation delay times
- ☐ Fan out of 30 LSTTL loads
- ☐ Fully TTL and CMOS compatible
- ☐ −40°C to +85°C operating temperature range
- ☐ Capable of operating over 3-volt to 6-volt range
- ☐ High speed silicon-gate CMOS technology

General Description

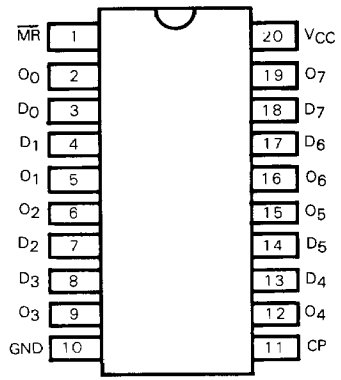
This monolithic, positive-edge-triggered flip-flop utilizes CMOS circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the postive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

FUNCTION TABLE (EACH FLIP-FLOP)

INPUTS			OUTPUT
$\overline{MR}$	CP	D	O
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Pin Configuration



Function Block Diagram