- **Members of the Texas Instruments Widebus™ Family**
- **3-State True Outputs**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Distributed V_{CC} and GND Pin Configuration Minimizes High-Speed Switching Noise**
- **EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic 300-mil Shrink Small-Outline (DL) Package Using 25-mil Center-to-Center Pin Spacings and 380-mil Fine-Pitch Ceramic Flat (WD) Package Using 25-mil Center-to-Center Pin Spacings**

54AC16472 . . . WD PACKAGE
74AC16472 . . . DL PACKAGE
(TOP VIEW)

1$\overline{OEAB}$	1	56	1$\overline{OEBA}$
1$\overline{LEAB}$	2	55	1$\overline{LEBA}$
1A1	3	54	1B1
GND	4	53	GND
1A2	5	52	1B2
1A3	6	51	1B3
V_{CC}	7	50	V_{CC}
1A4	8	49	1B4
1A5	9	48	1B5
1A6	10	47	1B6
GND	11	46	GND
1A7	12	45	1B7
1A8	13	44	1B8
1A9	14	43	1B9
2A1	15	42	2B1
2A2	16	41	2B2
2A3	17	40	2B3
GND	18	39	GND
2A4	19	38	2B4
2A5	20	37	2B5
2A6	21	36	2B6
V_{CC}	22	35	V_{CC}
2A7	23	34	2B7
2A8	24	33	2B8
GND	25	32	GND
2A9	26	31	2B9
2$\overline{LEAB}$	27	30	2$\overline{LEBA}$
2$\overline{OEAB}$	28	29	2$\overline{OEBA}$
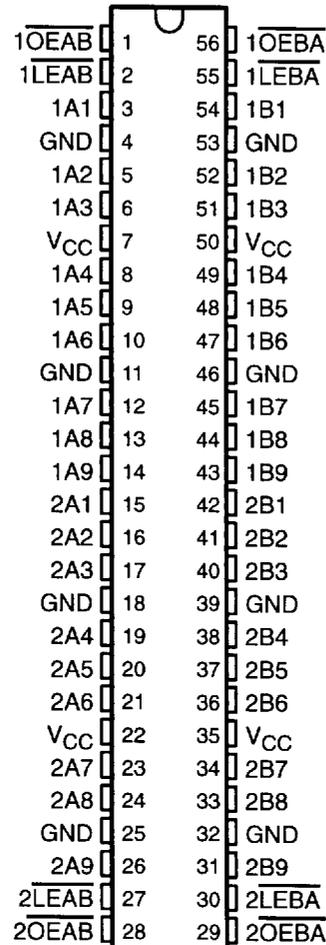
description

The 'AC16472 are 18-bit registered transceivers that contain two sets of D-type latches for temporary storage of data flowing in either direction. They can be used as two 9-bit transceivers or one 18-bit transceiver. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register to permit independent control in either direction of data flow.

When $\overline{OEAB}$ and $\overline{LEAB}$ are both low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{OEAB}$ low, the B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires the use of the $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

The 74AC16472 is packaged in TI's shrink small-outline package (DL), which provides twice the I/O pin count and functionality of standard small-outline packages in the same printed-circuit-board area.

The 54AC16472 is characterized for operation over the full military temperature range of –55°C to 125°C. The 74AC16472 is characterized for operation from –40°C to 85°C.

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TEXAS INSTRUMENTS

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FUNCTION TABLE†

INPUTS			OUTPUT
LEAB	OEAB	A	B
X	H	X	Z
H	L	X	B_0‡
L	L	H	H
L	L	L	L

† A-to-B data flow is shown: B-to-A flow is similar but uses LEBA and OEBA.

‡ Output level before the indicated steady-state input conditions were established

logic symbol§
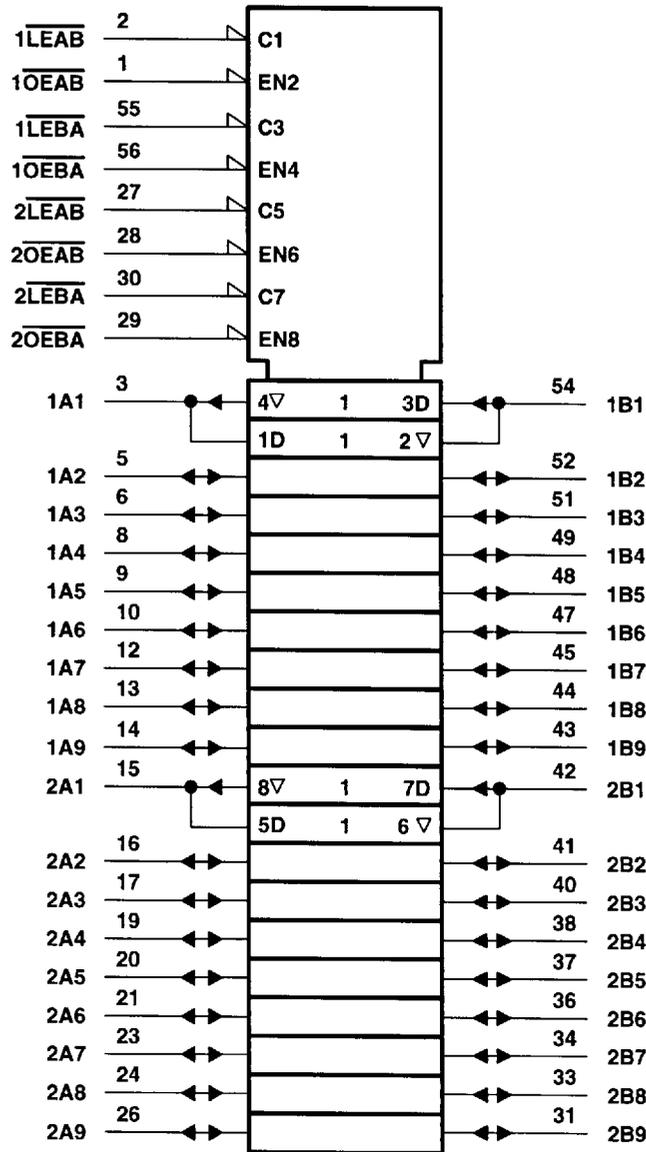
§ This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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logic diagram (positive logic)

To Eight Other Channels

To Eight Other Channels

3

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1)	−0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±50 mA
Continuous current through V_{CC} or GND	±450 mA
Maximum power package dissipation at $T_A = 55°C$ (in still air) (see Note 2): DL package	1.4 W
Storage temperature range, T_{stg}	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

recommended operating conditions (see Note 3)

			54AC16472			74AC16472			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		3	5	5.5	3	5	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 3$ V	2.1			2.1			V
		$V_{CC} = 4.5$ V	3.15			3.15			
		$V_{CC} = 5.5$ V	3.85			3.85			
V_{IL}	Low-level input voltage	$V_{CC} = 3$ V			0.9			0.9	V
		$V_{CC} = 4.5$ V			1.35			1.35	
		$V_{CC} = 5.5$ V			1.65			1.65	
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 3$ V			−4			−4	mA
		$V_{CC} = 4.5$ V			−24			−24	
		$V_{CC} = 5.5$ V			−24			−24	
I_{OL}	Low-level output current	$V_{CC} = 3$ V			12			12	mA
		$V_{CC} = 4.5$ V			24			24	
		$V_{CC} = 5.5$ V			24			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	0		10	ns/V
T_A	Operating free-air temperature		−55		125	−40		85	°C

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	$T_A = 25°C$			54AC16472		74AC16472		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		$I_{OH} = -50 \mu A$	3 V	2.9			2.9		2.9		V
			4.5 V	4.4			4.4		4.4		
			5.5 V	5.4			5.4		5.4		
		$I_{OH} = -4 mA$	3 V	2.58			2.48		2.48		
		$I_{OL} = -24 mA$	4.5 V	3.94			3.8		3.8		
			5.5 V	4.94			4.8		4.8		
		$I_{OH} = -75 mA†$	5.5 V				3.85		3.85		
V_{OL}		$I_{OL} = 50 \mu A$	3 V			0.1		0.1		0.1	V
			4.5 V			0.1		0.1		0.1	
			5.5 V			0.1		0.1		0.1	
		$I_{OL} = 12 mA$	3 V			0.36		0.44		0.44	
		$I_{OL} = 24 mA$	4.5 V			0.36		0.44		0.44	
			5.5 V			0.36		0.44		0.44	
		$I_{OL} = 75 mA†$	5.5 V					1.65		1.65	
I_I	Control inputs	$V_I = V_{CC}$ or GND	5.5 V		±0.1			±1		±1	μA
$I_{OZ}‡$	A or B ports	$V_O = V_{CC}$ or GND	5.5 V		±0.5			±5		±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V		8			80		80	μA
C_i	Control inputs	$V_I = V_{CC}$ or GND	5 V		3						pF
C_{io}	A or B ports	$V_O = V_{CC}$ or GND	5 V		11.5						pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.
‡ For I/O ports, the parameter I_{OZ} includes the input leakage current.

timing requirements over recommended operating free-air temperature range, $V_{CC} = 3.3 V \pm 0.3 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25°C$		54AC16472		74AC16472		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	4		4		4		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	0.5		0.5		0.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	3.5		3.5		3.5		ns

timing requirements over recommended operating free-air temperature range, $V_{CC} = 5 V \pm 0.5 V$ (unless otherwise noted) (see Figure 1)

		$T_A = 25°C$		54AC16472		74AC16472		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration, $\overline{LEAB}$ or $\overline{LEBA}$ low	4		4		4		ns
t_{su}	Setup time, data before $\overline{LEAB}$ or $\overline{LEBA}$ ↑	0.5		0.5		0.5		ns
t_h	Hold time, data after $\overline{LEAB}$ or $\overline{LEBA}$ ↑	2.5		2.5		2.5		ns

TEXAS INSTRUMENTS

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V $\pm$ 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16472		74AC16472		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	3.5	8	12.5	3.5	14.2	3.5	14.2	ns
t_{PHL}			3.9	8.4	12.8	3.9	13.9	3.9	13.9	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	4.8	10.3	15.6	4.8	17.9	4.8	17.9	ns
t_{PHL}			4.7	9.7	14.7	4.7	16.3	4.7	16.3	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3.9	8.9	14	3.9	15.9	3.9	15.9	ns
t_{PZL}			5	11.2	17.6	5	19.7	5	19.7	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.4	7	9.4	4.4	10	4.4	10	ns
t_{PLZ}			4	6.4	8.7	4	9.4	4	9.4	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			54AC16472		74AC16472		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	2.9	5.6	8.4	2.9	9.5	2.9	9.5	ns
t_{PHL}			3.1	6	8.7	3.1	9.6	3.1	9.6	
t_{PLH}	$\overline{LEBA}$ or $\overline{LEAB}$	A or B	3.9	7.3	10.3	3.9	11.7	3.9	11.7	ns
t_{PHL}			3.7	6.9	9.7	3.7	10.9	3.7	10.9	
t_{PZH}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	3.1	6.2	8.9	3.1	10.2	3.1	10.2	ns
t_{PZL}			3.9	7.3	10.4	3.9	11.6	3.9	11.6	
t_{PHZ}	$\overline{OEBA}$ or $\overline{OEAB}$	A or B	4.3	6.2	8.1	4.3	8.6	4.3	8.6	ns
t_{PLZ}			3.8	5.7	7.4	3.8	8	3.8	8	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance per transceiver	Outputs enabled	C_L = 50 pF, f = 1 MHz	59	pF
	Outputs disabled		6	

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PARAMETER MEASUREMENT INFORMATION
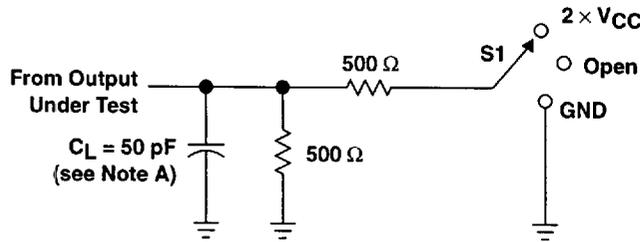
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

**LOAD CIRCUIT**
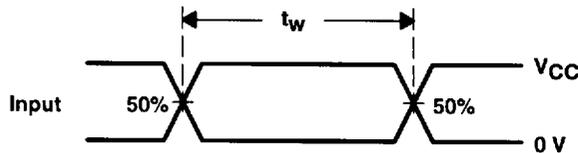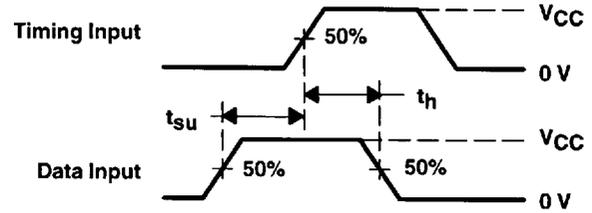
VOLTAGE WAVEFORMS
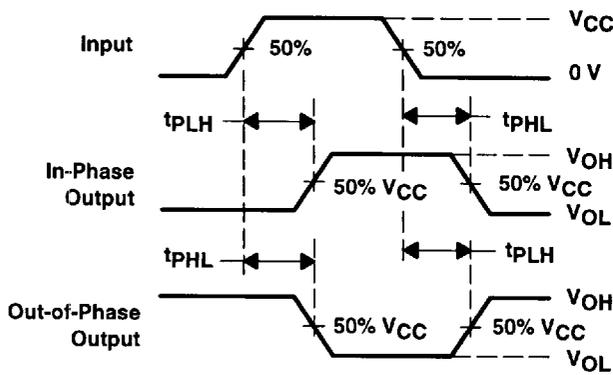
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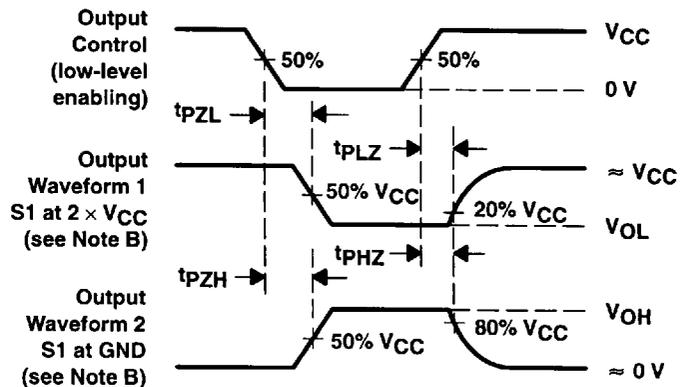
VOLTAGE WAVEFORMS

VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
   Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50 \Omega$, $t_r = 3$ ns, $t_f = 3$ ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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