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Memory Products	

27C210

1 MEG CMOS EPROM (64K × 16)

DESCRIPTION

Philips Components-Signetics 27C210 CMOS EPROM is a 1,048,576-bit 5V read only memory organized as 65,536 words of 16 bits each. It employs advanced CMOS circuitry for systems requiring low power, high-performance speeds, and immunity to noise. The 27C210 has a non-multiplexed addressing interface and is plug-compatible with the industry standard 27210.

Quick-pulse programming is employed on plastic devices which may speed up programming by as much as one hundred times. In the absence of quick-pulse programming equipment, the intelligent programming algorithm may be utilized.

The 27C210 is offered in windowed Ceramic Dual In-Line, Plastic Dual In-Line and Plastic Leaded Chip Carrier (PLCC) packages. This device can be programmed with standard EPROM programmers.

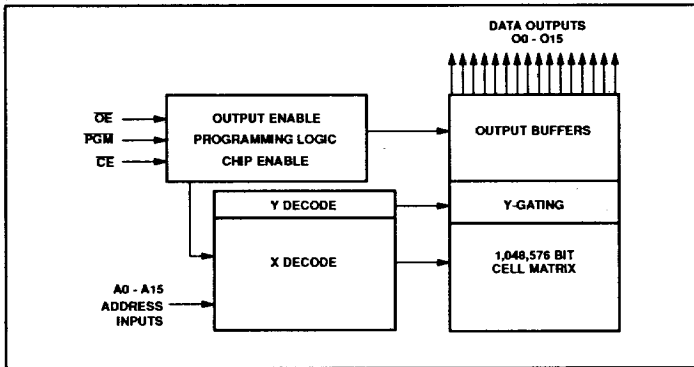
FEATURES

- Low power consumption
 - 100µA maximum CMOS standby current
- High-performance speed
 - 120ns maximum access time
- Noise immunity features
 - ±10% V_{CC} tolerance
 - Maximum latch-up immunity through Epitaxial processing
- Quick-pulse programming algorithm

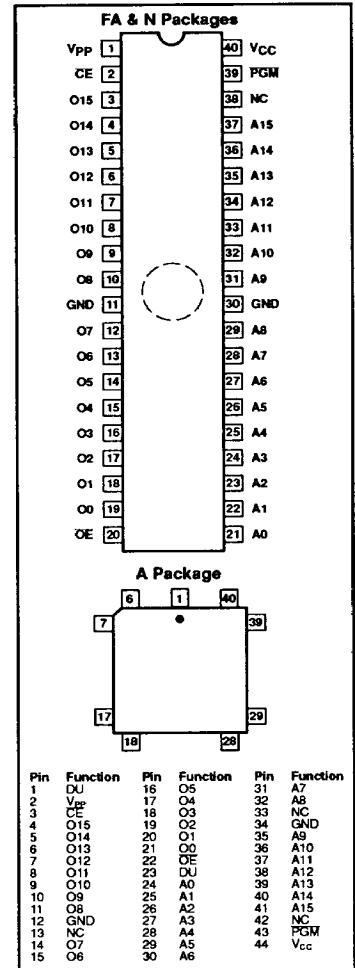
PIN DESCRIPTION

A0 - A15	Address
O0 - O15	Outputs
OE	Output Enable
CE	Chip Enable
PGM	Program Enable
NC	No Connection
GND	Ground
V _{PP}	Program voltage
V _{CC}	Power supply
DU	Don't Use

BLOCK DIAGRAM



PIN CONFIGURATIONS



1 MEG CMOS EPROM (64K × 16)**27C210****READ MODE**

The 27C210 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip enable (CE) is the power control and should be used for device selection. Output Enable (OE) is the output control and should be used to gate

data from the output pins. Data is available at the outputs after a delay of t_{OE} from the falling edge of OE, assuming that CE has been low and addresses have been stable for at least $t_{ACC} - t_{OE}$.

STANDBY MODE

The 27C210 has a standby mode which reduces the maximum V_{CC} current to 100 μ A. It is placed in the Standby mode when CE is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the OE input.

ORDERING INFORMATION

DESCRIPTION	ORDER CODE	
	COMMERCIAL	INDUSTRIAL
40-Pin Ceramic Dual In-Line with quartz window 600mil-wide	27C210-12 FA 27C210-15 FA 27C210-20 FA	27C210I15 FA 27C210I20 FA
40-Pin Plastic Dual In-Line 600mil-wide	27C210-12 N 27C210-15 N 27C210-20 N	27C210I15 N 27C210I20 N
44-Pin Plastic Leaded Chip Carrier 0.69 × 0.6	27C210-12 A 27C210-15 A 27C210-20 A	27C210I15 A 27C210I20 A

ABSOLUTE MAXIMUM RATINGS¹

SYMBOL	PARAMETER	RATING	UNIT
T_{stg}	Storage temperature range	-65 to +125	°C
V_I, V_O	Voltage inputs and outputs	-0.6 to 6.5	V
V_H	Voltage on A9 ² (during intelligent identifier interrogation)	-0.6 to +13.0	V
V_{PP}	Voltage on V_{PP} ² (during programming)	-0.6 to +14.0	V
V_{CC}	Supply voltage ²	-0.6 to +7.0	V

NOTES:

- Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
- All voltages are with respect to network ground.

DEVICE OPERATION¹

MODE	CE	OE	PGM	V_{PP} ²	OUTPUTS
Read	V_{IL}	V_{IL}	V_{IH}	V_{CC}	D_{OUT}
Output Disable	V_{IL}	V_{IH}	V_{IH}	V_{CC}	Hi-Z
Standby	V_{IH}	X^3	X^3	V_{CC}	Hi-Z

OPERATING TEMPERATURE RANGE

PARAMETER	RATING (°C)
Operating temperature range: T_{amb}	COMMERCIAL 0 to +70
	INDUSTRIAL -40 to +85

NOTES:

- All voltages are with respect to network ground.
- V_{PP} may be one diode voltage drop below V_{CC} , and can be connected directly to V_{CC} .
- X can be V_{IH} or V_{IL} .

1 MEG CMOS EPROM (64K × 16)**27C210****DC ELECTRICAL CHARACTERISTICS**Over operating temperature range, $+4.5V \leq V_{CC} \leq +5.5V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP ³	MAX	
Input current						
I _{IH}	Leakage High	V _{IN} = 5.5V = V _{CC}		0.01	1.0	μA
I _{IL}	Leakage Low	V _{IL} = 0V		0.01	-1.0	μA
I _{PP}	V _{PP} read	V _{PP} = V _{CC}			10	μA
Output current						
I _{LO}	Leakage	OE or CE = V _{IH} , V _{OUT} = 5.5V = V _{CC}	-10.0		10.0	μA
I _{OS}	Short circuit ^{7, 9}	V _{OUT} = 0V			100	mA
Supply current						
I _{CC} TTL	Operating (TTL inputs) ^{4, 6}	CE = OE = V _{IL} , f = 8.3MHz V _{PP} = V _{CC} , O0 - O15 = 0mA			50	mA
I _{CC} CMOS	Operating (CMOS inputs) ^{4, 6}	CE = GND, f = 8.3MHz Inputs = V _{CC} or GND, I/O = 0mA			30	mA
I _{SB} TTL	Standby (TTL inputs) ⁴	CE = V _{IH}			1.0	mA
I _{SB} CMOS	Standby (CMOS inputs) ⁵	CE = V _{IH}			100	μA
Input voltage ²						
V _{IL}	Low (TTL)	V _{PP} = V _{CC}	-0.5		0.8	V
V _{IL}	Low (CMOS)	V _{PP} = V _{CC}	-0.2		0.2	V
V _{IH}	High (TTL)	V _{PP} = V _{CC}	2.0		V _{CC} + 0.5	V
V _{IH}	High (CMOS)	V _{PP} = V _{CC}	V _{CC} - 2.0		V _{CC} + 0.2	V
V _{PP}	Read ⁸	(Operating)	V _{CC} - 0.7		V _{CC}	V
Output voltage ²						
V _{OL}	Low	I _{OL} = 2.1mA			0.45	V
V _{OH}	High	I _{OH} = -2.5mA	3.5			V
Capacitance ⁹ T _{amb} = 25°C						
C _{IN}	Address and control	V _{CC} = 5.0V, f = 1.0MHz			6	pF
C _{OUT}	Outputs	V _{IN} = 0V, V _{OUT} = 0V			12	pF

NOTES:

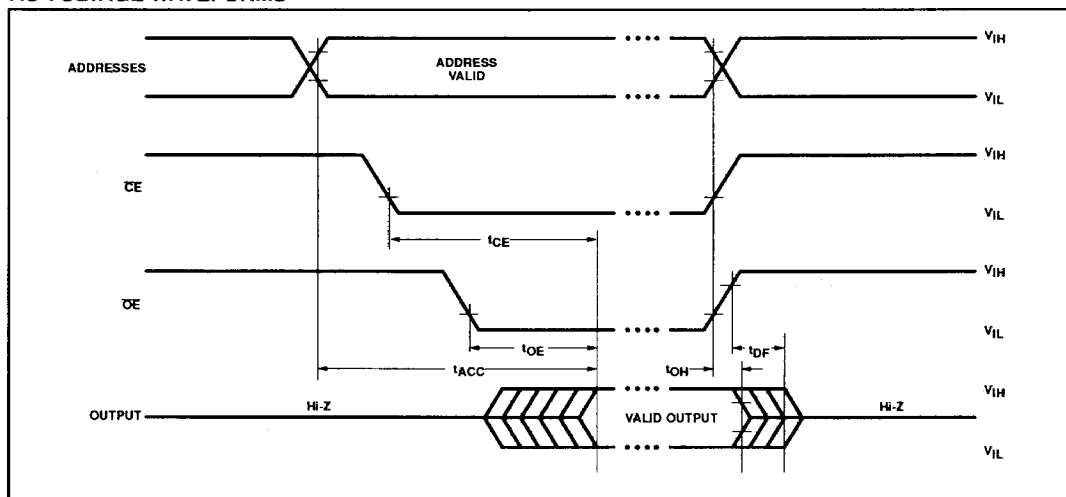
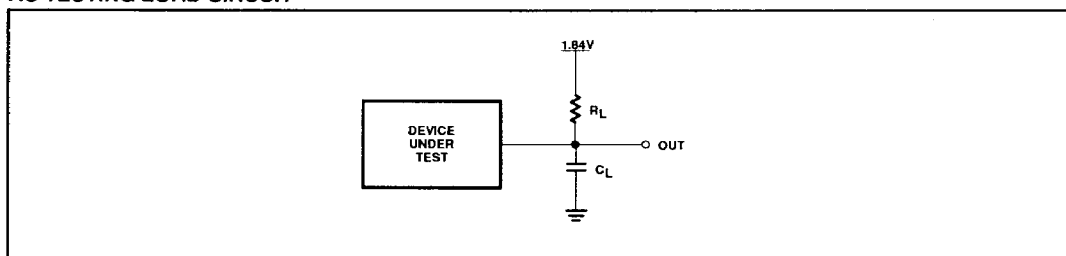
1. Minimum DC input voltage is -0.5V. During transitions the inputs may undershoot to -2.0V for periods less than 20ns.
2. All voltages are with respect to network ground.
3. Typical limits are at $V_{CC} = 5V$, $T_{amb} = 25^{\circ}C$.
4. TTL inputs: Spec V_{IL} , V_{IH} levels.
CMOS inputs: $GND \pm 0.2V$ to $V_{CC} \pm 0.2V$.
5. \overline{CE} is $V_{CC} \pm 0.2V$. All other inputs can have any value within spec.
6. Maximum active power usage is the sum of $I_{PP} + I_{CC}$ and is measured at a frequency of 8.3MHz.
7. Test one output at a time, duration should not exceed 1 second.
8. V_{PP} may be one diode voltage drop below V_{CC} , and can be connected directly to V_{CC} .
9. Guaranteed by design, not 100% tested.

1 MEG CMOS EPROM (64K × 16)**27C210****AC ELECTRICAL CHARACTERISTICS**Over operating temperature range, $+4.5\text{V} \leq V_{CC} \leq +5.5\text{V}$, $R_L = 660\Omega$, $C_L = 100\text{pF}$

SYMBOL	TO	FROM	27C210-12		27C210-15 27C210I15		27C210-20 27C210I20		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
Access time ¹									
t _{ACC}	Output	Address		120		150		200	ns
t _{CE}	Output	CE		120		150		200	ns
t _{OE} ³	Output	OE		50		60		70	ns
Disable time ²									
t _{DF}	Output Hi-Z	OE		30		50		60	ns
t _{OH}	Output hold	Address, CE or OE	0		0		0		ns

NOTES:

1. AC characteristics are tested at $V_{IH} = 2.4\text{V}$ and $V_{IL} = 0.45\text{V}$. Timing measurements made at $V_{OL} = 0.8\text{V}$ and $V_{OH} = 2.0\text{V}$.
2. Guaranteed by design, not 100% tested.
3. \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} .

AC VOLTAGE WAVEFORMS**AC TESTING LOAD CIRCUIT**

1 MEG CMOS EPROM (64K × 16)**27C210****PROGRAMMING INFORMATION**

Complete programming system specifications for both the intelligent programming method and for the quick-pulse programming method are available upon request from Signetics.

Signetics encourages the purchase of programming equipment from a manufacturer who has a full line of programming products to offer. Signetics also encourages the manufacturers of 27C210 programming equipment to submit their equipment for verification of electrical parameters and programming procedures. Information on manufacturers offering equipment certified by Signetics is available upon request from Signetics Memory Marketing.

PROGRAMMING THE 27C210

Caution: Exceeding 14.0V on V_{PP} pin may permanently damage the 27C210.

Initially, all bits of the 27C210 are in the "1" state. Data is introduced by selectively programming "0"s into the desired bit locations. Although only "0"s will be programmed, both "1"s and "0"s can be present in the data word.

The data to be programmed is applied 16 bits in parallel to the data output pins. The levels required for the address and data inputs are standard TTL logic levels.

QUICK-PULSE PROGRAMMING ALGORITHM

Signetics plastic EPROMs can be programmed using the quick-pulse programming algorithm to substantially reduce the throughput time in the production environment. This algorithm typically allows plastic devices to be programmed in under twelve seconds, a significant improvement over previous algorithms. Actual programming time is a function of the PROM programming equipment being used.

The quick-pulse programming algorithm uses initial pulses of 100μs followed by a byte verification to determine when the address byte has been successfully programmed. Up to 25 100μs pulses per byte are provided before a failure is recognized (refer to the following pages for algorithm specifications).

ERASURE CHARACTERISTICS

The erasure characteristics of the 27C210 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000 - 4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C210 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C210 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C210 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity × exposure time) for erasure should be minimum of 15Wsec/cm². The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000μW/cm² power rating. The 27C210 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C210 can be exposed to without damage is 7258Wsec/cm² (1 week @ 12000μW/cm²). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

INTELLIGENT PROGRAMMING ALGORITHM

The 27C210 intelligent programming algorithms rapidly program CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Actual programming times may vary due to differences in programming equipment.

The intelligent identifier also provides the reading out of a binary code from an EPROM that will identify its manufacturer and type. This is intended for use by programming equipment for the purpose of automatically matching the device to be programmed with its corresponding programming algorithm. This mode is functional in the 25° ± 5°C ambient temperature range that is required when programming the 27C210. To activate this mode, the programming equipment must force 11.5V to 12.5V on address A9 of the 27C210. Two bytes may then be read from the device outputs by toggling address line A0 from V_{IL} to V_{IH}. The CE, OE and all other address lines must be at V_{IL} during interrogation.

The identifier information for Signetics 27C210 is as follows:

When A0 = V _{IL} data is "Manufacturer"	FF15(HEX)
When A0 = V _{IH} data is "Product"	FF17(HEX)

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. The programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial PGM pulse(s) is 1ms, which is then followed by a longer overprogram pulse of 3Xms. X is an iteration counter and is equal to the number of the initial 1ms pulses applied to a particular location before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram pulse is applied (refer to the following pages for algorithm specifications).

CMOS NOISE CHARACTERISTICS

Special epitaxial processing techniques have enabled Signetics to build CMOS with features that add to system reliability. These include input/output protection to latch-up for stresses up to 100mA on Address and Data pins that range from -1V to (V_{CC} + 1V). In addition, the V_{PP} (Programming) pin is designed to resist latch-up to the 14V maximum device limit.

SIGNETICS DISCOURAGES THE CONSTRUCTION AND USE OF "HOMEMADE" PROGRAMMING EQUIPMENT

In order to consistently achieve excellent programming yields, periodic calibration of the programming equipment is required. Consult the equipment manufacturer for the recommended calibration interval. Signetics warranty for programmability extends only to product that has been programmed on certified equipment that has been serviced to the manufacturers recommendation.

1 MEG CMOS EPROM (64K × 16)**27C210****INTELLIGENT PROGRAMMING ALGORITHM****DC PROGRAMMING CHARACTERISTICS** $T_{amb} = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, $V_{CC} = 6.0\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.5\text{V}$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I_I	Input current (all inputs)	$V_{IN} = V_{IL} \text{ or } V_{IH}$		1.0	μA
V_{IL}	Input low level (all inputs)		-0.1	0.8	V
V_{IH}	Input high level		2.4	6.5	V
V_{OL}	Output low voltage during verify	$I_{OL} = 2.1\text{mA}$		0.45	V
V_{OH}	Output high voltage during verify	$I_{OH} = -2.5\text{mA}$	3.5		V
I_{CC2}	V_{CC} supply current	$Q0 - 15 = 0\text{mA}$		50	mA
I_{PP2}	V_{PP} supply current (program)	$\overline{CE} = V_{IL}$		50	mA

AC PROGRAMMING CHARACTERISTICS

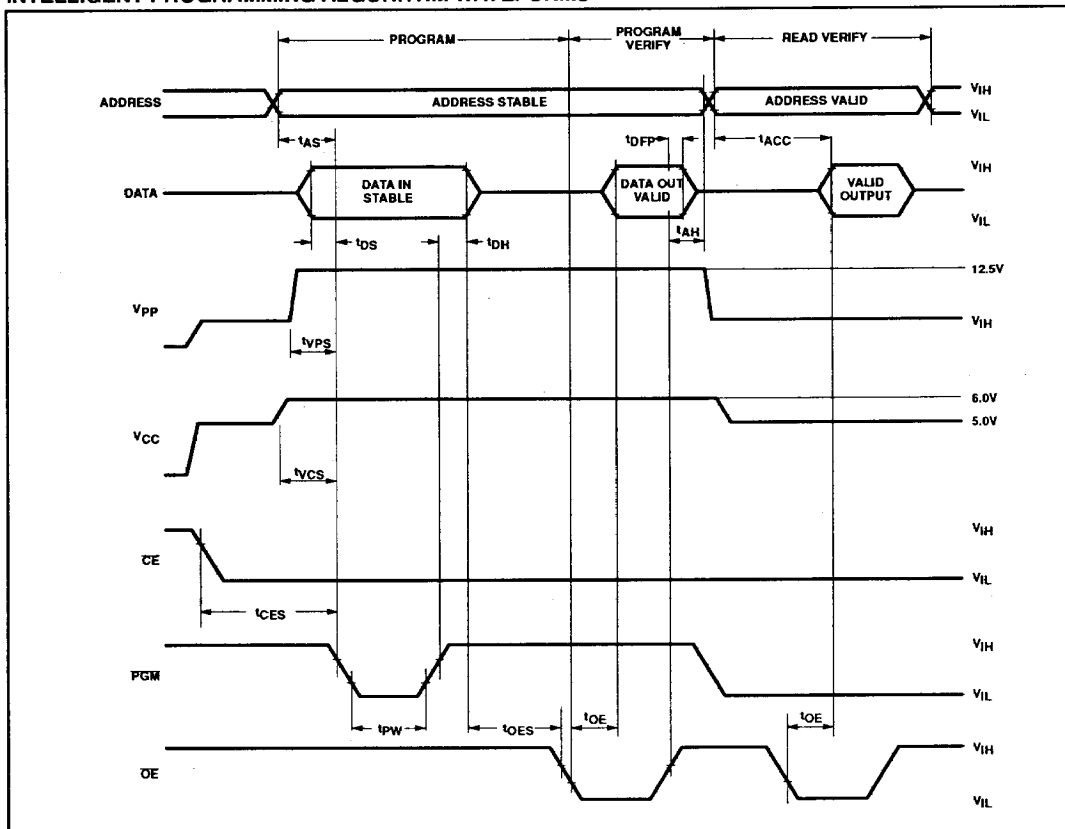
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t_{AS}	Address setup time		2			μs
t_{OES}	\overline{OE} setup time		2			μs
t_{DS}	Data setup time		2			μs
t_{AH}	Address hold time		0			μs
t_{DH}	Data hold time		2			μs
t_{OFF}^3	\overline{OE} high to output float delay		0		130	ns
t_{VPS}	V_{PP} setup time		2			μs
t_{VCS}	V_{CC} setup time		2			μs
t_{CES}	\overline{CE} setup time		2			μs
t_{PW}	\overline{CE} initial program pulse width	Note 1	0.95	1.0	1.05	ms
t_{OPW}	\overline{CE} overprogram pulse width	Note 2	2.85		78.75	ms
t_{OE}	Data valid from \overline{OE}				150	μs

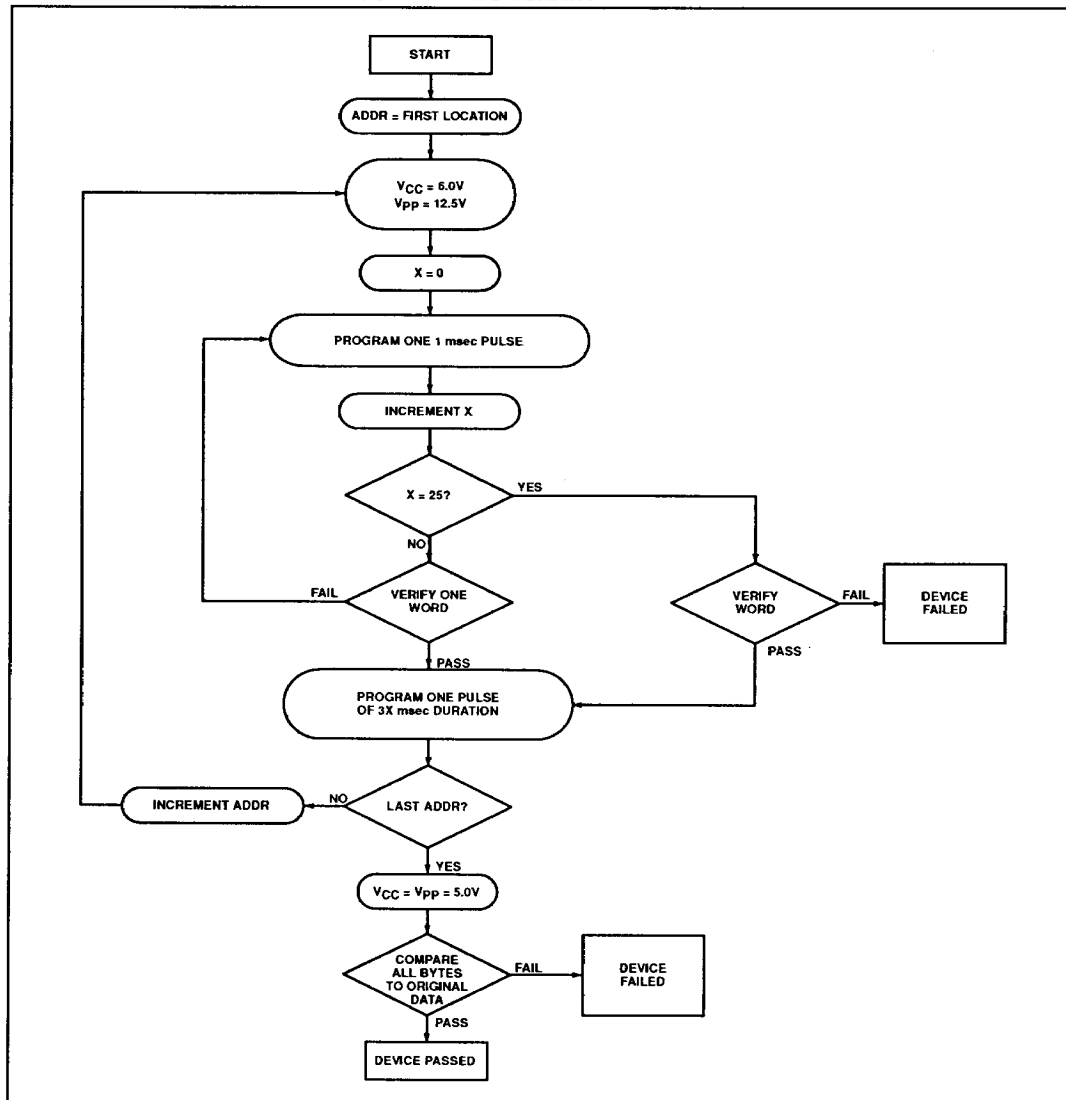
AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%) 20ns
 Input Pulse Levels 0.45V to 2.4V
 Input Timing Reference Level 0.8V and 2.0V
 Output Timing Reference Level 0.8V and 2.0V

NOTES:

1. Initial program pulse width tolerance is $1\text{ms} \pm 5\%$.
2. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of iteration counter value X.
3. The parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
4. During programming, a 0.1 μF capacitor is required from V_{PP} to GND node, to suppress voltage transients that can damage the device.

1 MEG CMOS EPROM (64K × 16)**27C210****INTELLIGENT PROGRAMMING ALGORITHM WAVEFORMS**

1 MEG CMOS EPROM (64K × 16)**27C210****INTELLIGENT PROGRAMMING ALGORITHM FLOWCHART**

1 MEG CMOS EPROM (64K × 16)**27C210****QUICK PULSE PROGRAMMING ALGORITHM****DC PROGRAMMING CHARACTERISTICS**T_{amb} = 25°C ±5°C, V_{CC} = 6.25V ±0.25V, V_{PP} = 12.75V ±0.25V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			MIN	MAX	
I _I	Input current (all inputs)	V _{IN} = V _{IL} or V _{IH}		1.0	μA
V _{IL}	Input low level (all inputs)		-0.1	0.8	V
V _{IH}	Input high level		2.4	6.5	V
V _{OL}	Output low voltage during verify	I _{OL} = 2.1mA		0.45	V
V _{OH}	Output high voltage during verify	I _{OH} = -2.5mA	3.5		V
I _{CC2}	V _{CC} supply current	Q0 - 15 = 0mA		50	mA
I _{PP2}	V _{PP} supply current (program)	CE = V _{IL}		50	mA
V _{PP}	Programming voltage		12.5	13.0	V

AC PROGRAMMING CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
t _{AS}	Address setup time		2			μs
t _{OES}	OE setup time		2			μs
t _{DS}	Data setup time		2			μs
t _{AH}	Address hold time		0			μs
t _{OH}	Data hold time		2			μs
t _{OFF} ³	OE high to output float delay		0		130	ns
t _{VPS}	V _{PP} setup time		2			μs
t _{VCS}	V _{CC} setup time		2			μs
t _{PW}	CE initial program pulse width	Note 1	.095	0.100	0.105	ms
t _{OPW}	CE overprogram pulse width	Note 2	2.85		78.8	ms
t _{OE}	Data valid from OE				150	μs

AC CONDITIONS OF TEST

Input Rise and Fall Times (10% to 90%)	20ns
Input Pulse Levels	0.45V to 2.4V
Input Timing Reference Level	0.8V and 2.0V
Output Timing Reference Level	0.8V and 2.0V

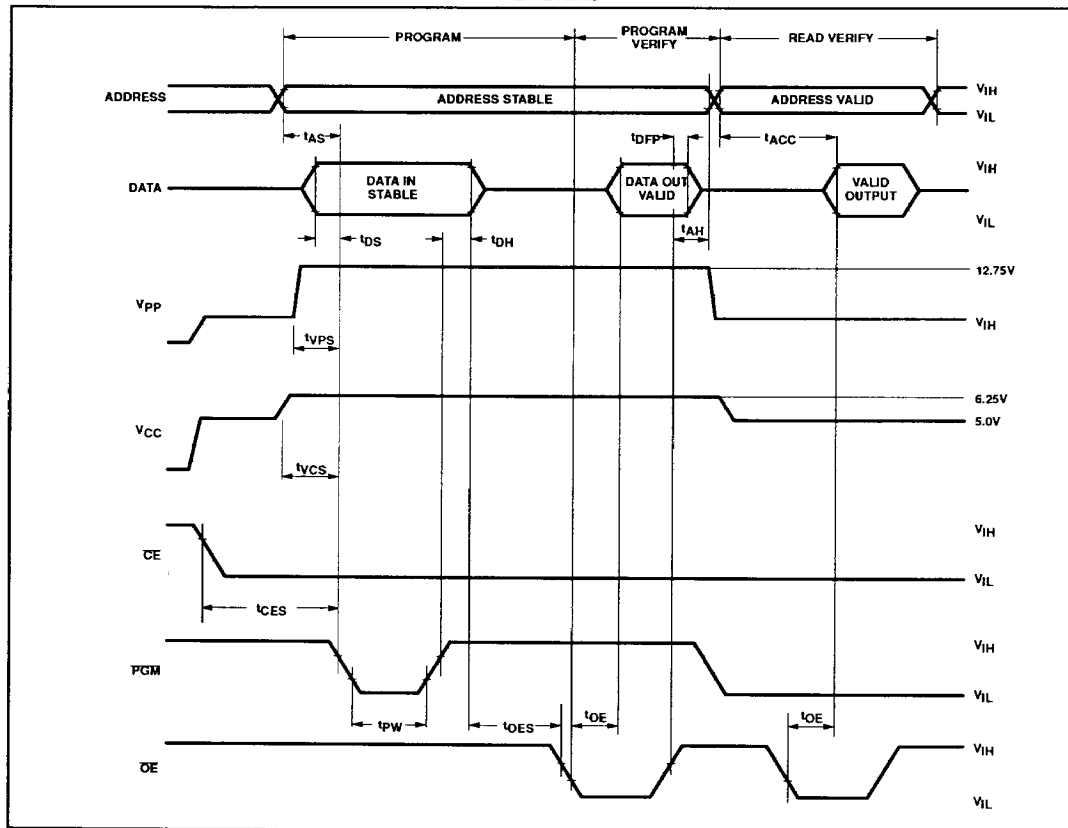
NOTES:

- Initial program pulse width tolerance is 1ms ±5%.
- The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of iteration counter value X.
- The parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven – see timing diagram.
- During programming, a 0.1μF capacitor is required from V_{PP} to GND node, to suppress voltage transients that can damage the device.

1 MEG CMOS EPROM (64K × 16)

27C210

QUICK PULSE PROGRAMMING ALGORITHM WAVEFORMS



1 MEG CMOS EPROM (64K × 16)**27C210****QUICK PULSE PROGRAMMING ALGORITHM FLOWCHART**