MOTOROLA

Dual J-K Master-Slave Flip-Flop

Military 10H535

ELECTRICALLY TESTED PER:
5962-8750501

The 10H535 is a dual master-slave dc coupled J-K flip-flop. The device is provided with asynchronous set(s) and Reset (R). These set and reset inputs override the clock.

A common clock is provided with separate $\overline{J}$-$\overline{K}$ inputs. When the clock is static, the $\overline{J}$-$\overline{K}$ inputs do not effect the output.

The output states of the flip-flop change on the positive transition of the clock.

- Propagation Delay, 1.5 ns Typical
- 410 mW Max/Pkg (No Load)
- f_{Tog} = 250 MHz Max
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

AVAILABLE AS

1) JAN: N/A
2) SMD: 5962-8750501
3) 883: 10H535/BXAJC
X = CASE OUTLINE AS FOLLOWS:

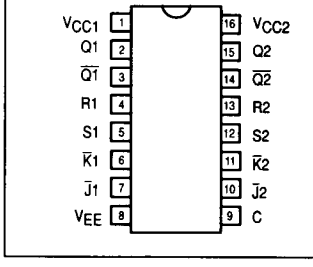
PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before the slash on LCC.

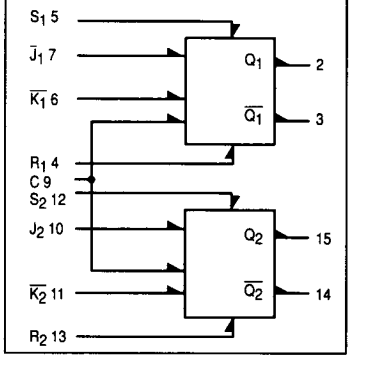
PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
V_{CC1}	1	5	2	GND
Q_1	2	6	3	51 Ω to V_{TT}
$\overline{Q_1}$	3	7	4	51 Ω to V_{TT}
R_1	4	8	5	51 Ω to V_{TT}
S_1	5	9	7	GND
$\overline{K_1}$	6	10	8	OPEN
$\overline{J_1}$	7	11	9	OPEN
V_{EE}	8	12	10	V_{EE}
C	9	13	12	OPEN
$\overline{J_2}$	10	14	13	OPEN
$\overline{K_2}$	11	15	14	OPEN
S_2	12	16	15	GND
R_2	13	1	17	51 Ω to V_{TT}
$\overline{Q_2}$	14	2	18	51 Ω to V_{TT}
Q_2	15	3	19	51 Ω to V_{TT}
V_{CC2}	16	4	20	GND

BURN - IN CONDITIONS:
V_{TT} = – 2.0 V MAX/ – 2.2 V MIN
V_{EE} = – 5.7 V MAX/ – 5.2 V MIN



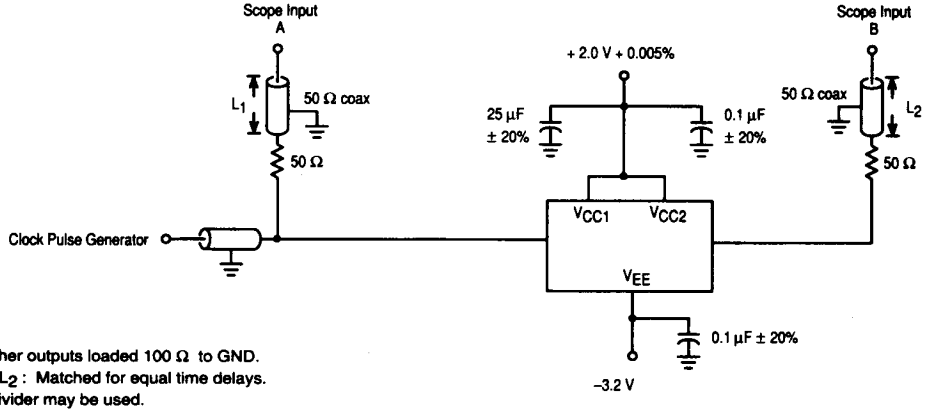
LOGIC DIAGRAM



R-S Truth Table		
R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined
A clock H is a clock transition from a Low to High state

Clock Truth Table		
$\overline{J}$	$\overline{K}$	Q_{n+1}
L	L	$\overline{Q}_n$
H	L	L
L	H	H
H	H	Q_n



NOTES

1. All other outputs loaded 100 Ω to GND.
2. $L_1 = L_2$: Matched for equal time delays.
3. 2:1 divider may be used.
4. $V_{IN} \geq 20$ ns.
5. $f_{IN} = 1.0$ MHz.
6. $t_r = t_f = 1.0$ ns ± 0.1 ns.

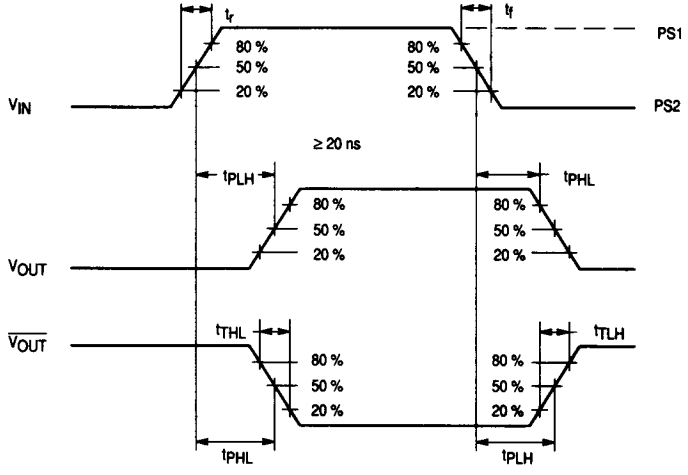
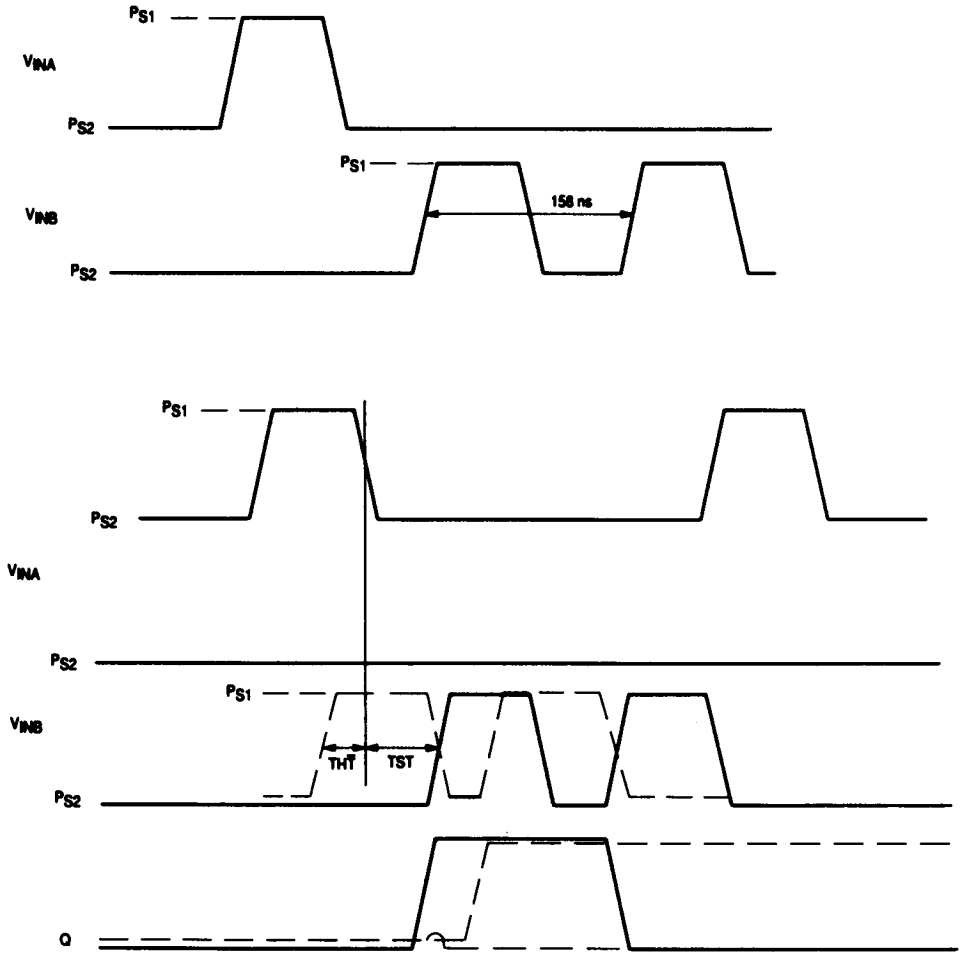


Figure 1. Switching Test Circuit and Waveforms



NOTES
1. TST = Minimum set up time for Toggle.
2. THT = Minimum hold time for Not Toggle.

Figure 2. Set, Reset and Toggle Waveforms

10H535
QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to –2.0 volts.

Test Temperature	Test Voltage Values (Volts)								
	V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	P_{S1}	P_{S2}	V_{EE1}	V_{EE2}	V_{EE2}
T_A = 25 °C	-0.780	-1.950	-1.11	-1.48	+1.11	+0.31	-5.46	-4.94	-2.94
T_A = 125 °C	-0.650	-1.950	-0.96	-1.465	+1.24	+0.36	-5.46	-4.94	-2.94
T_A = - 55 °C	-0.840	-1.950	-1.16	-1.51	+1.01	+0.28	-5.46	-4.94	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
	Functional Parameters:	+ 25 °C		+ 125 °C		– 55 °C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V_{IH1}	V_{IL1}	V_{IH2}	V_{IL2}	V_{EE2}	V_{EE1}	V_{CC}	P. U. T.
V_{OH}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5, 12, 13					8	1, 16	2, 3, 14, 15
V_{OL}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4, 5, 12, 13					8	1, 16	2, 3, 14, 15
V_{OH1}	High Output Voltage	–1.01	–0.78	–0.86	–0.65	–1.06	–0.84	V	4, 5, 12, 13	4 – 7 9 – 13	4, 5, 12, 13	4 – 7 9 – 13	8	8	1, 16	2, 3, 14, 15
V_{OL1}	Low Output Voltage	–1.95	–1.58	–1.95	–1.565	–1.95	–1.61	V	4, 5, 12, 13	4 – 7 9 – 13	4, 5 12, 13	4 – 7 9 – 13	8	8	1, 16	2, 3, 14, 15
I_{EE}	Power Supply Current	–68		–75		–75		mA						8	1, 16	8
I_{IH}	Input Current High		285		460		460	µA	6, 7, 10, 11					8	1, 16	6, 7, 10, 11
I_{IH1}	Input Current High		420		675		675	µA	9					8	1, 16	9
I_{IH2}	Input Current High		500		800		800	µA	4, 5, 12, 13					8	1, 16	4, 5, 12, 13
I_{IL}	Input Current Low	0.5		0.3		0.5		µA		4 – 7 9 – 13			8		1, 16	4 – 7, 9 – 13

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Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW					
	Functional Parameters:	+ 25° C		+ 125° C		– 55° C			Pinouts referenced are for DIL package, check Pin Assignments V_{CC} = 2.0 V, Output Load = 100 Ω to GND					
		Subgroup 9		Subgroup 10		Subgroup 11								
		Min	Max	Min	Max	Min	Max		P_{S2}	V_{IN}	V_{OUT}	V_{CC}	V_{EEL}	P.U.T.
t_{TLH1} t_{TLH1}	Rise Time 1 or Fall Time 1	0.5	2.0	0.7	2.4	0.5	2.0	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{TLH2} t_{TLH2}	Rise Time 2 or Fall Time 2	0.5	2.0	0.7	2.4	0.5	2.0	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH1} t_{PLH1}	Propagation Delay 1 Set, Reset	0.7	2.3	0.7	2.6	0.5	2.3	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{PLH2} t_{PLH2}	Propagation Delay 2 Clock	0.7	2.3	0.7	2.6	0.5	2.3	ns	6, 7, 10, 11	4, 5, 9, 14	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t_{SETUP}	Setup Time	1.5		1.5		1.5		ns	6, 7, 10, 11	6, 7, 10, 11	3, 14	1, 16	8	3, 14
t_{HOLD}	Hold Time	1.0		1.0		1.0		ns	6, 7, 10, 11	6, 7, 10, 11	3, 14	1, 16	8	3, 14
f_{tog}	Toggle Frequency	250		250		250		MHz	6, 7, 10, 11	6, 7, 10 -11	3, 14	1, 16	8	3, 14