



Dual 4-5 Input "OR/NOR" Gate

ELECTRICALLY TESTED PER:
5962-8985601

The 10H509 is a dual 4-5 input **OR/NOR** gate. This MECL 10H part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay, and no increase in power-supply current.

- Propagation Delay, 1.0 ns Typical
- 40 mW Max/Gate (No Load)
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K-Compatible

PIN ASSIGNMENTS

FUNCTION	DIL	FLATS	LCC	BURN-IN (CONDITION C)
VCC1	1	5	2	GND
AOUT	2	6	3	51 Ω to V _{TT}
$\overline{AOUT}$	3	7	4	51 Ω to V _{TT}
A ₁ N	4	8	5	51 Ω to V _{TT}
A ₂ N	5	9	7	GND
A ₃ N	6	10	8	OPEN
A ₄ N	7	11	9	OPEN
VEE	8	12	10	VEE
B ₁ N	9	13	12	OPEN
B ₂ N	10	14	13	OPEN
B ₃ N	11	15	14	OPEN
B ₄ N	12	16	15	GND
B ₅ N	13	1	17	51 Ω to V _{TT}
$\overline{BOUT}$	14	2	18	51 Ω to V _{TT}
BOUT	15	3	19	51 Ω to V _{TT}
VCC2	16	4	20	GND

BURN - IN CONDITIONS:

V_{TT} = - 2.0 V MAX/ - 2.2 V MIN

VEE = - 5.7 V MAX/ - 5.2 V MIN

Military 10H509

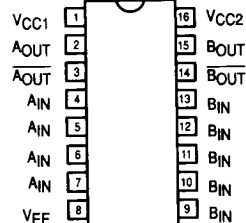


AVAILABLE AS

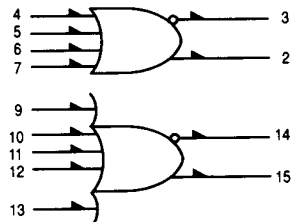
- 1) JAN: N/A
 - 2) SMD: 5962-8985601
 - 3) 883: 10H509/BXAJC
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: CERDIP: E
CERFLAT: F
LCC: 2

The letter "M" appears before
the slash on LCC.

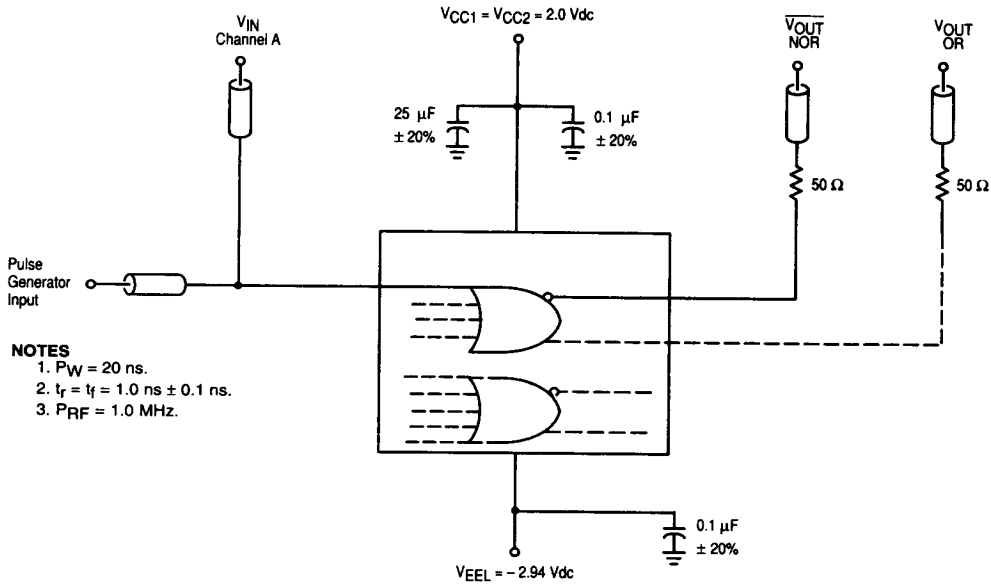


POSITIVE LOGIC DIAGRAM



10H509

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NOTES

1. Perform test in accordance with test table; each output is tested separately.
2. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable. Wire length should be ≤ 0.250 (6.35 mm) from TP_{IN} to input pin and TP_{OUT} to output pin.
3. Outputs not under test should be connected to a 100 Ω resistor to ground.

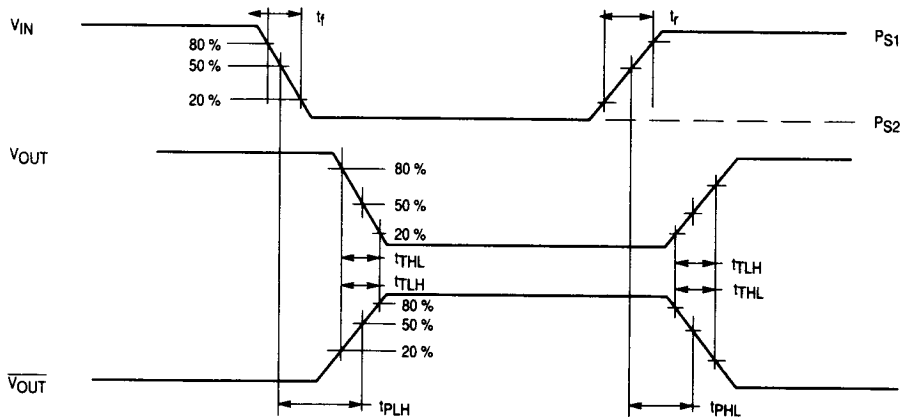


Figure 1. Switching Test Circuit and Waveforms

10H509 QUIESCENT LIMIT TABLE *

* ELECTRICAL CHARACTERISTICS

Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100 Ω resistor to - 2.0 volts.

Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{TTL}	V _{ITH}	V _{CC}	V _{EE1}
T _A = 25 °C	-0.78	-1.95	-1.11	+0.31	-1.475	-1.105	0	-5.2
T _A = 125 °C	-0.85	-1.95	-0.96	+0.36	-1.400	-1.000	0	-5.2
T _A = -55 °C	-0.84	-1.95	-1.16	+0.28	-1.510	-1.255	0	-5.2

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW							
		+ 25 °C		+ 125 °C		- 55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 0 V, Output Load = 100 Ω to - 2.0 V							
		Subgroup 1		Subgroup 2		Subgroup 3										
		Min	Max	Min	Max	Min	Max		V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{CC}	V _{EE1}	P. U. T.	
	Functional Parameters:															
V _{OH}	High Output Voltage	-0.93	-0.78	-0.825	-0.63	-1.06	-0.88	V	4 - 7 9 - 13	4 - 7 9 - 13			1, 16	8	2, 3, 14, 15	
V _{OL}	Low Output Voltage	-1.86	-1.62	-1.82	-1.545	-1.92	-1.655	V	4 - 7 9 - 13	4 - 7 9 - 13			1, 16	8	2, 3, 14, 15	
V _{OTH}	High Output Voltage	-0.96		-0.845		-1.1		V			4 - 7 9 - 13	4 - 7 9 - 13	1, 16	8	2, 3, 14, 15	
V _{OTL}	Low Output Voltage		-1.6		-1.525		-1.635	V			4 - 7 9 - 13	4 - 7 9 - 13	1, 16	8	2, 3, 14, 15	
I _{EE}	Power Supply Current	-14		-16		-16		mA					1, 16	8	8	
I _{IH}	Input Current High		265		450		450	μA	4 - 7 9 - 13				1, 16	8	4 - 7, 9 - 13	
I _{IL}	Input Current Low	0.5		0.3		0.5		μA		4 - 7 9 - 13			1, 16	8	4 - 7, 9 - 13	

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Test Temperature	Test Voltage Values (Volts)							
	V _{IH1}	V _{IL1}	V _{IH2}	V _{IL2}	V _{ITL}	V _{ITH}	V _{CC}	VEEL
T _A = 25 °C	-0.78	-1.85	-1.11	+0.31	-1.475	-1.105	0	-2.94
T _A = 125 °C	-0.63	-1.82	+1.24	+0.36	-1.400	-1.000	0	-2.94
T _A = -55 °C	-0.88	-1.92	+1.01	+0.28	-1.510	-1.255	0	-2.94

Symbol	Parameter	Limits						Units	TEST VOLTAGE APPLIED TO PINS BELOW:				
	Functional Parameters:	+25 °C		+125 °C		-55 °C			Pinouts referenced are for DIL package, check Pin Assignments VCC = 2.0 V, Output Load = 100 Ω to GND				
		Subgroup 9		Subgroup 10		Subgroup 11							
		Min	Max	Min	Max	Min	Max						
t _{TLH}	Rise Time	0.4	2.1	0.4	2.3	0.35	2.0	ns	V _{IN}	V _{OUT}	V _{CC}	VEEL	P.U.T.
t _{THL}	Fall Time	0.4	2.1	0.4	2.3	0.35	2.0	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t _{PLH}	Propagation Delay Low to High	0.4	2.1	0.4	2.3	0.35	2.0	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t _{PLH}	Propagation Delay High to Low	0.3	1.3	0.45	1.6	0.25	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15
t _{PHL}	Propagation Delay High to Low	0.3	1.3	0.45	1.6	0.25	1.3	ns	6, 11	2, 3, 14, 15	1, 16	8	2, 3, 14, 15